Logic Circuits Course

Ch. 6-3

Functions of Combinational Logic

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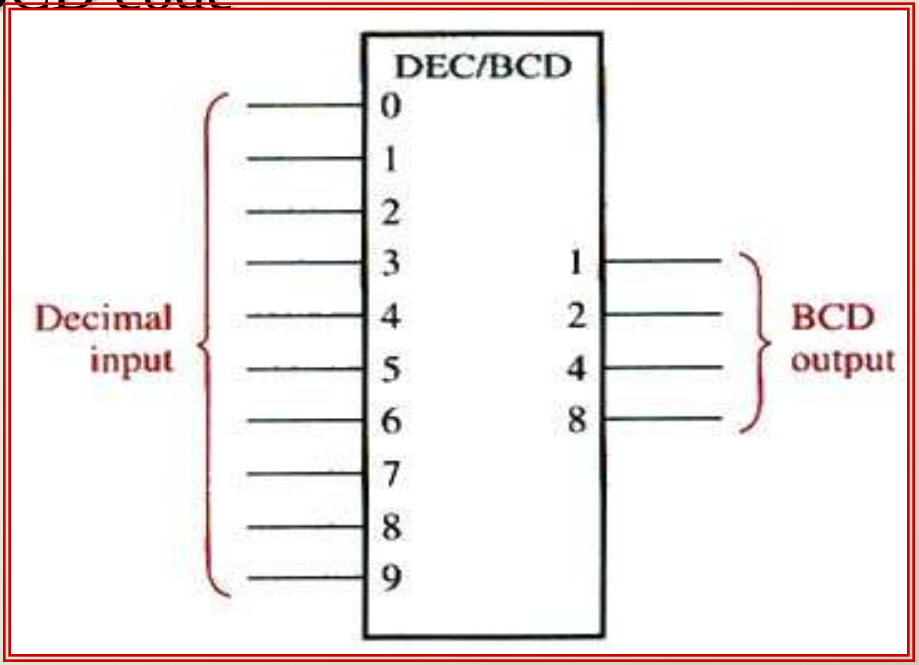
Functions of Combinational Logic

1. Basic Adders
2. Parallel Binary Adders
3. Ripple Carry versus Look-Ahead Carry Adders
4. Comparators
5. Decoders
6. Encoders
7. Code Conversion
8. Multiplexers (data Selectors)
9. Demultiplexers
10. Parity Generators/Checkers

6. Encoders

An encoder is a combinational logic circuit that essentially performs a reverse decoder function. An encoder accepts an active level on one of its inputs representing a digit such a decimal or octal and converts it to a coded output such as BCD or Binary.

The Decimal-to-BCD Encoder :- This type of encoder has ten inputs- one for each decimal digit-and four outputs corresponding to the BCD code

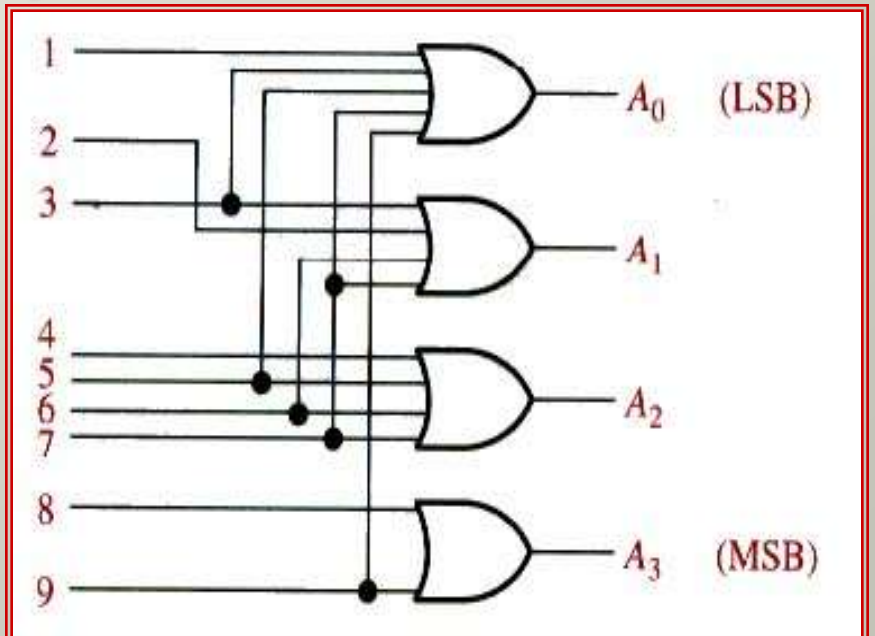


DECIMAL DIGIT	BCD CODE A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

From the table you can determine the following :-

- The MSB of the BCD A_3 is always 1 for decimal digit 8 and 9. So $A_3 = 8 + 9.$
- Bit A_2 is always 1 for decimal digit 4,5,6, or 7 can be expressed as $A_2 = 4 + 5 + 6 + 7$
- Bit A_1 is always 1 for decimal digit 2,3,6 or 7 can be expressed as $A_1 = 2 + 3 + 6 + 7$
- Finally A_0 is always a 1 for decimal digit 1,3,5,7, or 9 can be expressed as $A_0 = 1 + 3 + 5 + 7 + 9$

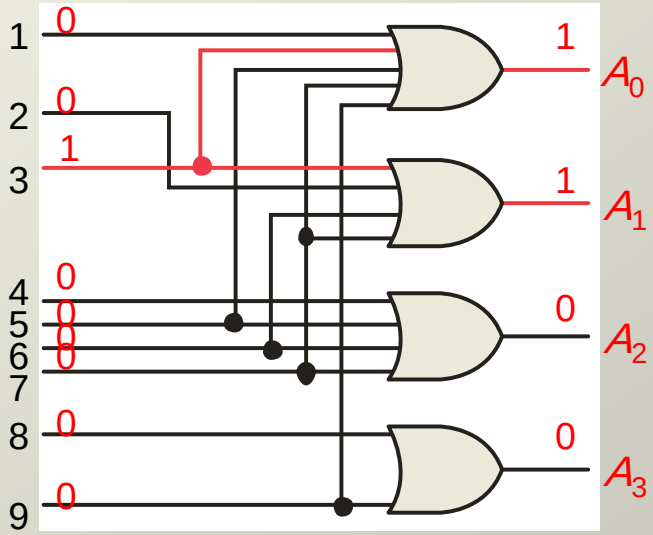
This condition will produce HIGH on output A_0 and A_3 and LOW on outputs A_1 and A_2 which the BCD code (1001) for decimal 9.



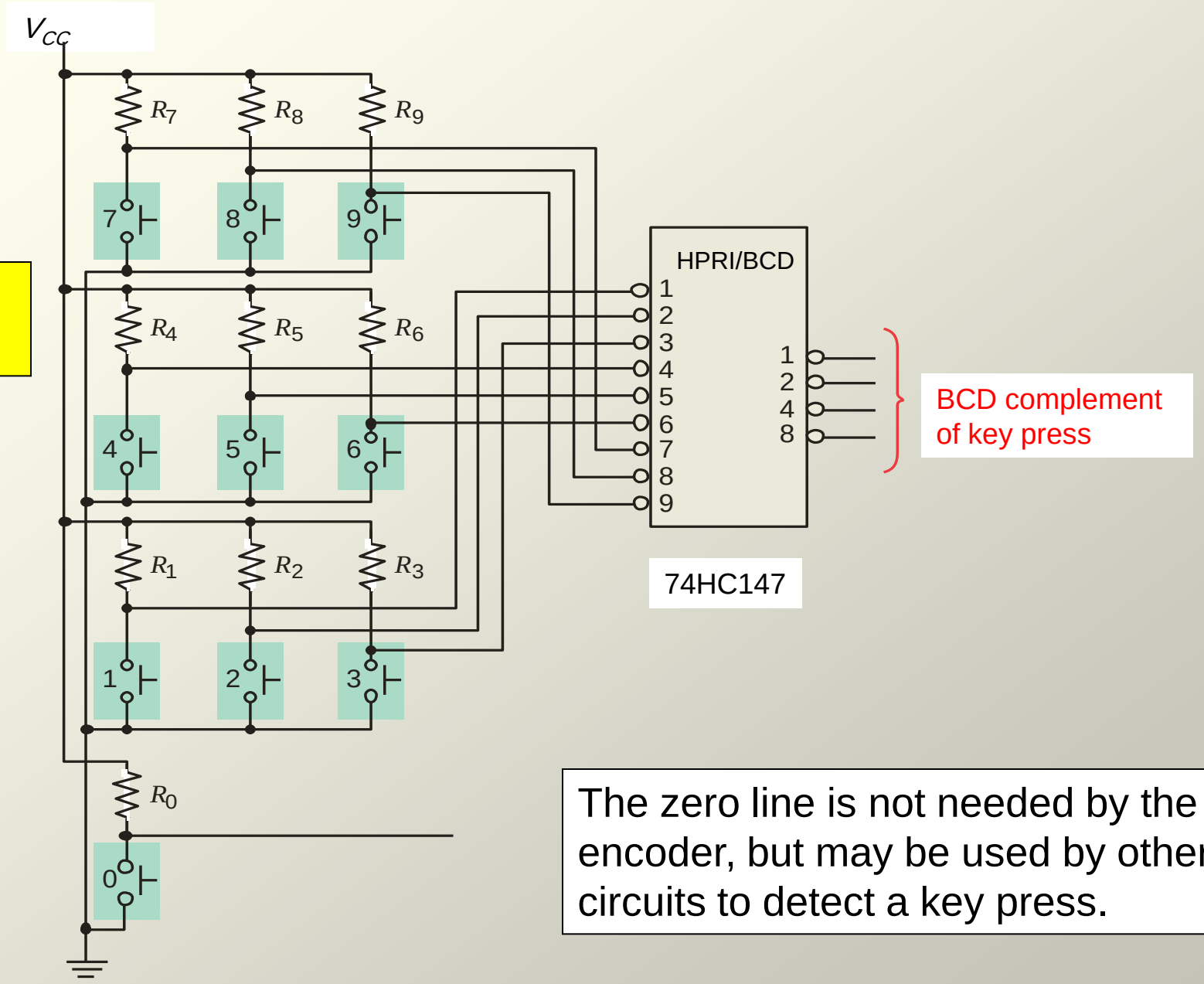
Example

Show how the decimal-to-BCD encoder converts the decimal number 3 into a BCD 0011.

The top two OR gates have ones as indicated with the red lines. Thus the output is 0111.



Keyboard encoder

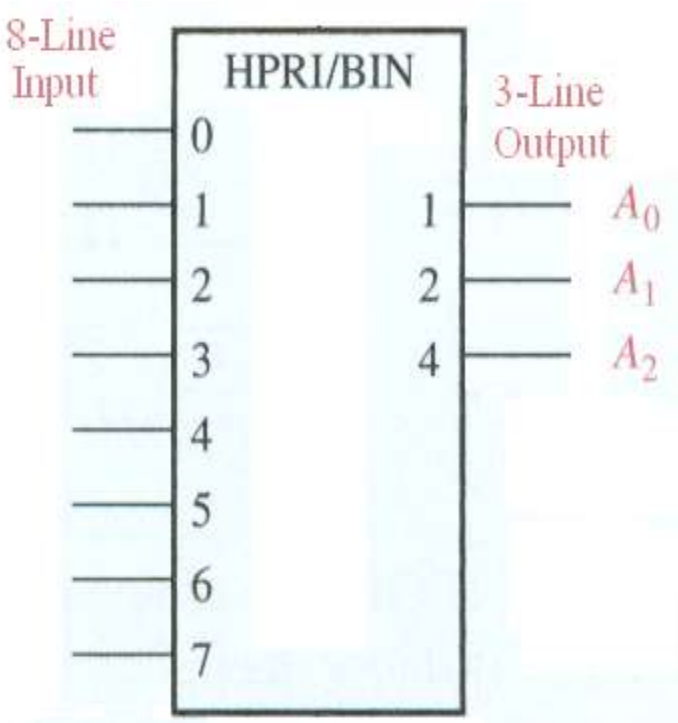


The zero line is not needed by the encoder, but may be used by other circuits to detect a key press.

Encoders

- 8-line-to-3-line encoder

8-LINE INPUT	3-LINE OUTPUT		
	A_2	A_1	A_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



7. Code Converters

BCD-to-Binary Conversion :- One method of BCD-to-binary conversion uses adder circuits. The basic conversion process is as follows:-

1. The value, or weight of each bit in BCD number is represented by a binary number.
2. All of the binary representations of the weights of bits are 1s in the BCD number is added.
3. The result of this addition is the binary equivalent of the BCD number.

Example :- let's take the BCD number 1000 0111 → 8 7

The left most 4-bit group represents 80, and the right most 4-bit group represents 7 because the left most group has a weight of 10, and the right-most group has a weight of 1. within each group, the binary weight of each bit is as follows:

BCD Tens Digit Units Digit

weight: 80 40 20 10 8 4 2 1

Bit Designation: B_3 B_2 B_1 B_0 A_3 A_2 A_1 A_0

The binary equivalent of each BCD bit is a binary number representing the weight of that bit within the total BCD number.

BCD BIT	BCD WEIGHT	(MSB) BINARY REPRESENTATION						(LSB)
		64	32	16	8	4	2	1
A_0	1	0	0	0	0	0	0	1
A_1	2	0	0	0	0	0	1	0
A_2	4	0	0	0	0	1	0	0
A_3	8	0	0	0	1	0	0	0
B_0	10	0	0	0	1	0	1	0
B_1	20	0	0	1	0	1	0	0
B_2	40	0	1	0	1	0	0	0
B_3	80	1	0	1	0	0	0	0

Example :- convert the BCD numbers 00100111 (decimal 27) and 10011000 (decimal 98) to binary.

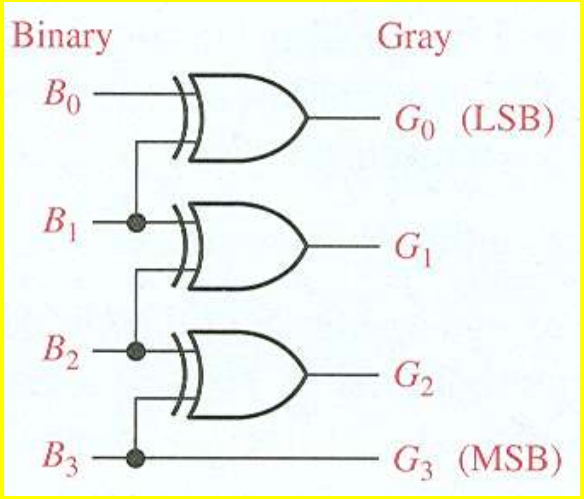
Solution Write the binary representations of the weights of all 1s appearing in the numbers, and then add them together.

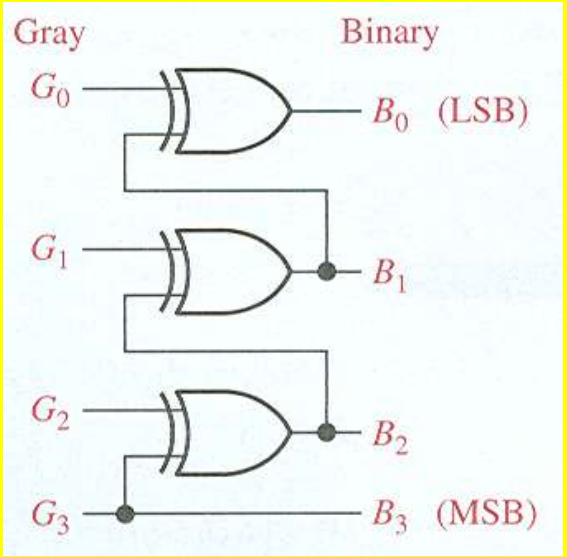
80	40	20	10	8	4	2	1		
0	0	1	0	0	1	1	1		
								0000001	1
								0000010	2
								0000100	4
								+ 0010100	20
								0011011	Binary number for decimal 27

80	40	20	10	8	4	2	1		
1	0	0	1	1	0	0	0		
								0001000	8
								0001010	10
								+ 1010000	80
								1100010	Binary number for decimal 98

Code Converters

- Binary-Gray conversions

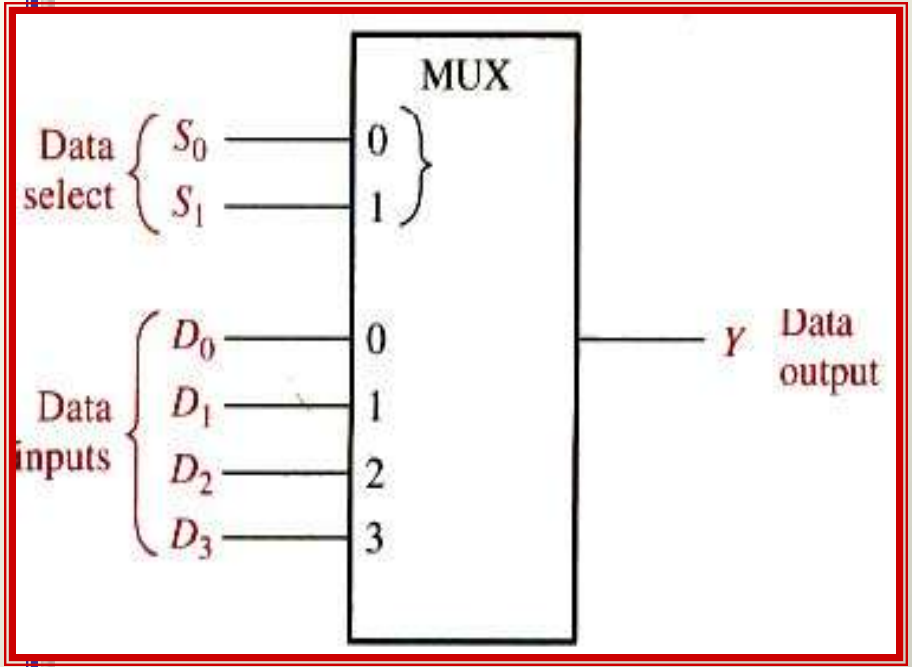




BINARY	GRAY CODE
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

8. Multiplexers (Data Selectors)

A multiplexer (MUX) selects one data line from two or more input lines and routes data from the selected line to the output. The particular data line that is selected is determined by the select inputs.



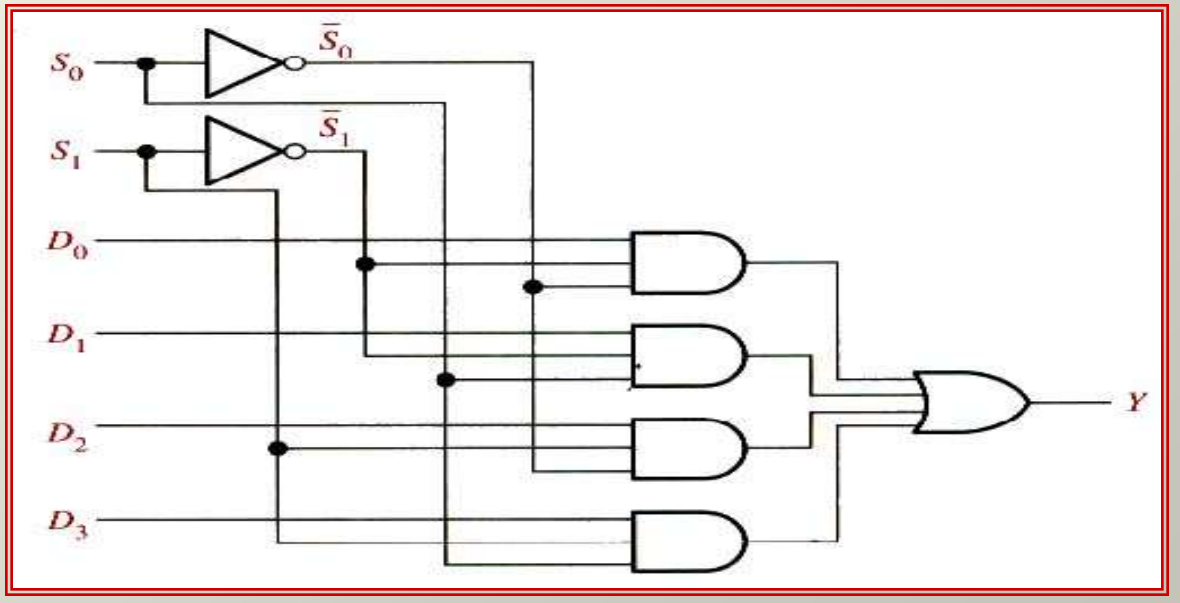
DATA-SELECT INPUTS S_1	DATA-SELECT INPUTS S_0	INPUT SELECTED
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

The logic circuitry required to perform multiplexing are:-

- The data output is equal to D_0 only if S_1=0 and S_0=0 :
- The data output is equal to D_1 only if S_1=0 and S_0=1 :
- The data output is equal to D_2 only if S_1=1 and S_0=0 :
- The data output is equal to D_3 only if S_1=1 and S_0=1 :

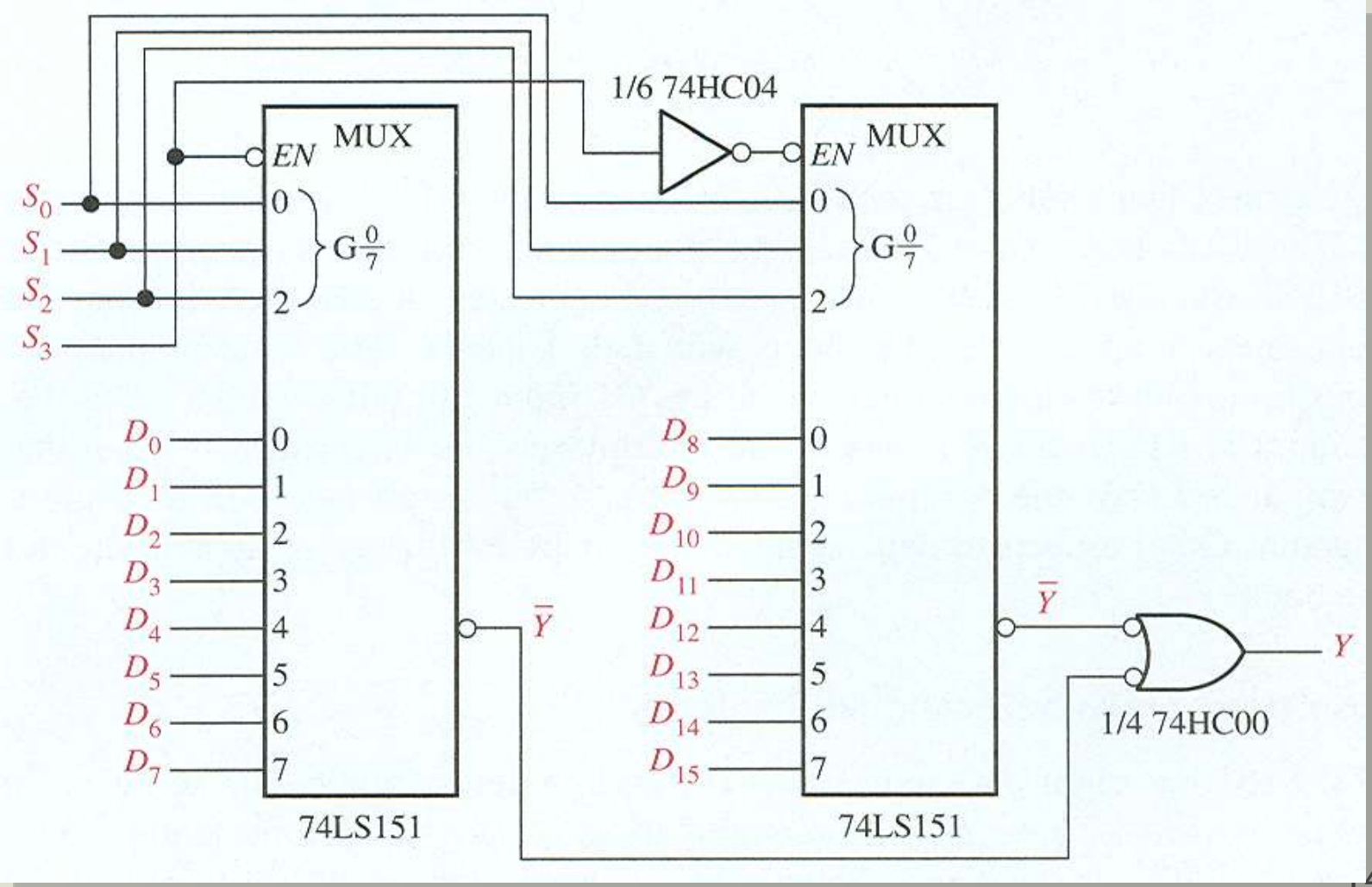
When the sum are Ored the total expression for the data output is

$$Y = D_0 \overline{S}_1 \overline{S}_0 + D_1 \overline{S}_1 S_0 + D_2 S_1 \overline{S}_0 + D_3 S_1 S_0$$



Multiplexers (Data Selectors)

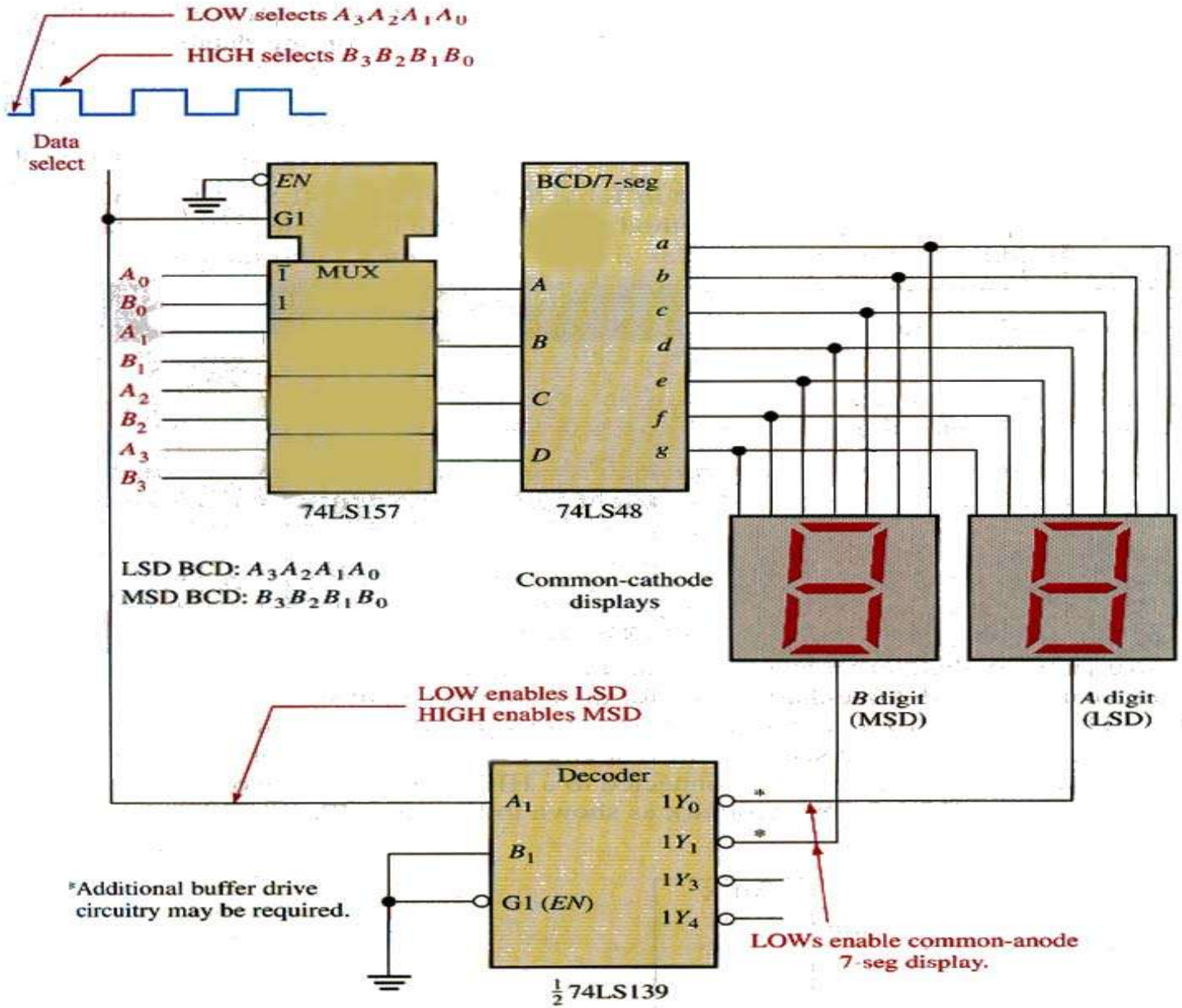
- Expanded multiplexers



Application Examples- *A 7-segment Display Multiplexer:-*

Figure below shows a simplified method of multiplexing BCD numbers to a 7-segment display. Two digit numbers are displayed on the 7-segment readout by the use of a single BCD-to-7-segment decoder. The basic operation is as follows:

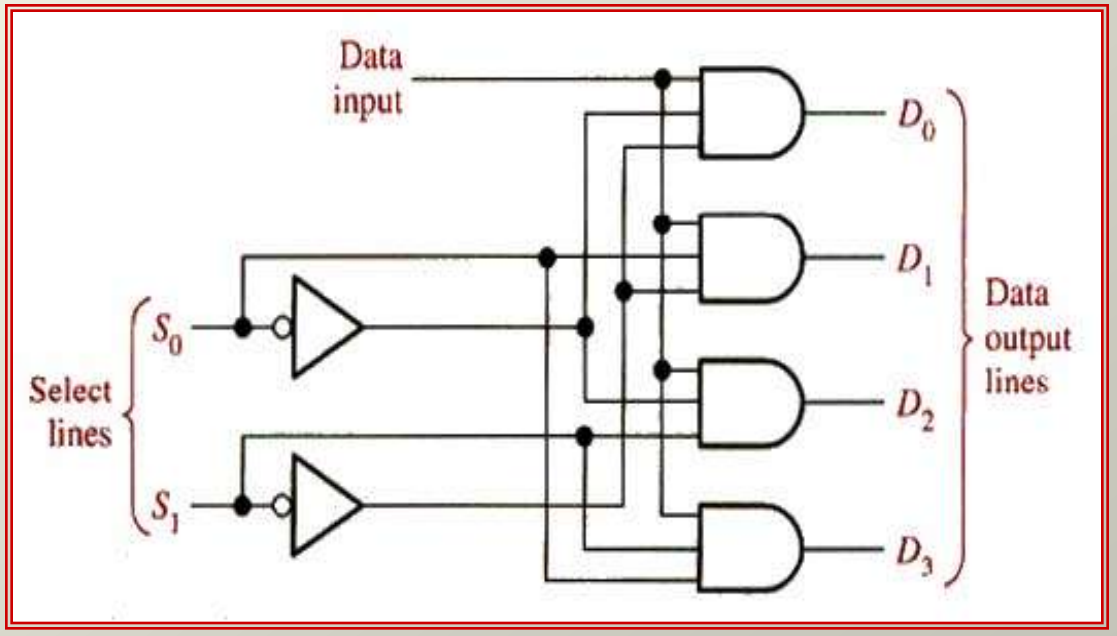
Two BCD digits ($A_3A_2A_1A_0$ and $B_3B_2B_1B_0$) are applied to the multiplexer inputs. A square wave is applied to the data-select line, and when it is LOW, the A bits ($A_3A_2A_1A_0$) are passed through to the inputs of the 74LS48 BCD-to-7-segment decoder. The LOW on the data select also puts a LOW on the A_1 input of the 74LS139 2line-to-4-line decoder. Thus activating its 0 output and enabling the A-digit display by effectively connecting its common terminal to ground. The A digit is now on and the B digit is off. When the data-select line goes HIGH, the B bits ($B_3B_2B_1B_0$) are passed through to the inputs of the BCD-to-7-segment decoder. Also the 74LS139 decoder's 1 output is activated thus enabling the B-digit display. The B digit is now on and the A digit is off.


LOW selects $A_3A_2A_1A_0$
HIGH selects $B_3B_2B_1B_0$
Data select
EN
G1
MUX
A_0
B_0
A_1
B_1
A_2
B_2
A_3
B_3
74LS157
BCD/7-seg
A
B
C
D
a
b
c
d
e
f
g
74LS48
LSD BCD: $A_3A_2A_1A_0$
MSD BCD: $B_3B_2B_1B_0$
Common-cathode displays
LOW enables LSD
HIGH enables MSD
B digit (MSD)
A digit (LSD)
Decoder
A_1
B_1
G1 (EN)
$1Y_0$
$1Y_1$
$1Y_3$
$1Y_4$
*Additional buffer drive circuitry may be required.
LOWs enable common-anode 7-seg display.
$\frac{1}{2}$ 74LS139

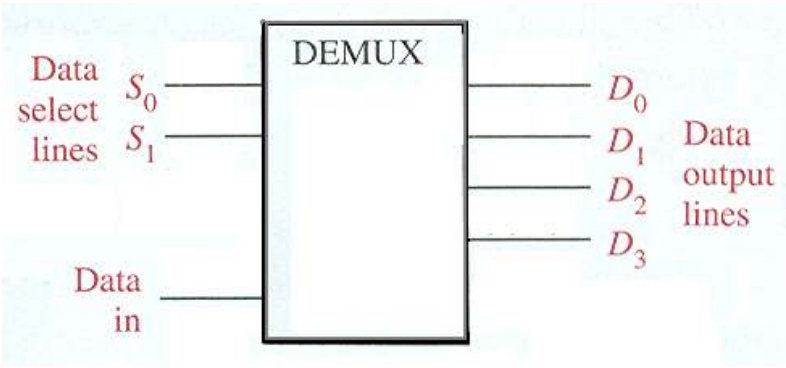
9. Demultiplexers

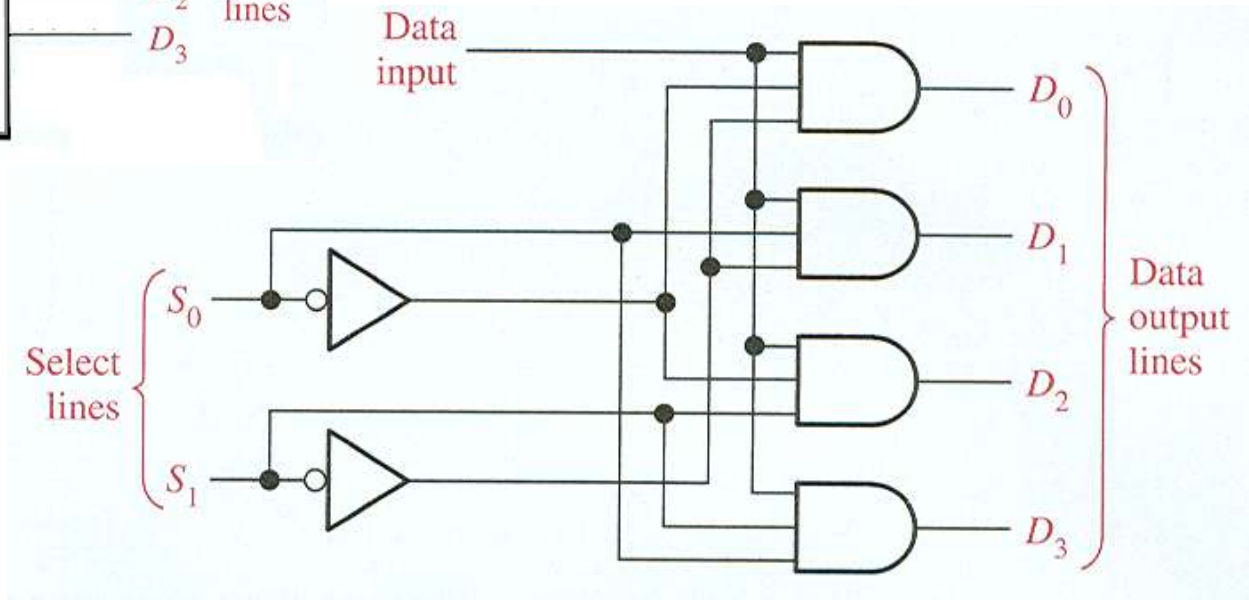
A demultiplexer (DEMUX) performs the opposite function from a MUX. It switches data from one input line to two or more data lines depending on the select inputs.

1-line-to-4-line demultiplexer circuit is shown in the figure. The two data-select lines enable only one gate at a time, and the data appearing on the data-input line will pass through the selected gate to the associated data output line.



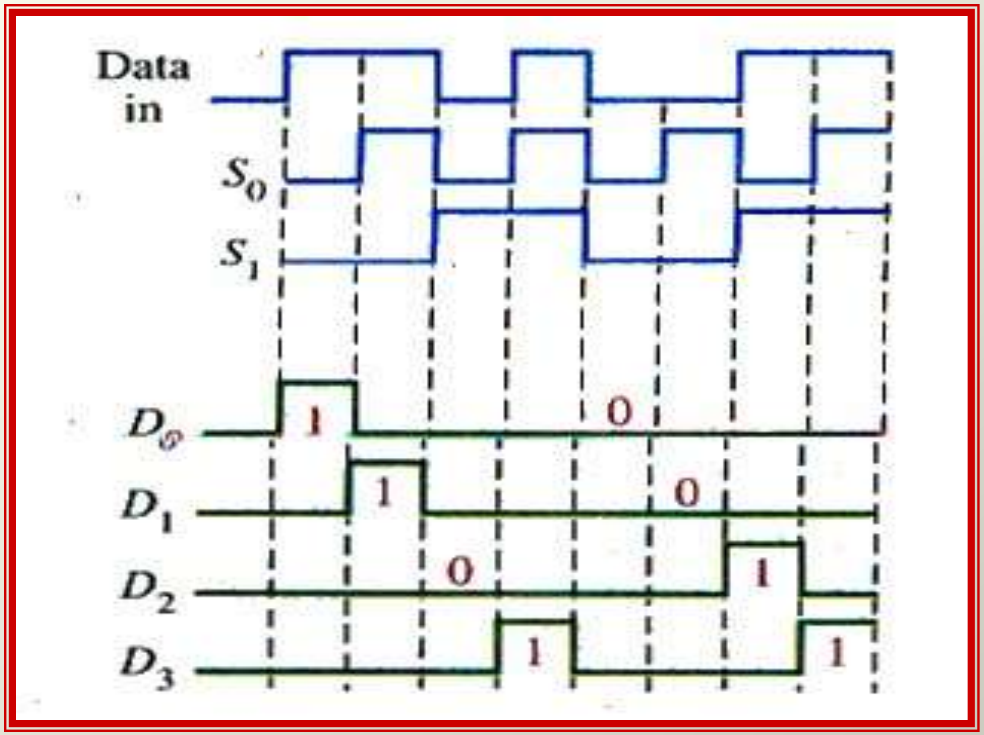
DATA-SELECT INPUTS S_1	S_0	OUTPUT SELECTED
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3





Example :- The serial data-input waveform (data in) and data-select inputs (S_0 and S_1) are shown. Determine the data-output waveforms on D_0 through D_3 for the demultiplexer.

Solution:-



The select lines go through a binary sequence so that each successive input bit is routed to D_0, D_1, D_2 and D_3 in sequence as shown by the output waveforms in figure above.

10. Parity Generators/Checkers

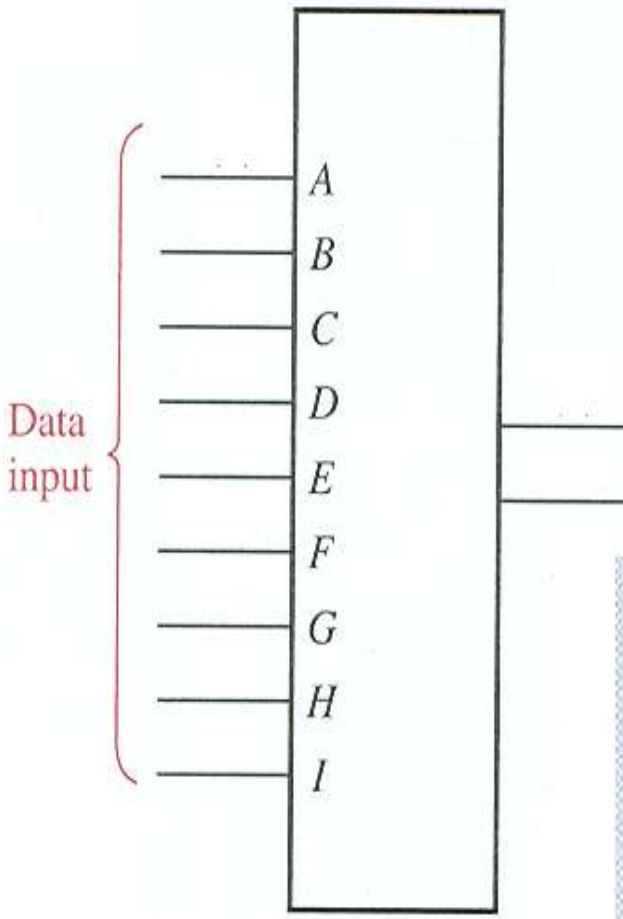
Errors can occur as digital codes are being transferred from one point to another within a digital system or while codes are being transmitted from one system to another. The errors take the form of undesired change in the bits that make up the coded information; that is , a 1 can change to a 0, or a 0 to a 1, because of component malfunctions or electronic noise.

Parity is an error detection method that uses an extra bit appended to a group of bits to force them to be either odd or even. In even parity, the total number of ones is even; in odd parity the total number of ones is odd.

The ASCII letter S is 1010011. Show the parity bit for the letter S with odd and even parity.

S with odd parity = 11010011

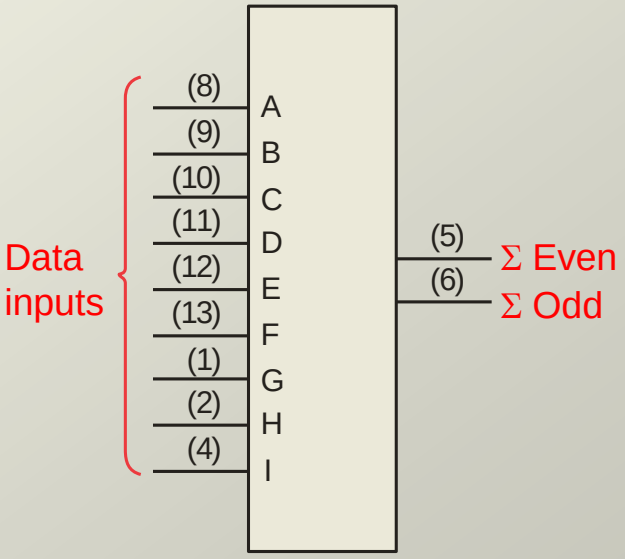
S with even parity = 01010011



Number of Inputs A–I That Are HIGH	Outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

The 74LS280 can be used to generate a parity bit or to check an incoming data stream for even or odd parity.

Checker: The 74LS280 can test codes with up to 9 bits. The even output will normally be HIGH if the data lines have even parity; otherwise it will be LOW. Likewise, the odd output will normally be HIGH if the data lines have odd parity; otherwise it will be LOW.



Generator: To generate <u>even</u> parity, the parity bit is taken from the <u>odd</u> parity output. To generate <u>odd</u> parity, the output is taken from the <u>even</u> parity output.

Key Terms

- ***Half Adder***
- ***Full-adder***
- ***Cascading***
- ***Ripple carry***
- ***Look-ahead carry***

- ***Decoder***
- ***Encoder***
- ***Multiplexer (MUX)***
- ***Demultiplexer (DEMUX)***
- ***Parity bit***