Logic Circuits Course

Ch. 8-2

Counters

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Counters

1- Asynchronous Counters
2- Synchronous Counters
3- Up/Down synchronous Counter
4- Design of synchronous Counter
5- Cascaded Counters
6- Counter Decoding
7- Counter Applications
8- Logic Symbols with Dependency Notation

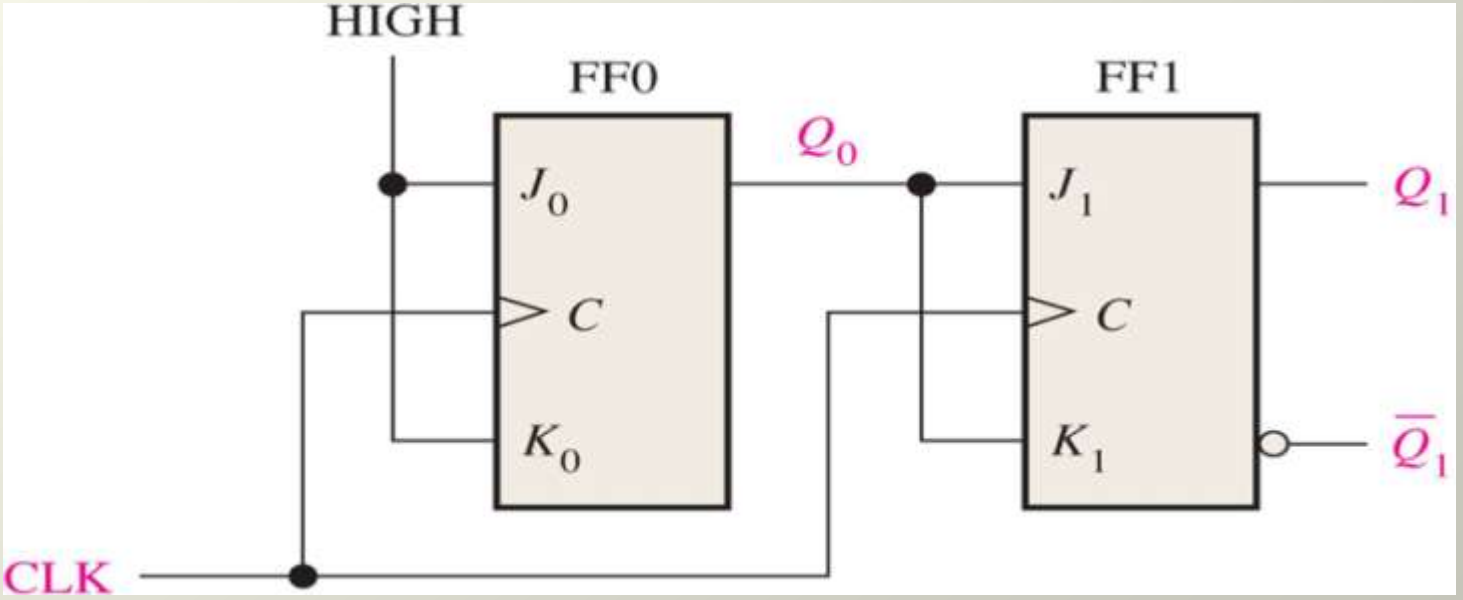
2. Synchronous Counters

- Synchronous binary counter
  - 2-bit asynchronous binary counter
  - 3-bit asynchronous binary counter
  - 4-bit asynchronous binary counter
- Synchronous decade counter

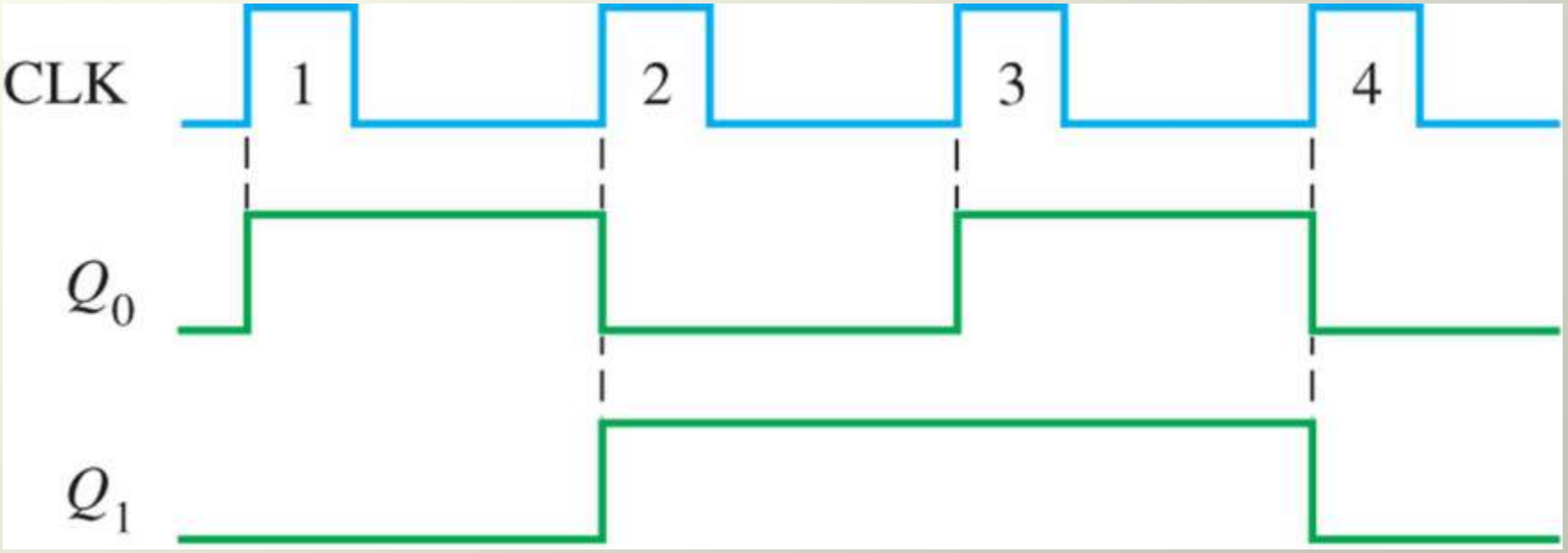
The term **synchronous** refers to events that have a fixed time relationship with each other. With respect to counter operation, synchronous means that all the flip-flops in the counter are clocked at the same time by a common clock pulse.

2-Bit Synchronous Binary Counter

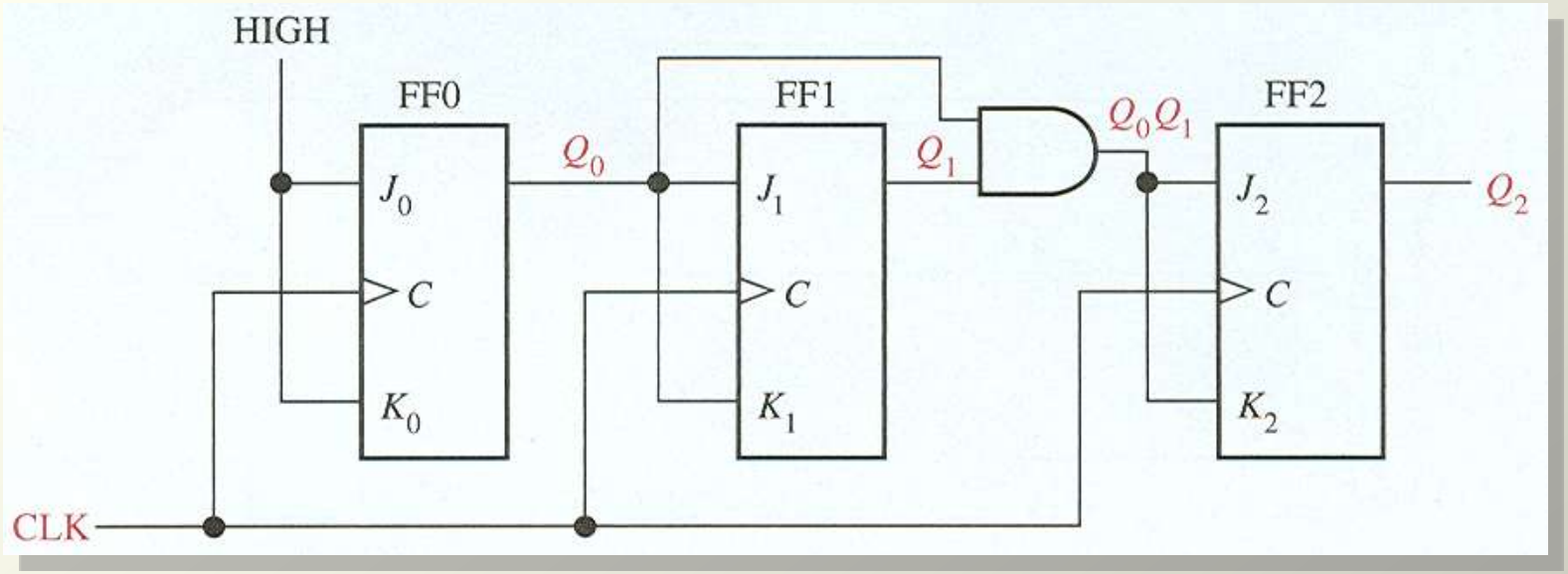
an arrangement difference from that for the asynchronous counter must be used for the J_1 and k_1 inputs of FF1 in order to achieve a binary sequence.

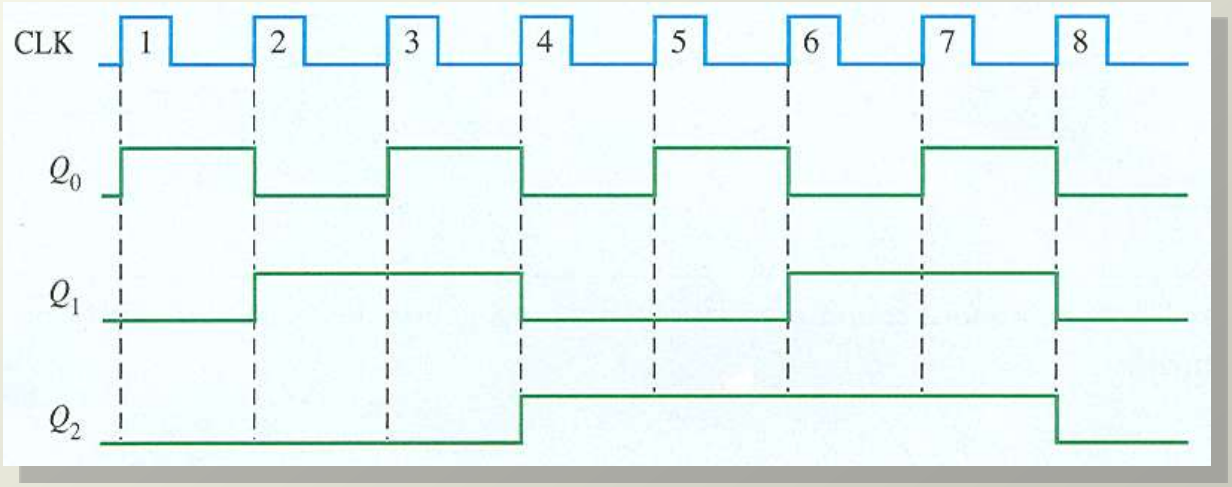


The operation of this synchronous counter is as follows: first, assume that the counter is initially in the binary 0 state; that is, both flip-flops are RESET. When the positive edge of the first clock pulse is applied, FF0 will toggle and Q_0 will therefore go HIGH. Inputs J_1 and K_1 are both LOW because Q_0 to which they are connected, has not yet gone HIGH that mean J=0 and K=0, when the leading edge of the first clock pulse is applied. This is no-change condition, and therefore FF_1 does not change state.



3-Bit Synchronous Binary Counter



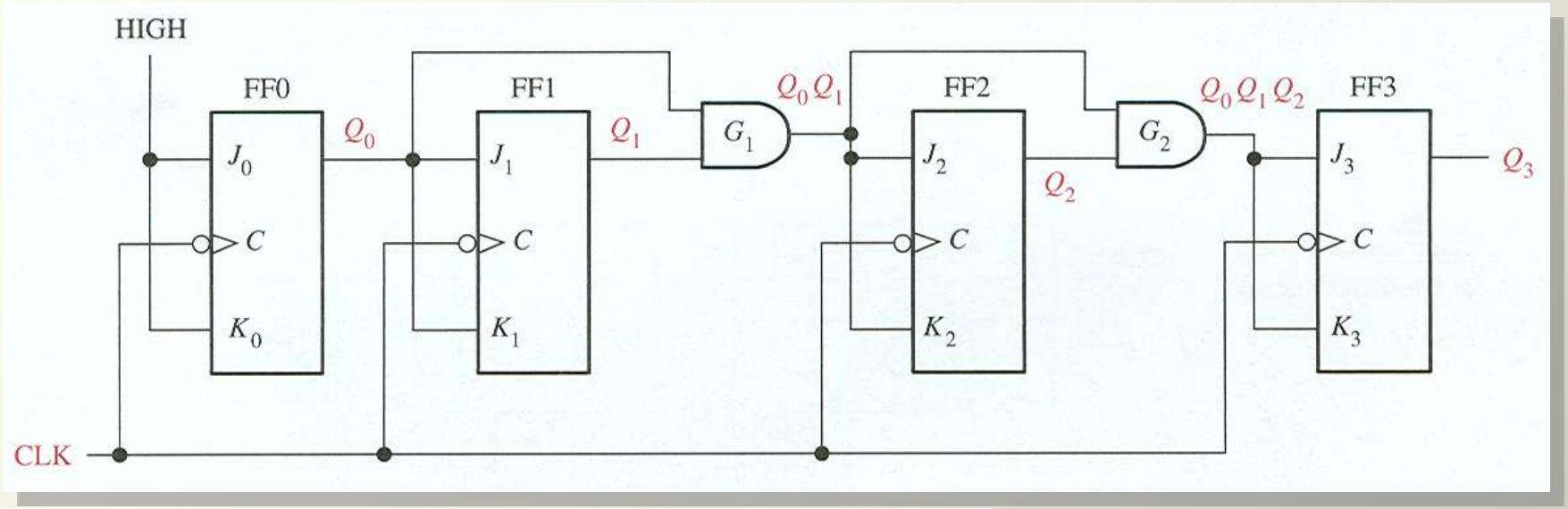


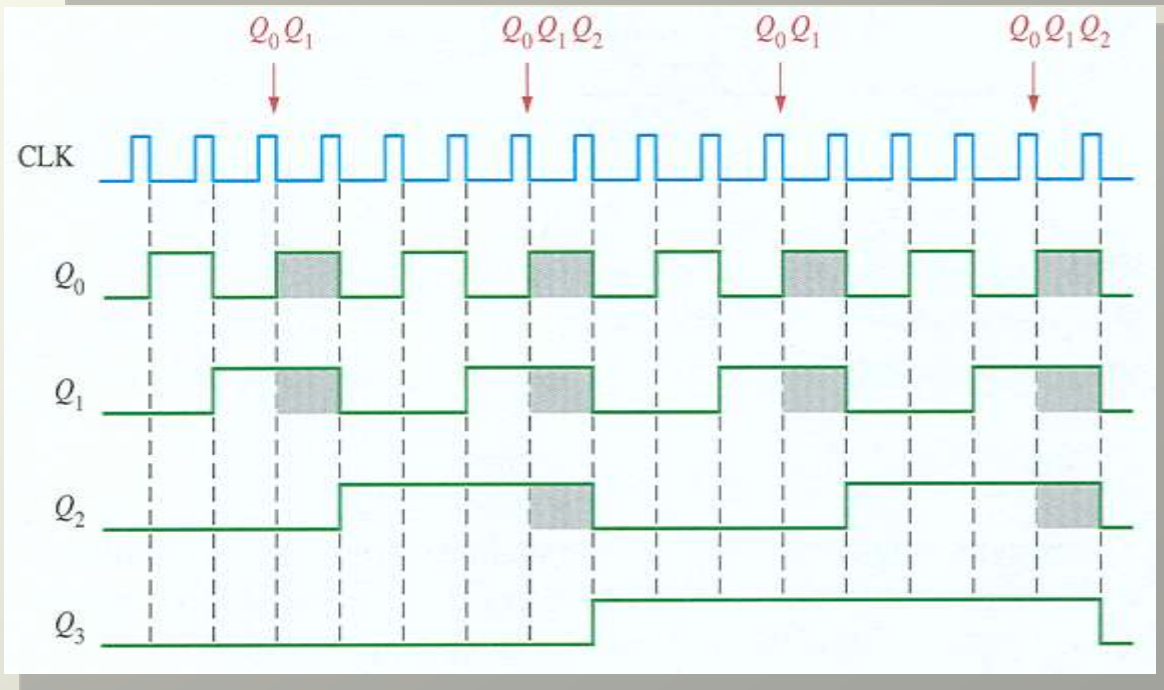
CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

Q_0 changes on each clock pulse as the counter progresses form its original state to its final state and then back to its original state. To produce this operation FF0 must be held in the toggle mode by constant HIGHs on its J_0 and K_0 inputs. Notice that Q_1 goes to the opposite state following each time Q_0 is a 1. this change occurs at CLK2,CLK4, CLK6 and CLK8.

The CLK8 pulse causes the counter to recycle. To produce this operation Q_0 is connected to the J_1 and K_1 inputs of FF1. when Q0 is a 1 and a clock pulse occurs, FF1 is in the toggle mode therefore changes state. The other times, when Q_0 is a 0, FF1 is in the no-change mode and remains in its present state. Both times Q_2 changes state. It is preceded by the unique condition in which both Q_0 and Q_1 are HIGH. This condition is detected by the AND gate and applied to the J_2 and K_2 inputs of FF2. whenever both Q_0 and Q_1 are HIGH, the output of the AND gate makes the J_2 and K_2 inputs of FF2 HIGH, and FF2 toggles on the following clock pulse. At all other times, the J_2 and K_2 inputs of FF2 are held LOW by the AND gate output, and FF2 does not change state

4-Bit Synchronous Binary Counter

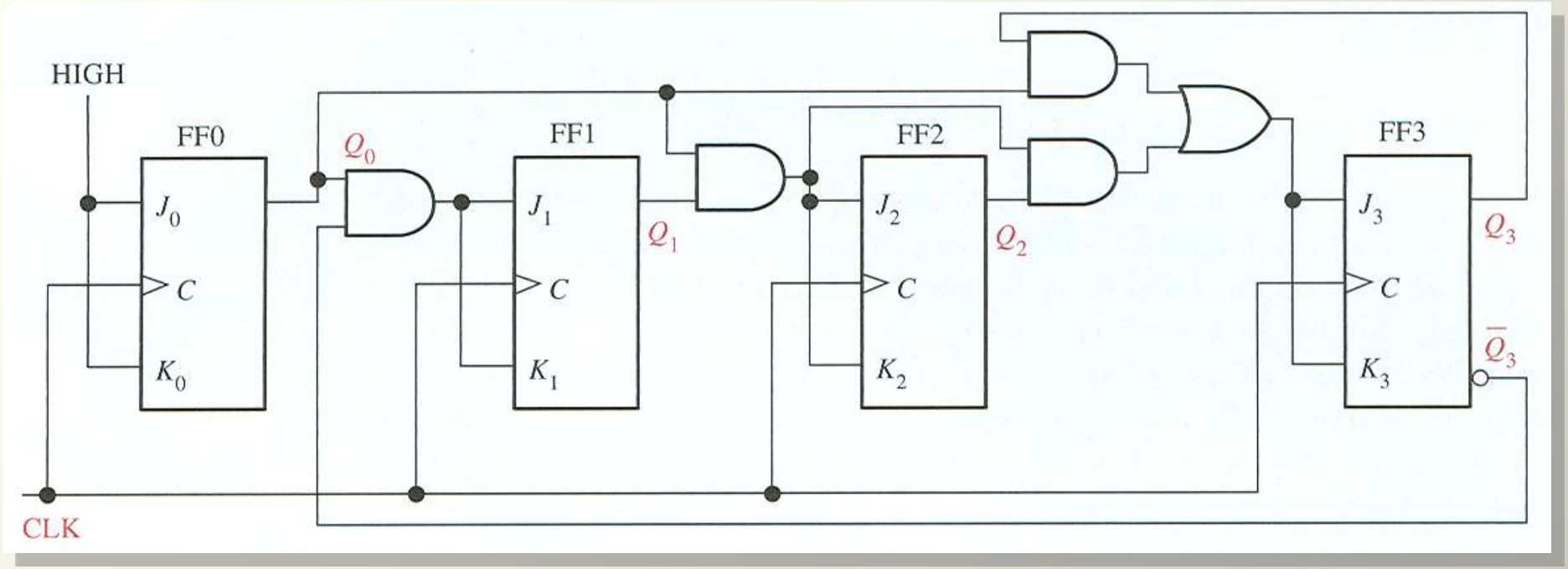


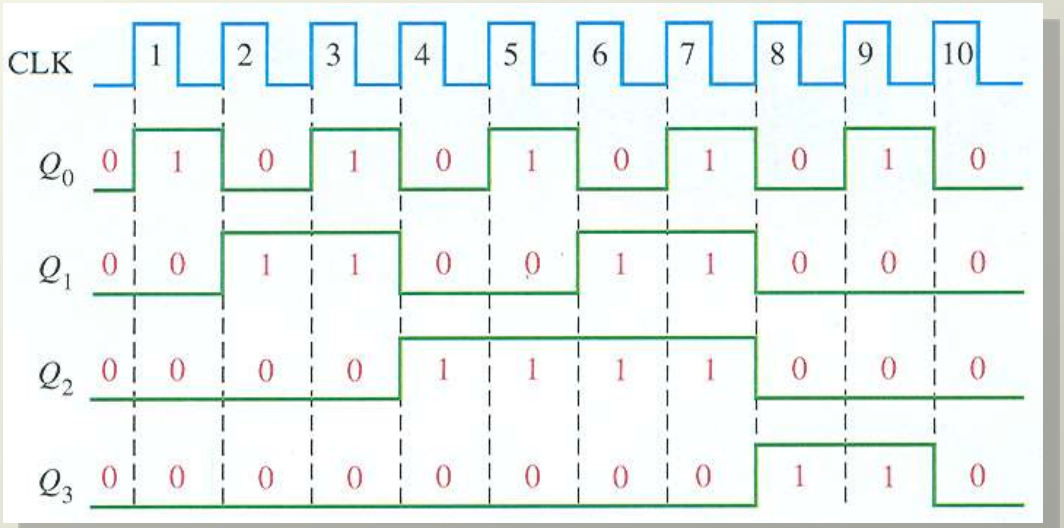


DECIMAL NUMBER	BINARY NUMBER			
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

The process is the same as for the 3-bit counter. The fourth stage FF3, changes only twice in the sequence. Both of these transitions occur following the times that Q_0, Q_1 and Q_2 are all HIGH. This condition is decoded by AND gate G_2 so that when a clock pulse occurs, FF3 will change state. For all other times the J_3 and K_3 inputs of FF3 are LOW, and it is in a no-change condition.

4-Bit Synchronous Decade Counter





CLOCK PULSE	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

BCD decade counter exhibits a truncated binary sequence and goes from 0000 through the 1001 state. Rather than going from the 1001 state to the 1010 state, it recycles to the 0000 state.

You can understand the counter operation by examining the sequence of states in the table above. FF0 (Q_0) toggles on each clock pulse, so the logic equation for its J_0 and K_0 inputs is

$$J0 = K0 = 1$$

this equation is implemented by connecting J_0 and K_0 to a constant HIGH level. In the table FF1 (Q_1) changes on the next clock pulse each time Q_0 =1 and Q_3 = 0, so the logic equation for J_1 and K_1 is

$$J_1 = K_1 = Q_0Q'_3$$

This equation is implemented by ANDing Q_0 and Q'_3 and connecting the gate output to the J_1 and K_1 inputs of FF_1. flip-flop 2 (Q_2) changes on the next clock pulse each time both Q_0 = 1 and Q_1 =1 so

$$J_2 = K_2 = Q_0Q_1$$

This equation is implemented by ANDing Q_0 and Q_1 and connecting the gate output to the J_2 and K_2 inputs of FF_2.

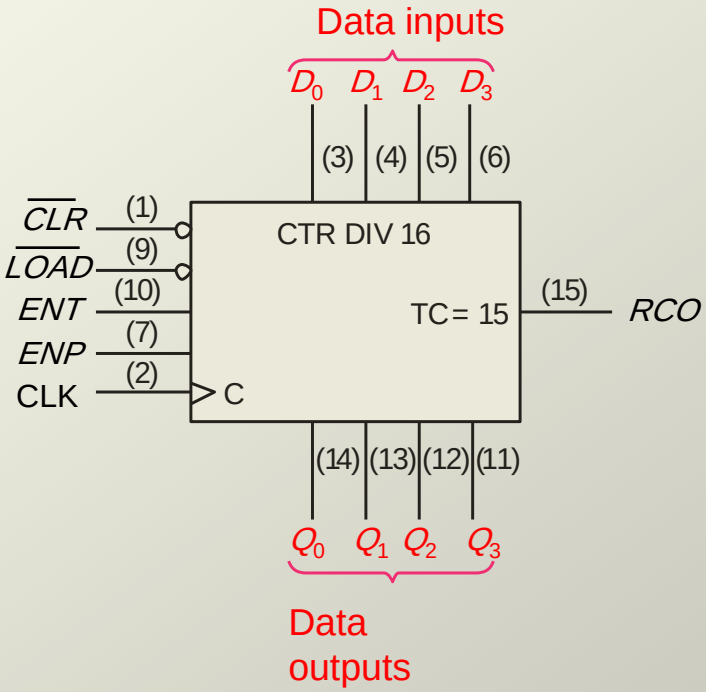
Finally FF_3 (Q_3) changes to the opposite state on the next clock pulse each time $Q_0 = 1$, $Q_1 = 1$ and $Q_2 = 1$ (state 7), or when $Q_0 = 1$ and $Q_3 = 1$ (state 9). This equation for this is s follows

$$J_3 = K_3 = Q_0Q_1Q_3 + Q_0Q_3$$

this function is implemented with the AND/OR logic connected to the J_3 and K_3 inputs of the FF_3.

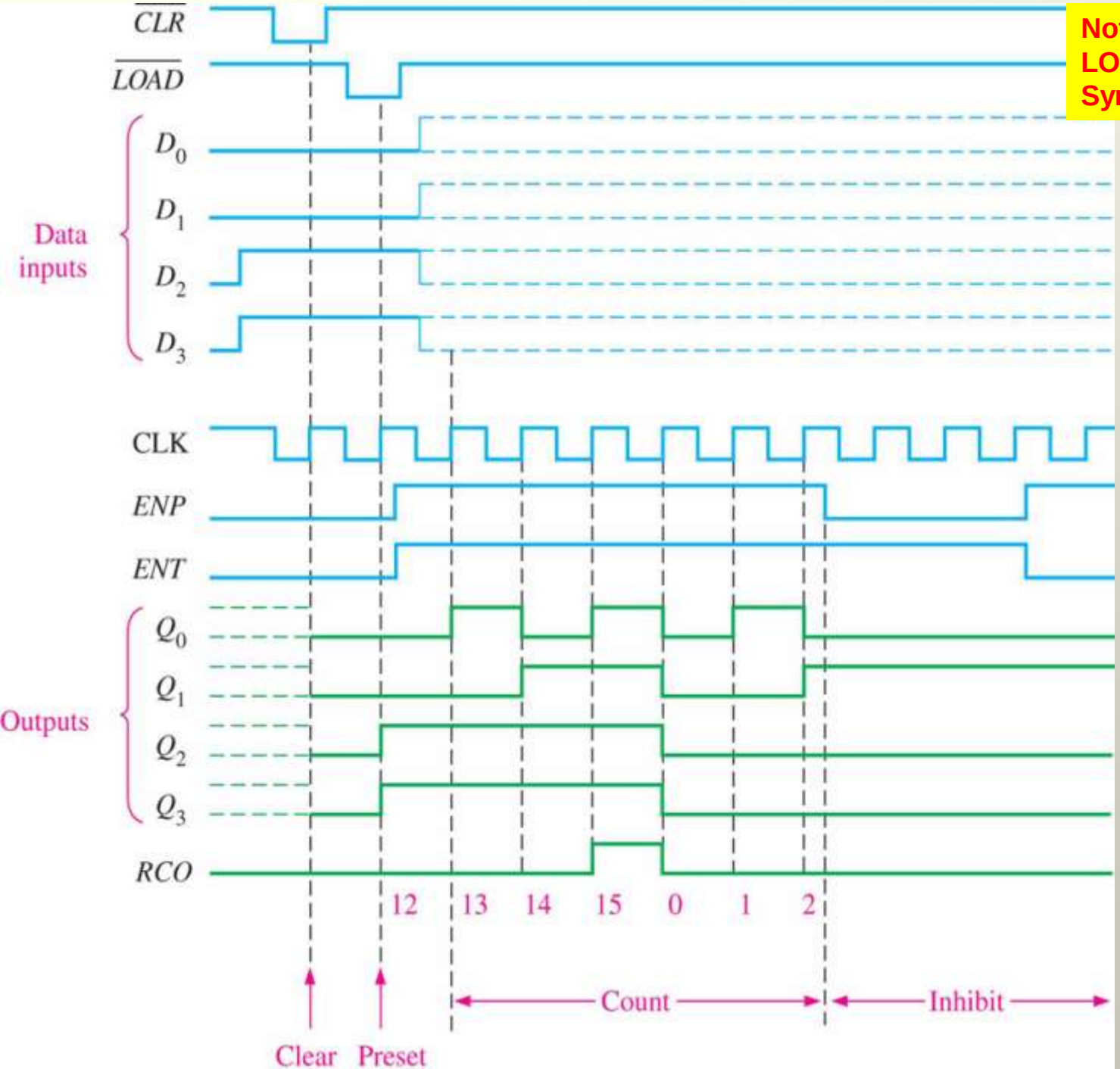
The 74LS163 4-bit Synchronous Binary Counter

The 74LS163 is a 4-bit IC synchronous counter with additional features over a basic counter. It has parallel load, a $\overline{CLR}$ input, two chip enables, and a ripple count output RCO that signals when the count has reached the **terminal count TC**.



Note:
LOAD and CLR are Synchronous with CLK

Example waveforms are on the next slide…

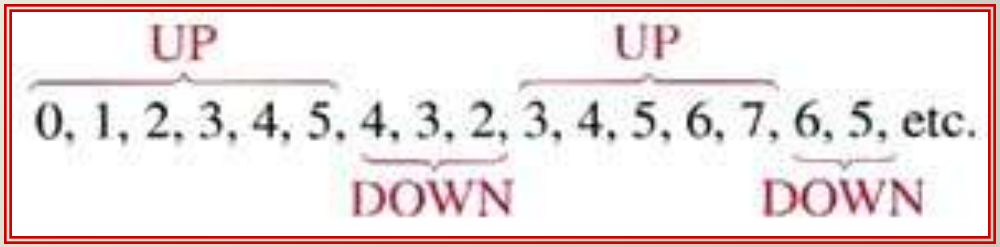


Note:
LOAD and CLR are Synchronous with CLK

3. Up / Down Synchronous Counters

An Up/Down counter is one that is capable of processing in either direction through a certain sequence. An up/down counter sometimes called a bidirectional counter, can have any specific sequence of states. A 3-Bit binary counter that advances upward through its sequence (0,1,2,3,4,5,6,7) and then reversed so that it goes through the sequence in the opposite direction (7,6,5,4,3,2,1,0).

In general, most up/down counters can be reversed at any point in their sequence. For instance the 3-bit binary counter can be made to go through the following sequence:



An examination of Q_0 for both the up and down sequence shows that FF0 toggles on each clock pulse. Thus $J_0 = K_0 = 1$ For FF0

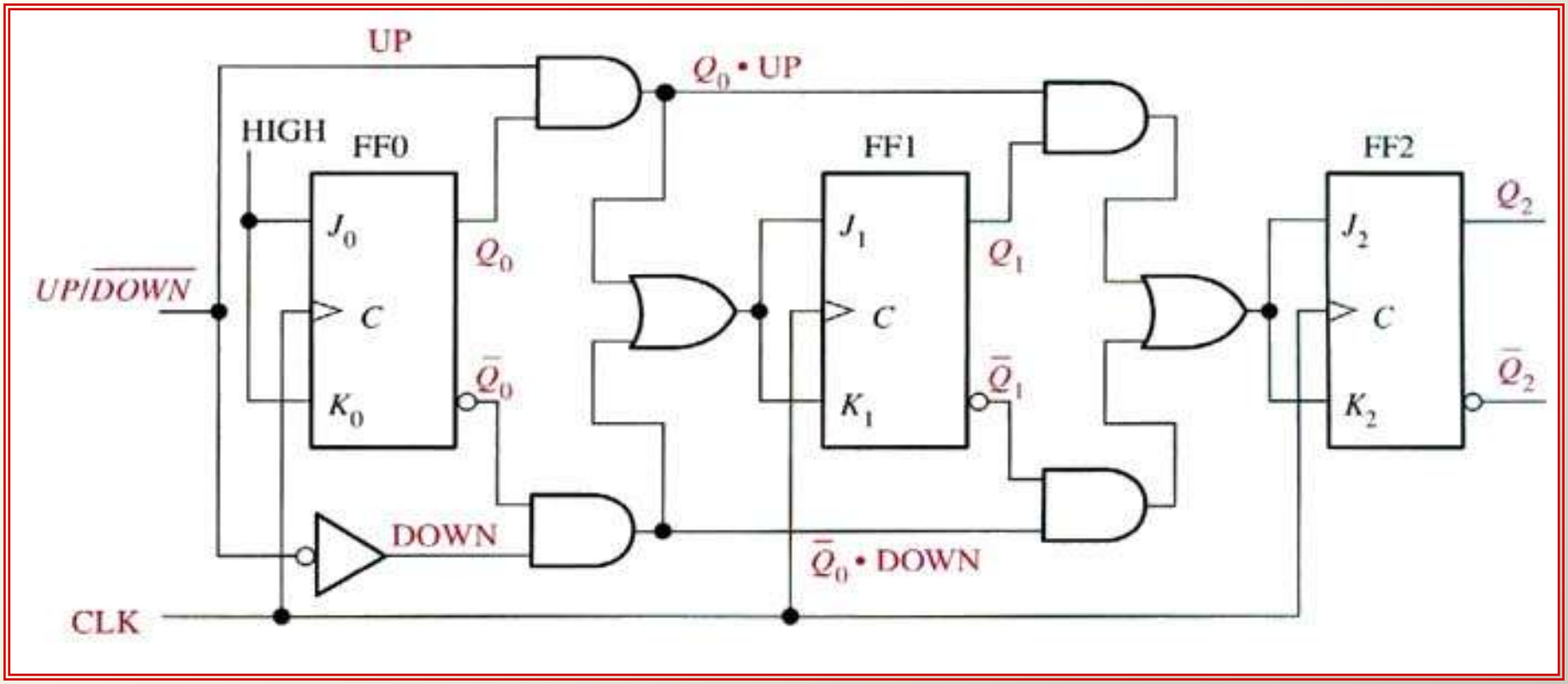
CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

For the up sequence Q_1 changes state on the next clock pulse when $Q_0 = 1$. For the down sequence Q_1 changes on the next clock pulse when $Q_0 = 0$. thus, the J_1 and K_1 inputs of FF1 must equal 1 under the conditions expressed by the following equation:

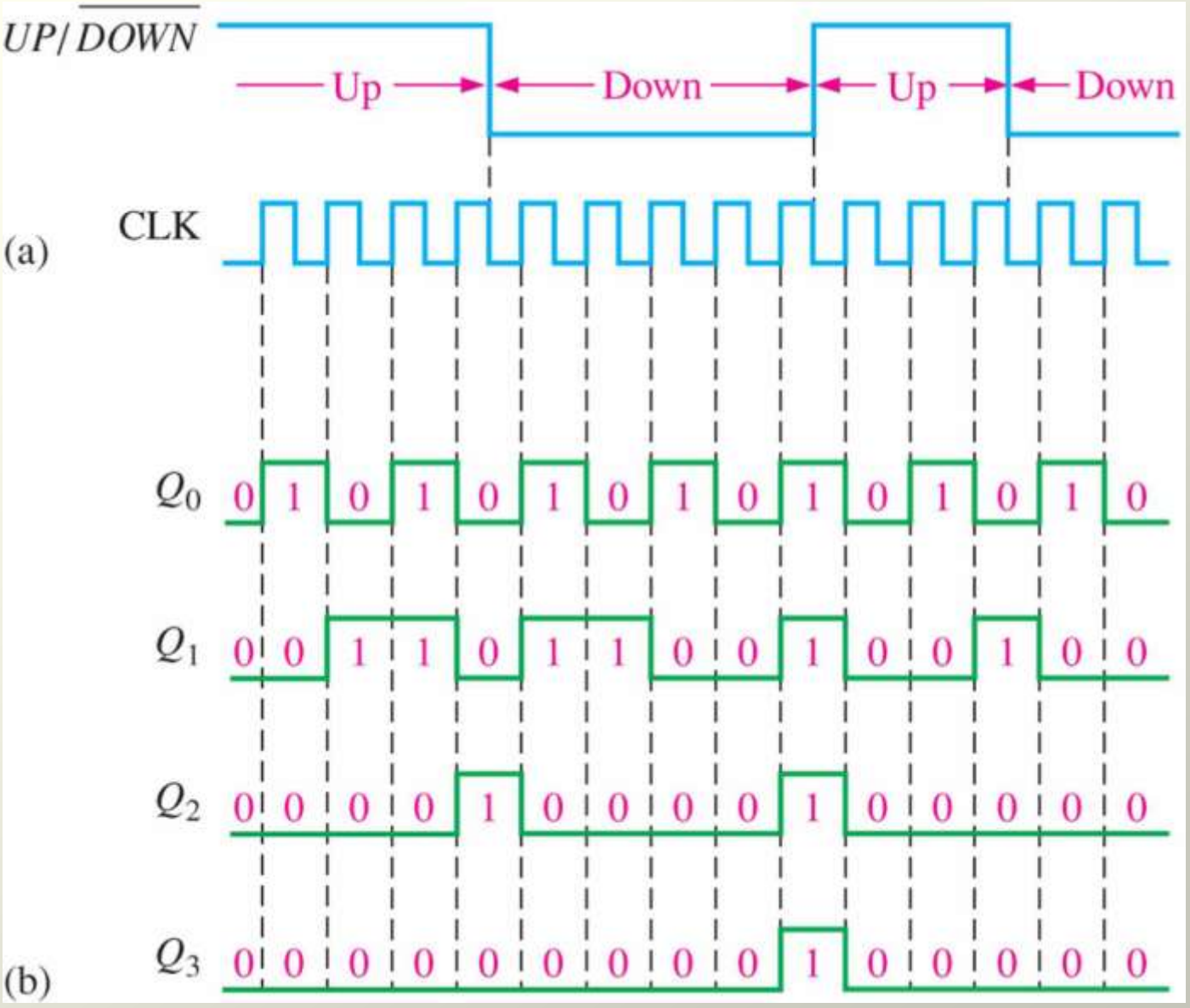
$$J_1 = K_1 = (Q_0 \cdot \text{UP}) + (\overline{Q}_0 \cdot \text{DOWN})$$

For the up sequence Q_2 changes state on the next clock pulse when $Q_0 = Q_1 = 1$. Thus, the J_2 and K_2 inputs of FF2 must equal 1 under the conditions expressed by the following equation:

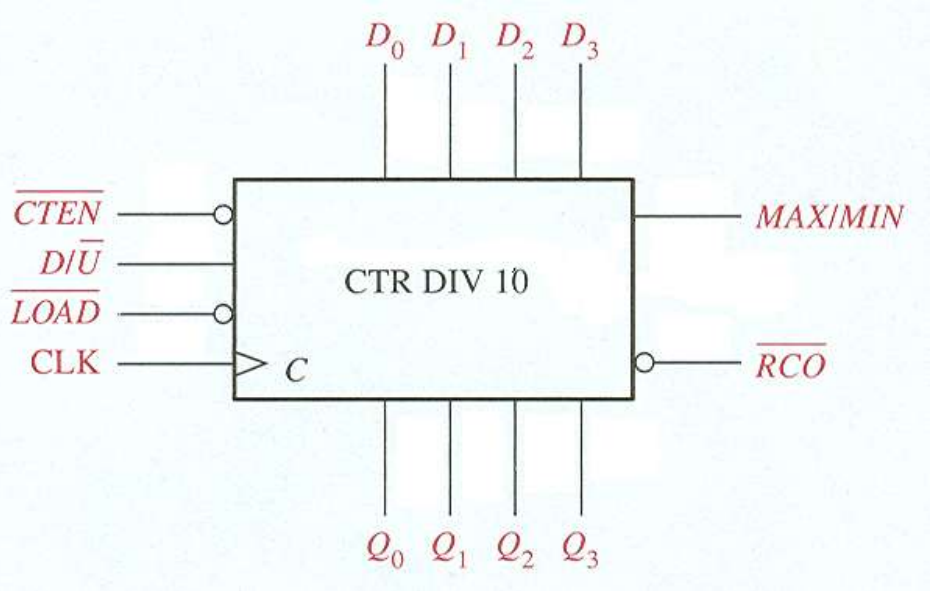
$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \text{UP}) + (\overline{Q}_0 \cdot \overline{Q}_1 \cdot \text{DOWN})$$



Each of the conditions for the J and K inputs of each flip-flop produces a toggle at the appropriate point in the counter sequence. The figure above shows a basic implementation of a 3-bit up/down binary counter. Notice that the control input is HIGH for UP and LOW for DOWN.


UP/DOWN
Up
Down
Up
Down
(a)
CLK
Q_0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Q_1 0 0 1 1 0 1 1 0 0 1 0 0 1 0 0
Q_2 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0
Q_3 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
(b)

Up / Down Synchronous Decade Counter (74HC190)



-The 74HC190 is a high speed CMOS synchronous up/down decade counter with parallel load capability. It also has a active LOW ripple clock output (*RCO*) and a *MAX/MIN* output when the terminal count is reached.

- MAX/MIN output produces a HIGH pulse when the terminal count nine (1001) reaches in the UP mode or (0000) in the DOWN mode.
-Count enable input CTEN .
- CTEN, RCO, MAX/MIN are used when cascading counters.

Up / Down Synchronous Decade Counter (74HC190)