Logic Circuits Course

Ch. 8-3

Counters

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Counters

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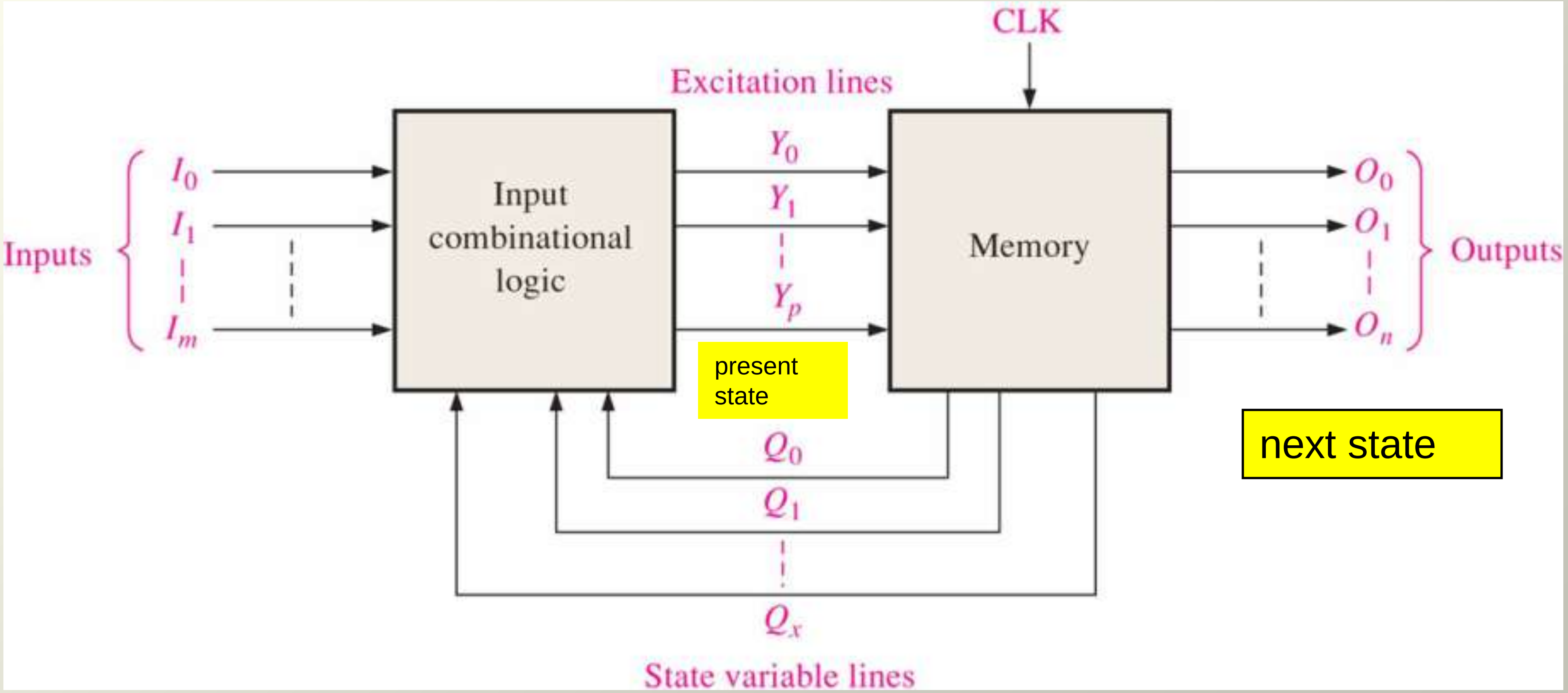
4. Design of Synchronous Counters

General Model of a Sequential Circuit or State machine

A general Sequential circuit consists of a combinational logic section (not always) and a memory section (flip-flops). In clocked sequential circuit, there is a clock input to the memory section. At any given time the memory is in a state called the "present state" and will advance to the "next state" on a clock pulse as determine by the conditions on the excitation lines (Y_0, Y_1, Y_2, . . Y_p). Counters are a special case of clocked sequential circuits.



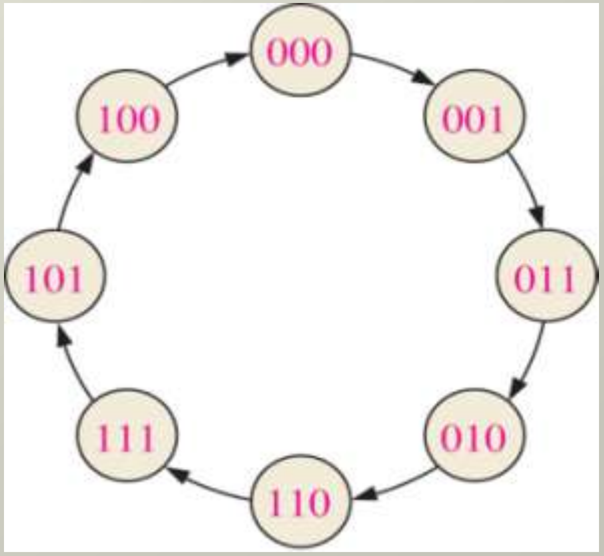
Design of Synchronous Counters

Most requirements for synchronous counters can be met with available ICs. In cases where a special sequence is needed, you can apply a step-by-step design process.

6 steps are used in the design of counters

Step 1 : state Diagram :-A counter is first described by a state diagram which shows the progression of states through which the counter advances when it is clocked.

State diagram for a 3-bit Gray code counter



Step 2 : Next-state Table:- The next state is the state that the counter goes to from its present state upon application of a clock pulse. The next-state table is derived from the state

Present State Q_2	Q_1	Q_0	Next State Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Step 3 : Flip-flop Transition Table.

OUTPUT TRANSITIONS Q_N		Q_{N+1}	FLIP-FLOP INPUTS J	K
0	$\longrightarrow$	0	0	X
0	$\longrightarrow$	1	1	X
1	$\longrightarrow$	0	X	1
1	$\longrightarrow$	1	X	0

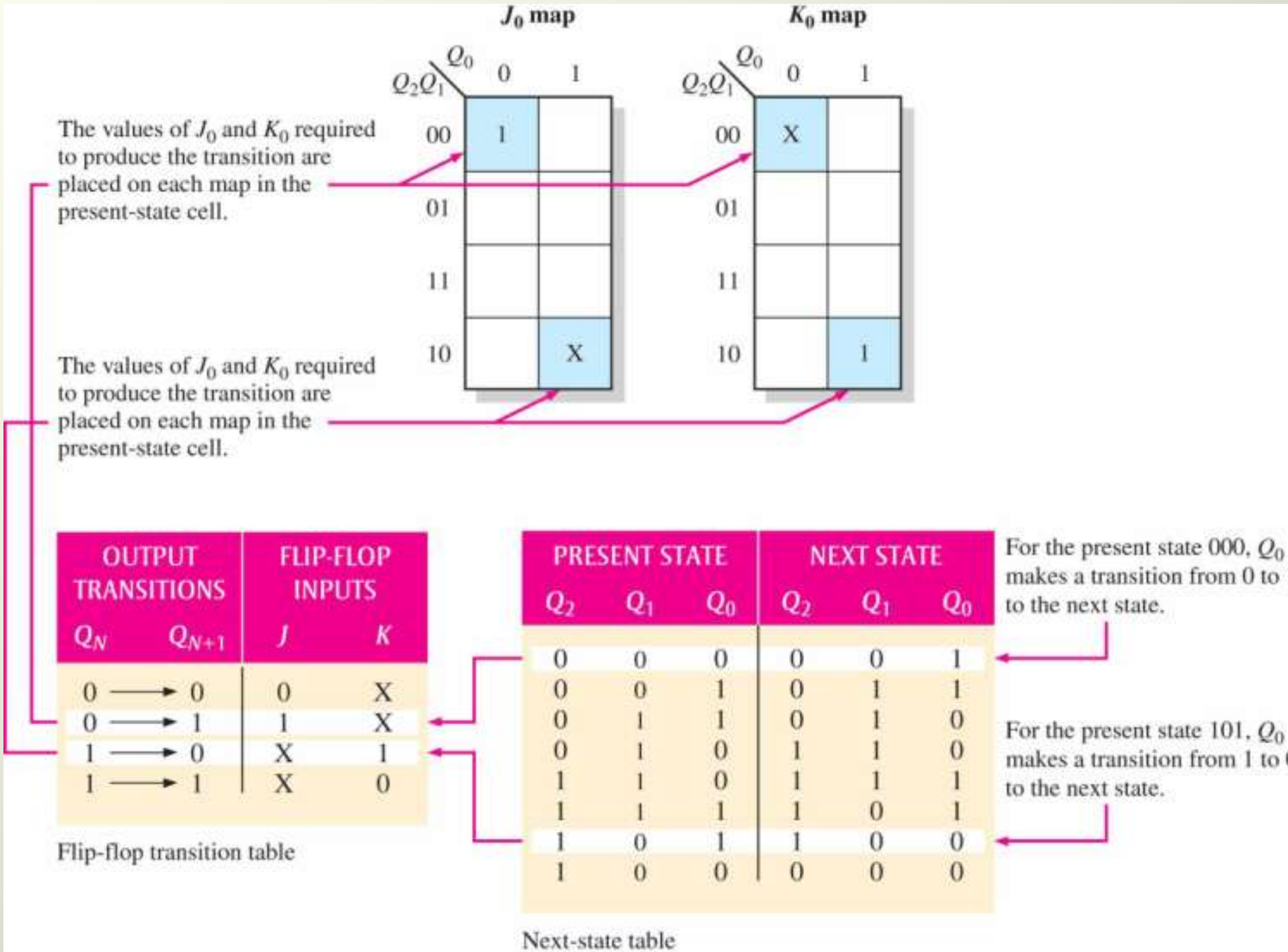
Q_N: present state

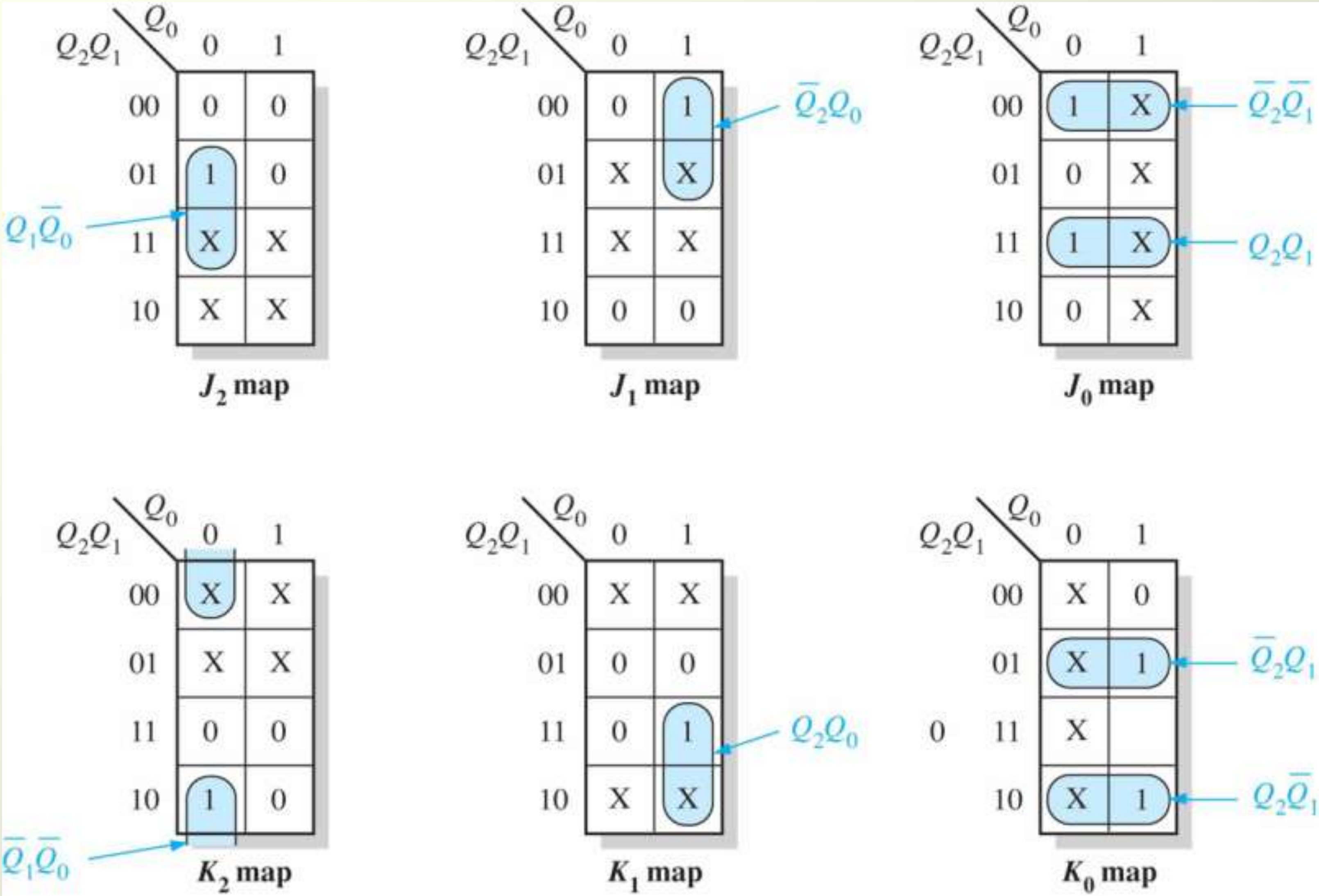
Q_{N+1}: next state

X: "don't care"

The J-K transition table lists all combinations of present output (Q_N) and next output (Q_{N+1}) on the left. The inputs that produce that transition are listed on the right.

Step 4 : Karnaugh Maps:- this can be used to determine the logic required for the J and K inputs of each flip-flop in the counter. There is a Karnaugh map for the J input and another one for the K input of each flip-flop




$Q_2Q_1 \backslash Q_0$
$Q_1\overline{Q}_0$
J_2 map
$\overline{Q}_2Q_0$
J_1 map
$\overline{Q}_2\overline{Q}_1$
Q_2Q_1
J_0 map
$\overline{Q}_1\overline{Q}_0$
K_2 map
Q_2Q_0
K_1 map
$\overline{Q}_2Q_1$
$Q_2\overline{Q}_1$
K_0 map

Step 5 : Logic Expression for Flip-flop inputs:- from the karnaugh map you obtain the following expression for the J and K inputs of each flip-flop.

$$J_0 = Q_2Q_1 + \overline{Q}_2\overline{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2\overline{Q}_1 + \overline{Q}_2Q_1 = Q_2 \oplus Q_1$$

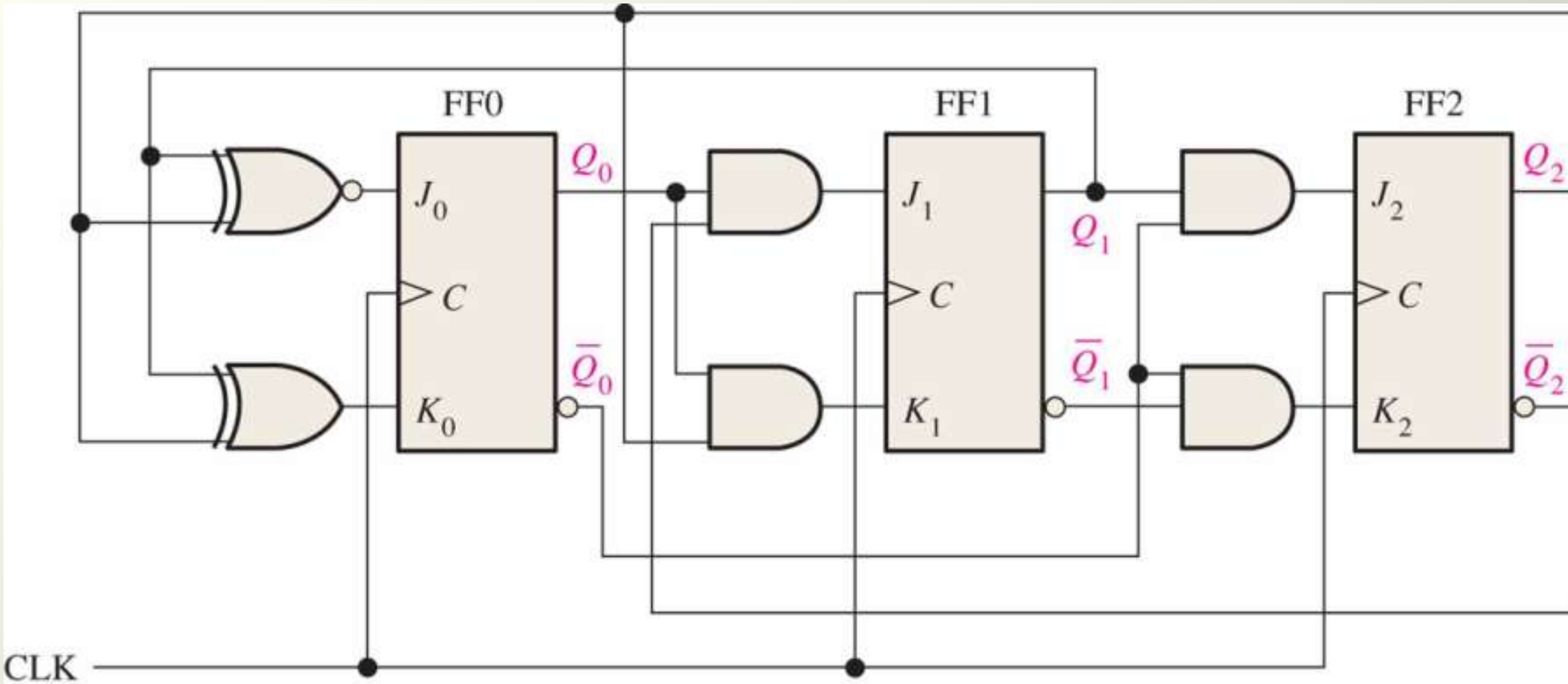
$$J_1 = \overline{Q}_2Q_0$$

$$K_1 = Q_2Q_0$$

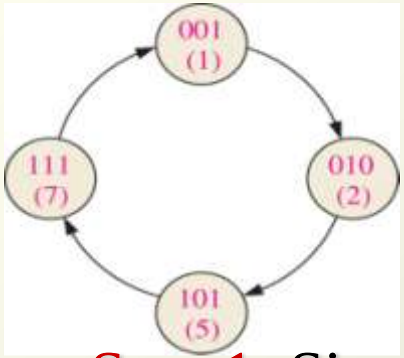
$$J_2 = Q_1\overline{Q}_0$$

$$K_2 = \overline{Q}_1\overline{Q}_0$$

Step 6 : Counter Implementation:- The final step to implement the combinational logic from the expression for the J and k inputs and connect the flip-flops to form the complete 3-bit counter.



Example :- Design a counter with the irregular binary count sequence in the state diagram , use J-K flip-flops



Solution:- Step 1. Since the required sequence does not include all the possible binary states, the invalid states (0,3,4, and 6) can be treated as "Don't cares".

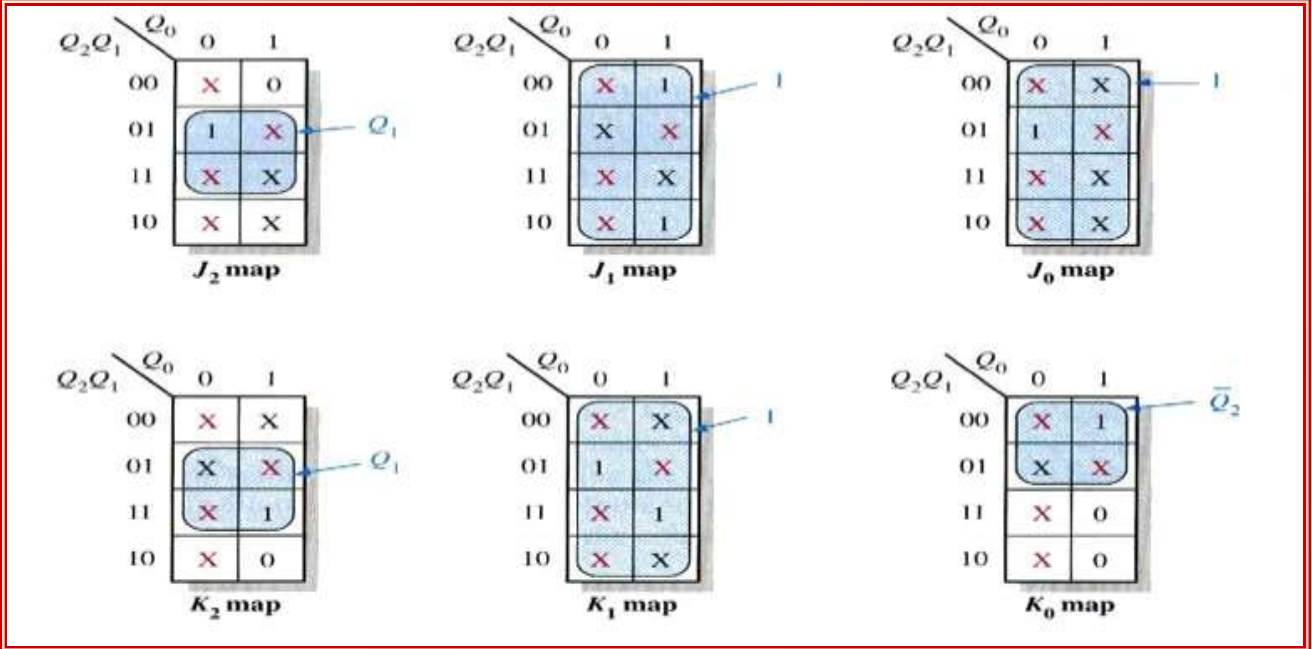
Step 2. The next-state table is developed from the diagram

PRESENT STATE			NEXT STATE		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	1	0	1	0
0	1	0	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1

Step 3. The transition table for the J-K flip-flop is

OUTPUT TRANSITIONS Q_N		Q_{N+1}	FLIP-FLOP INPUTS J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

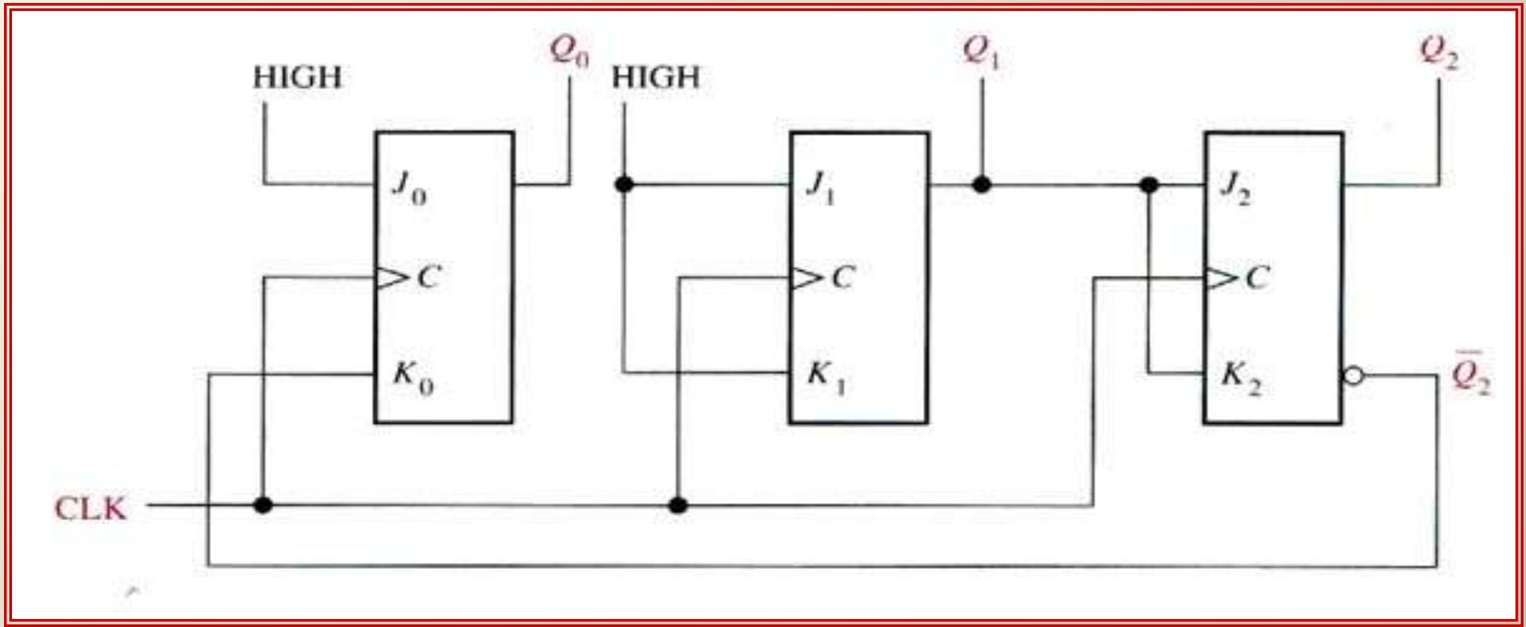
Step 4. The J and K inputs are plotted in the present state karnaugh maps. Also don't cares can be placed in the cells corresponding to the invalid states 000,011,100 and 110 as indicated by the red Xs.



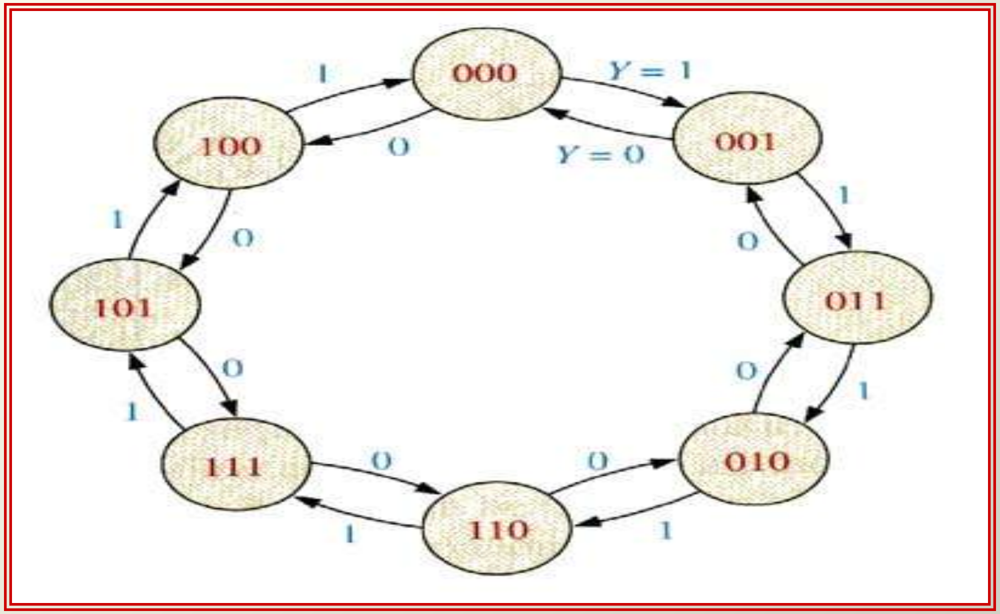
Step 5. Group the 1s, taking advantage of as many of the "Don't care" state as possible for maximum simplification. Notice that when all cells in a map are grouped, the expression is simply equal to 1. the expression for each J and K input taken form the maps as follows:-

$$J_0 = 1, K_0 = \overline{Q}_2$$
$$J_1 = K_1 = 1$$
$$J_2 = K_2 = Q_1$$

Step 6. The implementation of the counter is



Example :- Develop a synchronous 3-bit up/down counter. The counter should count up when an $Up/\overline{DOWN}$ control input is 1 and count down when the control input is 0.



Solution:- Step 1. The 1 or 0 beside each arrow indicates the state of the Up/Down control input Y.

Step 2. The next-state table is developed. Notice that for each present state there are two possible next states, depending on the Up/Down control variable Y.

PRESENT STATE			NEXT STATE Y = 0 (DOWN)			NEXT STATE Y = 1 (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

Y = UP/$\overline{\text{DOWN}}$ control input.

Step 3 :- The transition table for the J-K flip-flops is

OUTPUT TRANSITIONS			FLIP-FLOP INPUTS	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Step 4 :- The karnaugh maps for the J and K inputs of the flip-flop are shown. The $Up/\overline{DOWN}$ control input Y is considered one of the state variables along with Q_0, Q_1 and Q_2 using the next state table.

Q_2Q_1 \ Q_0Y	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	X	X	X	X
10	X	X	X	X

$Q_1\bar{Q}_0Y$

$\bar{Q}_1\bar{Q}_0\bar{Y}$

J_2 map

$\bar{Q}_2Q_0Y$

Q_2Q_1 \ Q_0Y	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	0	1

J_1 map

$Q_2Q_0\bar{Y}$

$\bar{Q}_2\bar{Q}_1Y$

$\bar{Q}_2Q_1\bar{Y}$

Q_2Q_1 \ Q_0Y	00	01	11	10
00	0	1	X	X
01	1	0	X	X
11	0	1	X	X
10	1	0	X	X

Q_2Q_1Y

J_0 map

$Q_2\bar{Q}_1\bar{Y}$

Q_2Q_1 \ Q_0Y	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	0	0	0
10	0	1	0	0

$Q_1\bar{Q}_0\bar{Y}$

K_2 map

$\bar{Q}_1\bar{Q}_0Y$

$\bar{Q}_2Q_0\bar{Y}$

Q_2Q_1 \ Q_0Y	00	01	11	10
00	X	X	X	X
01	0	0	0	1
11	0	0	1	0
10	X	X	X	X

K_1 map

Q_2Q_0Y

$\bar{Q}_2\bar{Q}_1\bar{Y}$

Q_2Q_1 \ Q_0Y	00	01	11	10
00	X	X	0	1
01	X	X	1	0
11	X	X	0	1
10	X	X	1	0

$\bar{Q}_2Q_1Y$

$Q_2Q_1\bar{Y}$

K_0 map

$Q_2\bar{Q}_1Y$

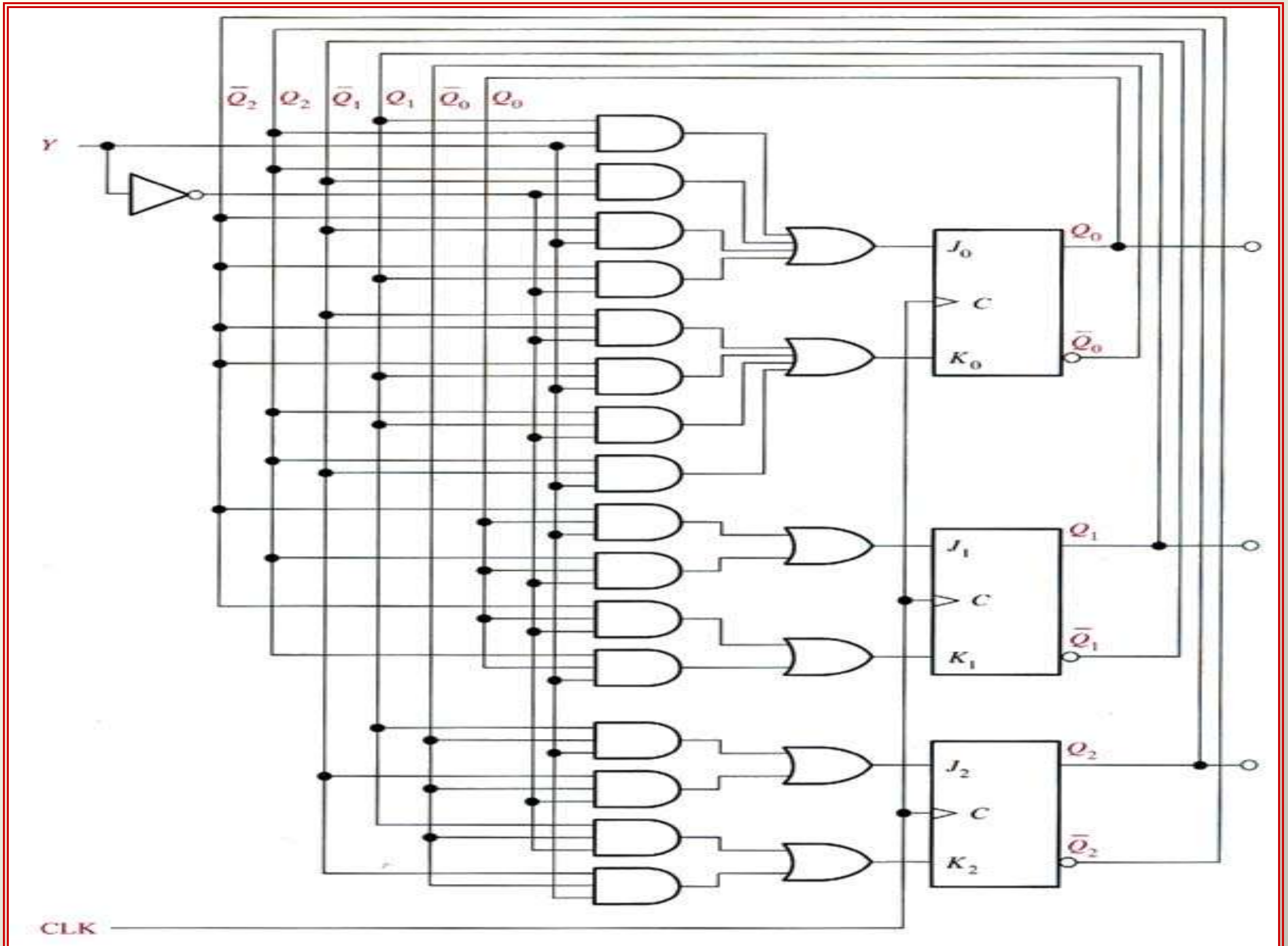
Step 5 : The 1s are combined in the largest possible groupings, with "don't care (Xs) " used where possible. The groups are forced, and the expressions for the J and K inputs are as follows:-

$$J_0 = Q_2Q_1Y + Q_2\overline{Q}_1\overline{Y} + \overline{Q}_2\overline{Q}_1Y + \overline{Q}_2Q_1\overline{Y} \qquad K_0 = \overline{Q}_2\overline{Q}_1\overline{Y} + \overline{Q}_2Q_1Y + Q_2\overline{Q}_1Y + Q_2Q_1\overline{Y}$$

$$J_1 = \overline{Q}_2Q_0Y + Q_2Q_0\overline{Y} \qquad K_1 = \overline{Q}_2Q_0\overline{Y} + Q_2Q_0Y$$

$$J_2 = Q_1\overline{Q}_0Y + \overline{Q}_1\overline{Q}_0\overline{Y} \qquad K_2 = Q_1\overline{Q}_0\overline{Y} + \overline{Q}_1\overline{Q}_0Y$$

Step 6 : The J and K equations are implemented with combinational logic.



$\overline{Q}_2$ Q_2 $\overline{Q}_1$ Q_1 $\overline{Q}_0$ Q_0
Y
J_0
C
K_0
Q_0
$\overline{Q}_0$
J_1
C
K_1
Q_1
$\overline{Q}_1$
J_2
C
K_2
Q_2
$\overline{Q}_2$
CLK