Logic Circuits Course

Ch. 9-1

Shift Registers

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Shift Registers

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2- Serial in/serial out shift registers
3- Serial in/parallel out shift registers
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1. Basic Shift Register Functions

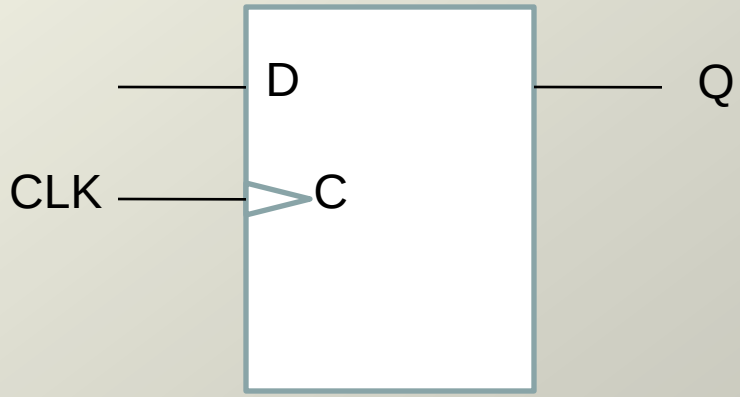
A shift register (sequential circuit) is an arrangement of flip-flops and are important in applications in the storage and movement of data in digital system. SR is solely used for storing and shifting data (1s and 0s) entered into it from an external source and typically do not possess a characteristic internal sequence of states as do counters.

The storage capability of a register makes it an important type of memory device.

The following figure illustrate the concept of storing a 1 or o in

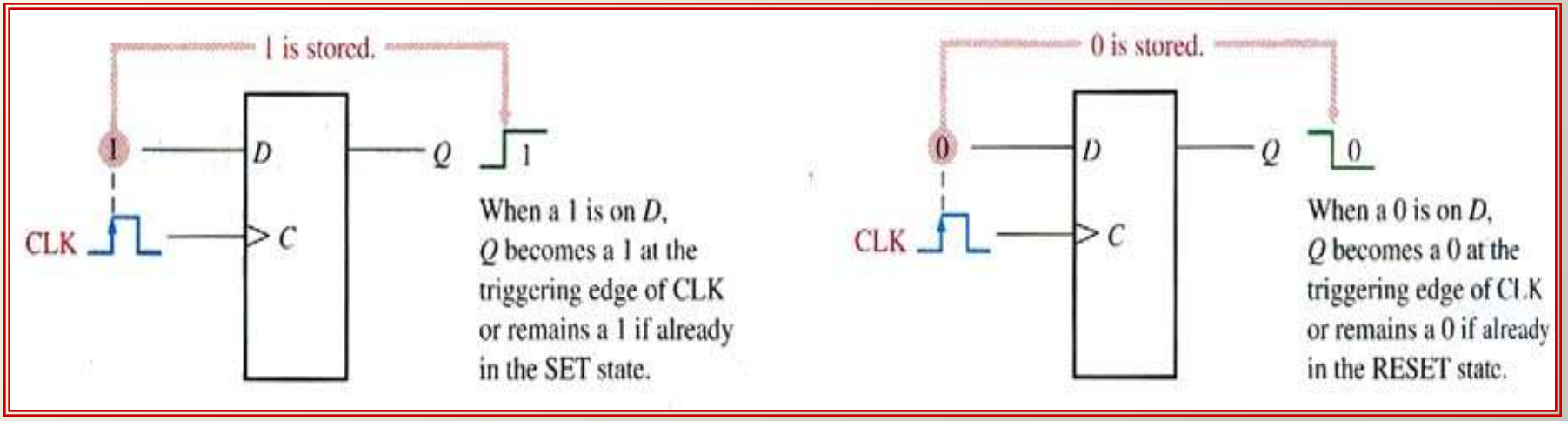
a D flip-flop.

Latch



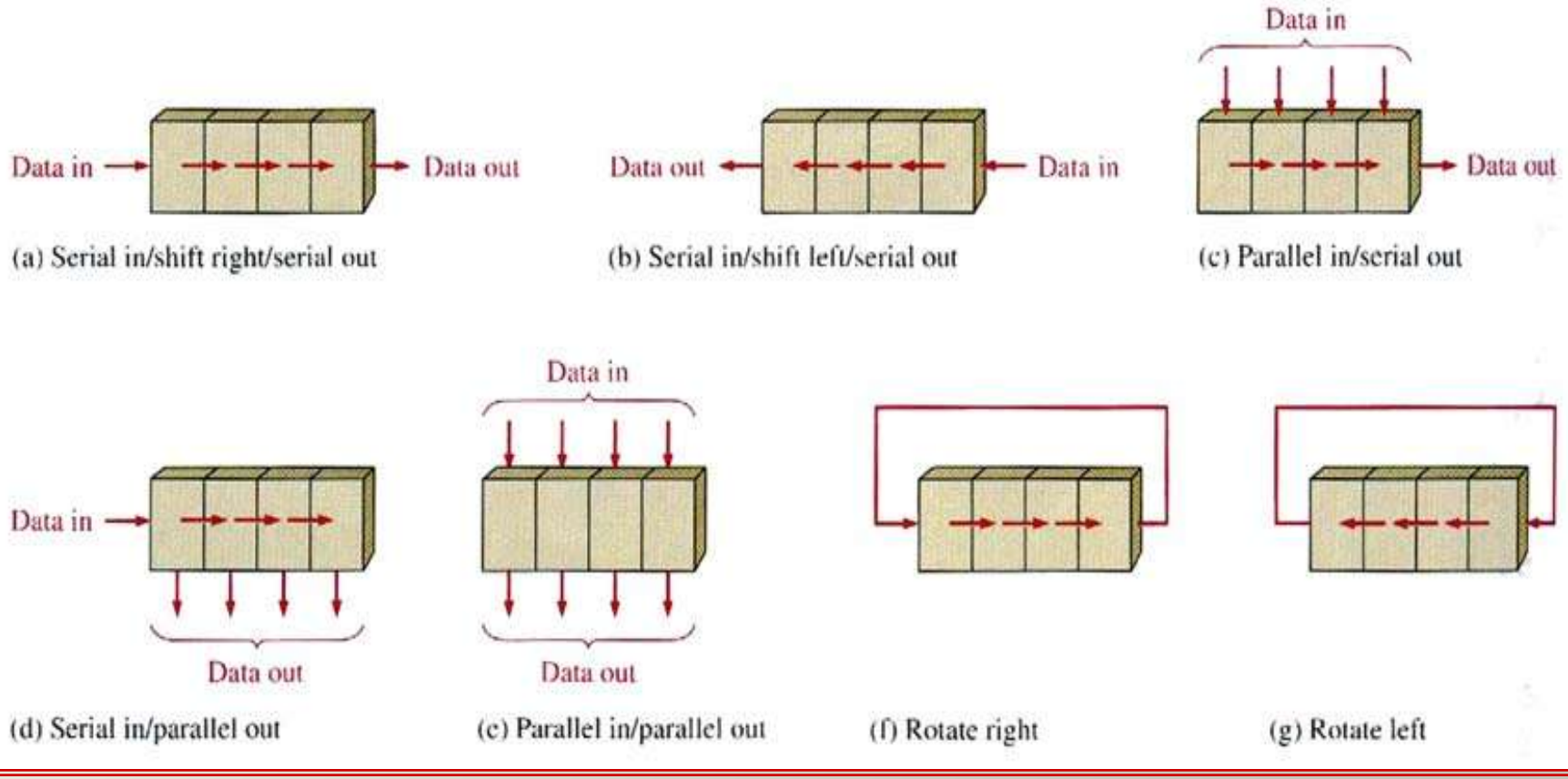
CLK	D	Q
↑	1	1
↑	0	0

A 1 is applied to the data input and a clock pulse is applied that stores the 1 by setting the flip-flop. When the 1 on the input is removed, the flip-flop remains in the SET state, thereby storing 1. A similar procedure applies to the storage of a 0 by resetting the flip-flop.



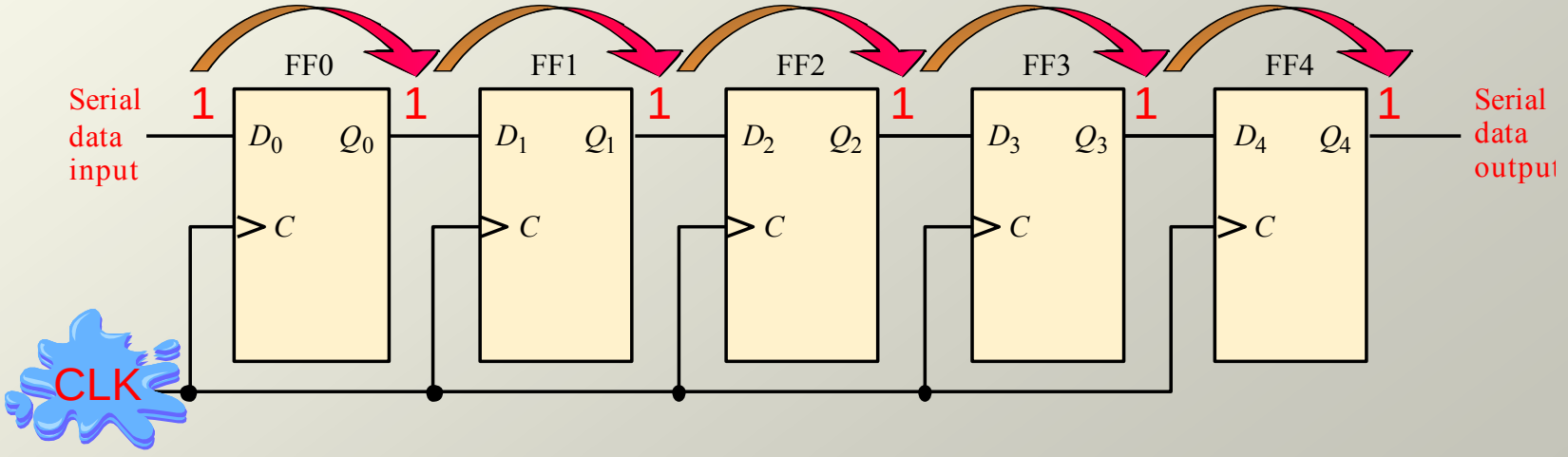
One stage = one filp-flop = one bit of storage capacity

Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)



Shift registers are available in IC form or can be constructed from discrete flip-flops as is shown here with a five-bit serial-in serial-out register.

Each clock pulse will move an input bit to the next flip-flop. For example, a 1 is shown as it moves across.



2. Serial in/Serial Out Shift Registers

The Serial In Serial Out shift registers accepts data serially- that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

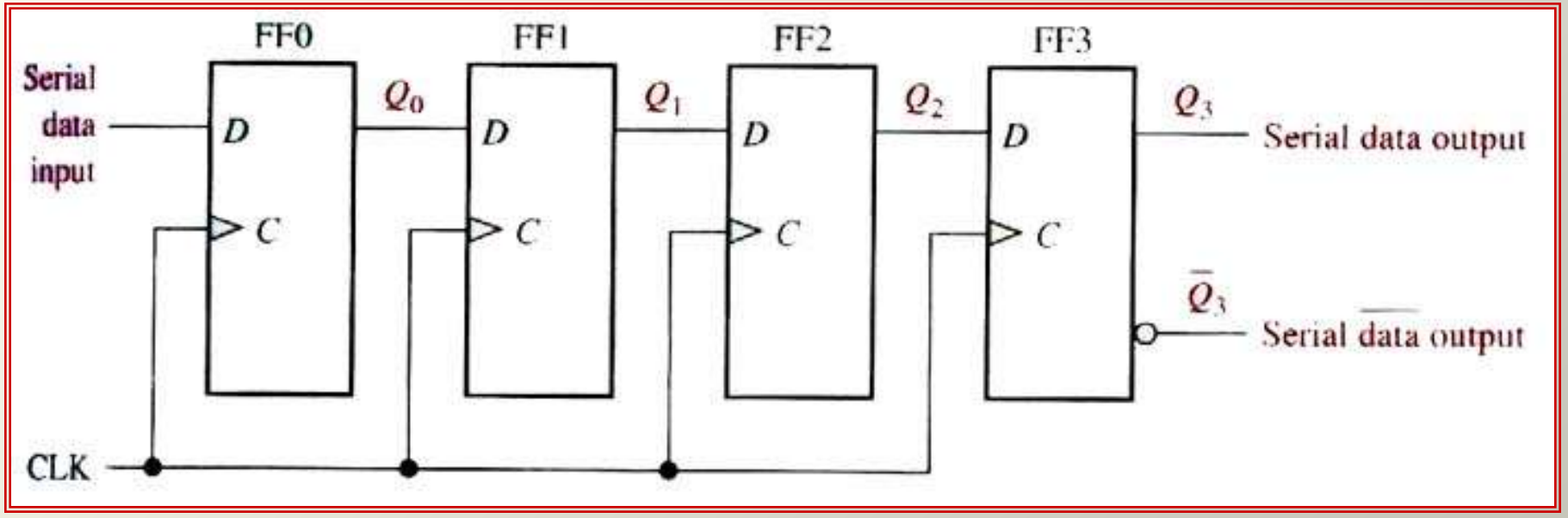


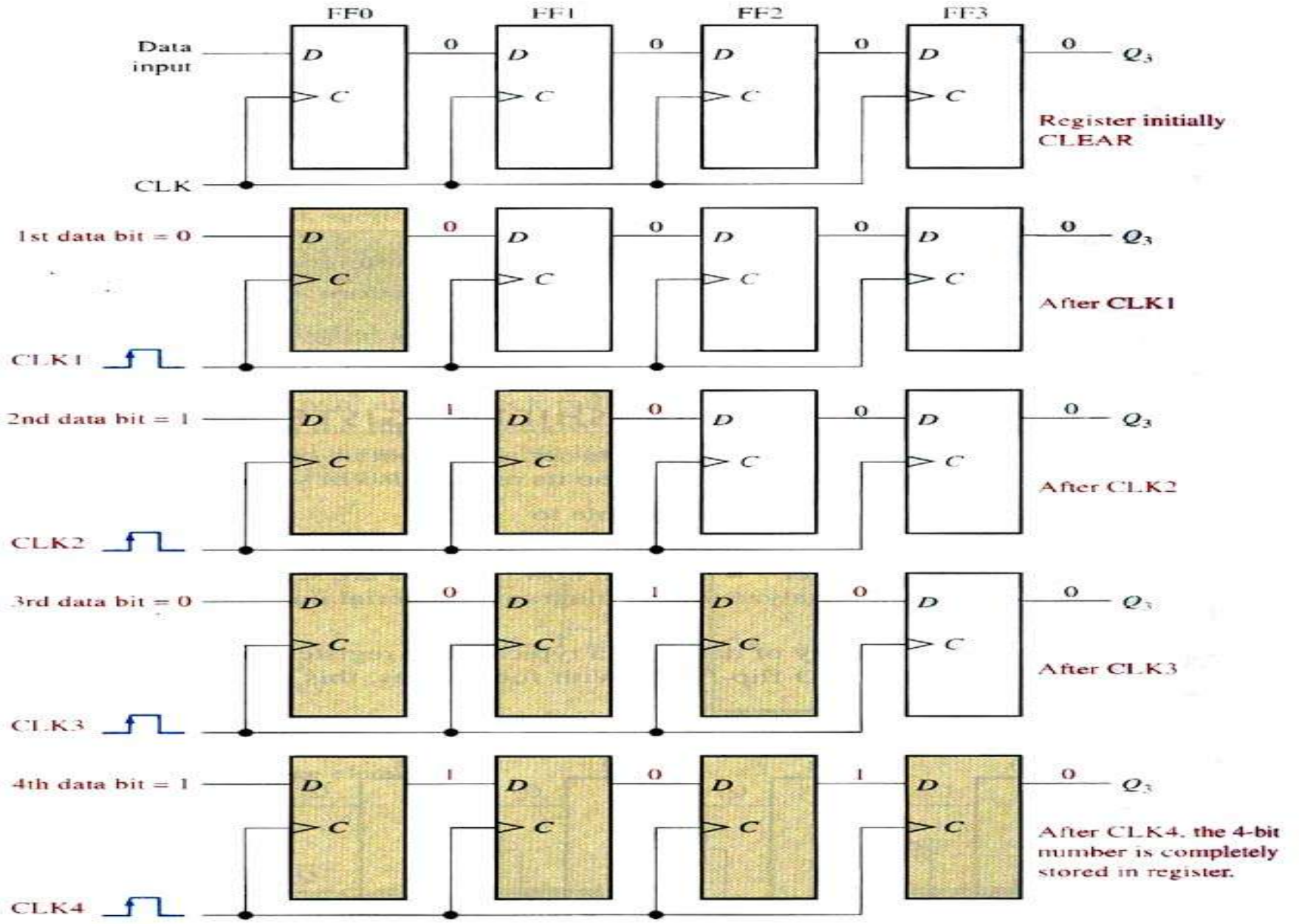
Figure above illustrates entry of the four bits 1010 into the register, beginning with the right-most bit. The register is initially clear. The 0 is put onto the data input line making D= 0 for FF0.

when the first clock pulse is applied, FF0 is reset, thus storing the 0.

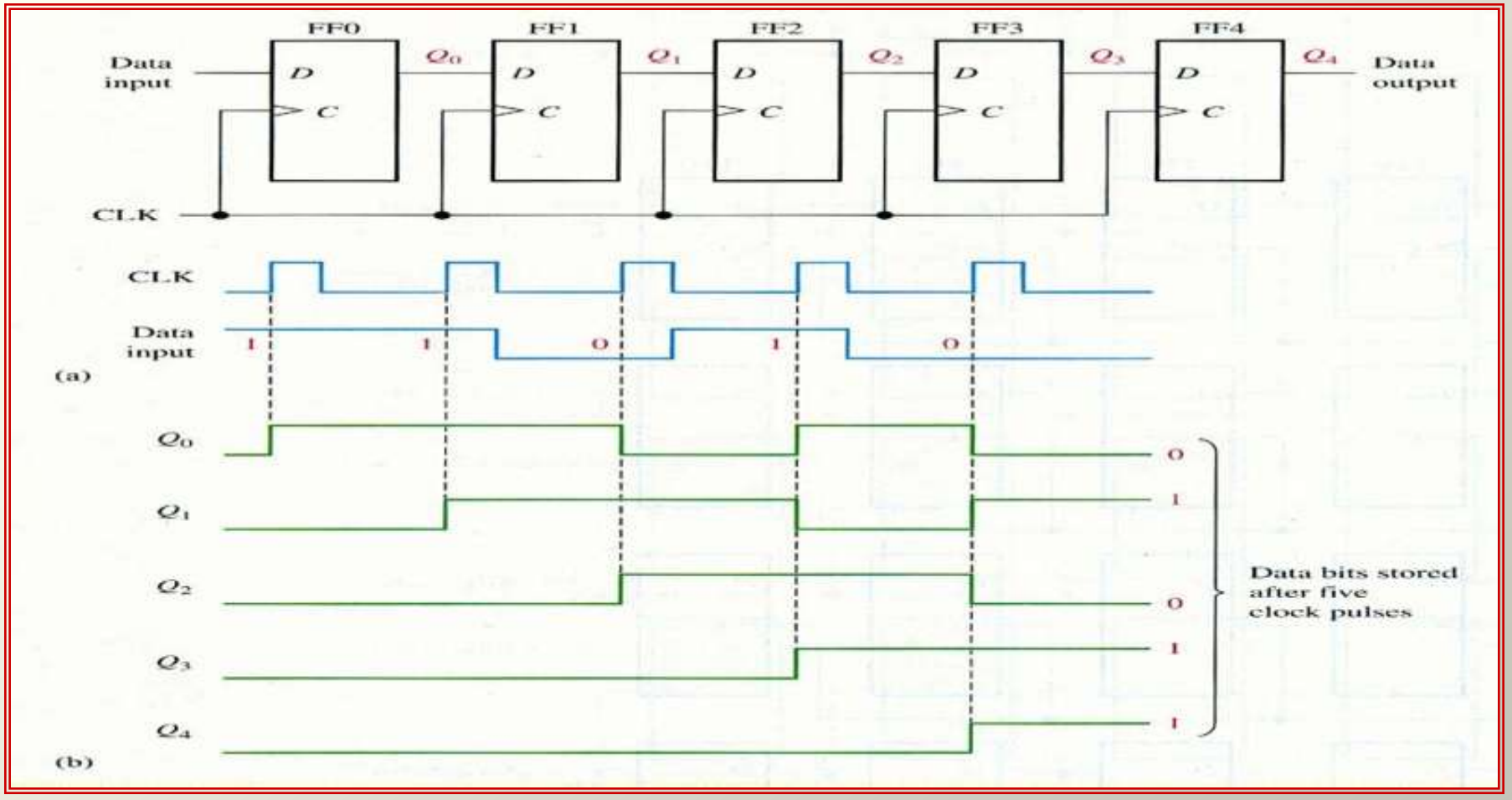
Next the second bit, which is 1, is applied to the data input, making D=1 for FF0 and D=0 for FF1 because the D input of FF1 is connected to the Q_0 output. When the second clock pulse occurs, the 1 on the data input is shifted into FF0, causing FF0 to set; and the 0 that was in FF0 is shifted into FF1.

The third bit, a 0 is now put onto the data-input line, and a clock pulse is applied. The 0 is entered into FF0, the 1 stored in FF0 is shifted into FF1, and the 0 stored in FF1 is shifted onto FF2

The last bit, a 1 is now applied to the data input, and a clock pulse is applied. This time the 1 is entered into FF0, the 0 stored in FF0 is shifted into FF1, the 1 stored in FF1 shifted into FF2, and the 0 stored in FF2 is shifted into FF3. this completes the serial entry of the four bits into the shift register, where they can be stored for any length of time as long as the flip-flops have dc power.

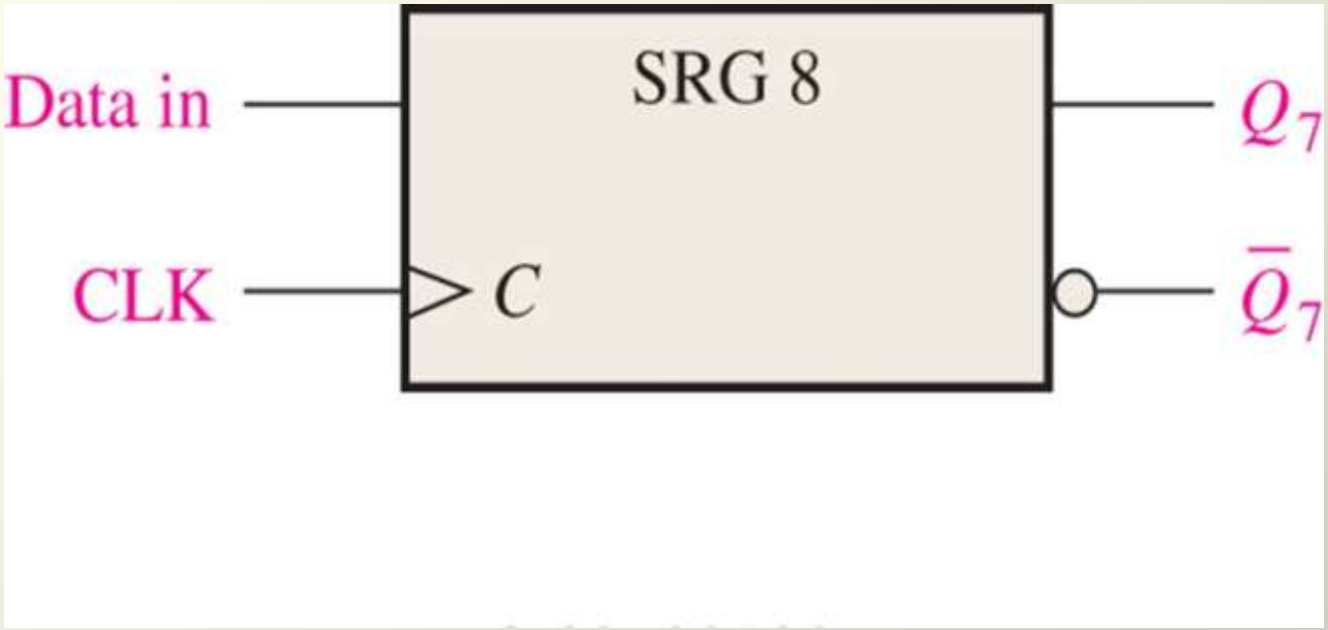

FF0
FF1
FF2
FF3
Data input
CLK
D
C
0
Q_3
Register initially CLEAR
1st data bit = 0
CLK1
After CLK1
2nd data bit = 1
1
CLK2
After CLK2
3rd data bit = 0
CLK3
After CLK3
4th data bit = 1
CLK4
After CLK4, the 4-bit number is completely stored in register.

Example :- Show the states of the 5-bit register for the specified data input and clock waveforms . Assume that the register is initially cleared (all 0s).



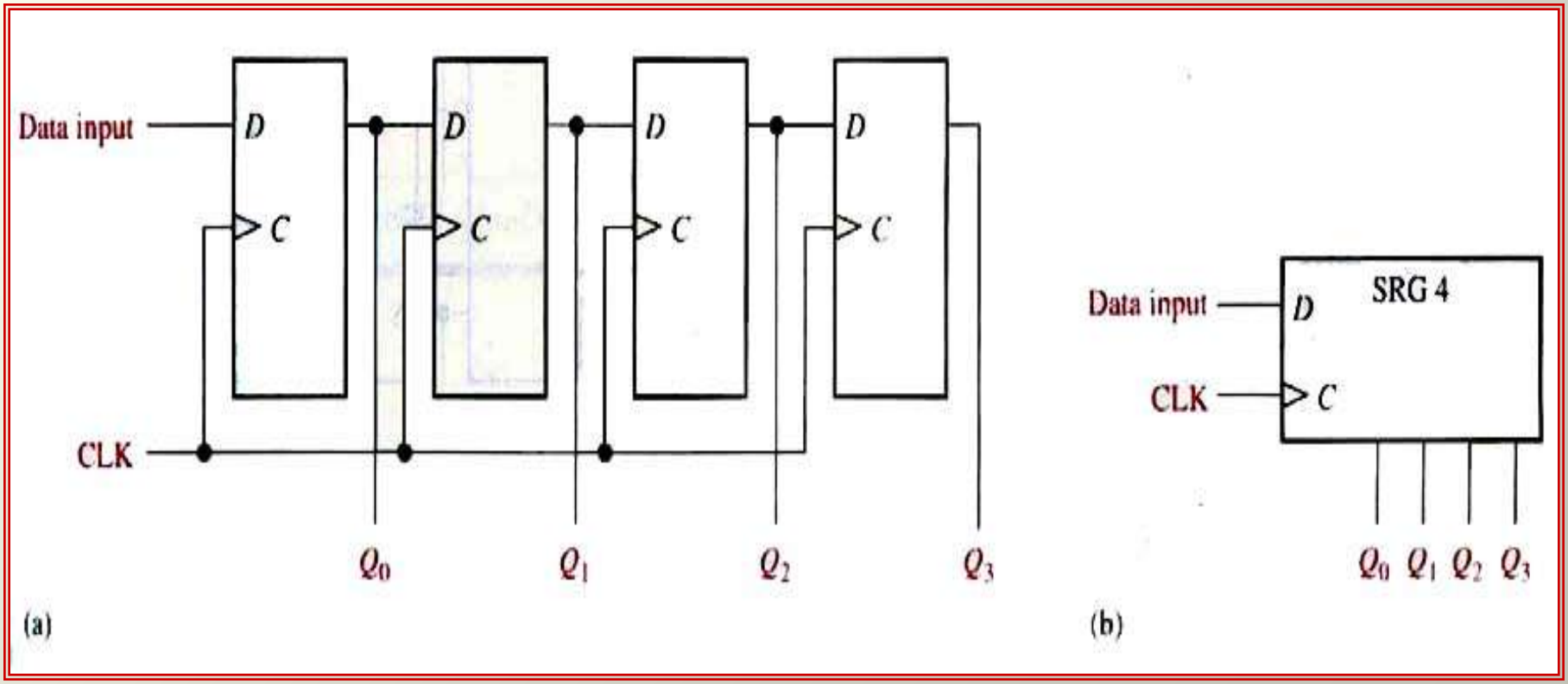
Solution:- The first data bit (1) is entered into the register on the first clock pulse and then shifted from left to right as the remaining bitts are entered and shifted. The register contains $Q_4Q_3Q_2Q_1Q_0 = 11010$ after five clock pulses.

Logic symbol for an 8-bit serial in/serial out shift register.

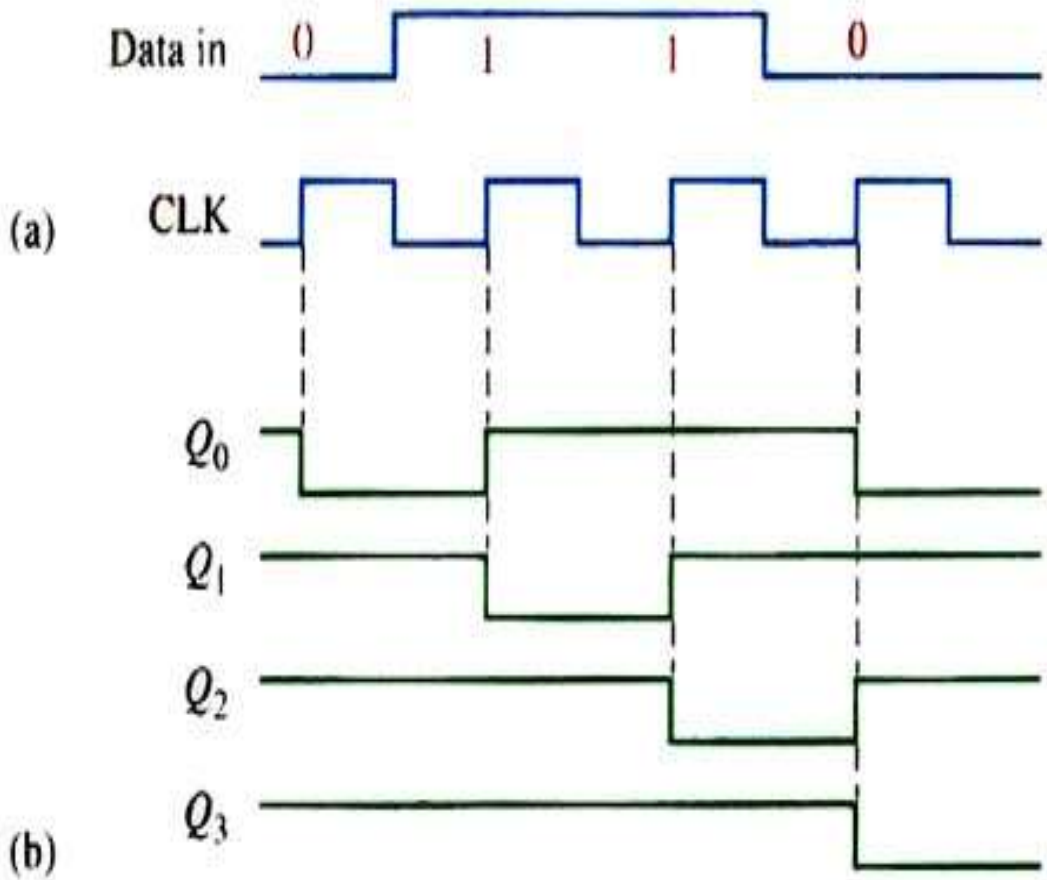


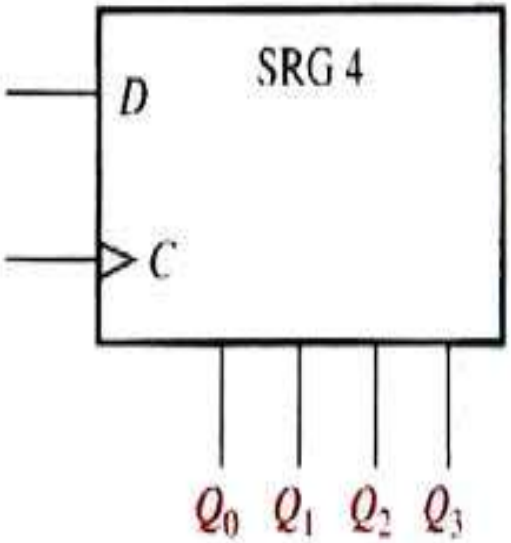
3. Serial in/Parallel Out Shift Registers

The difference of this method is in the way in which the data bits are taken out of the register; in the parallel output register, the output of each stage is available. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously, rather than on a bit-by-bit basis as with serial output.



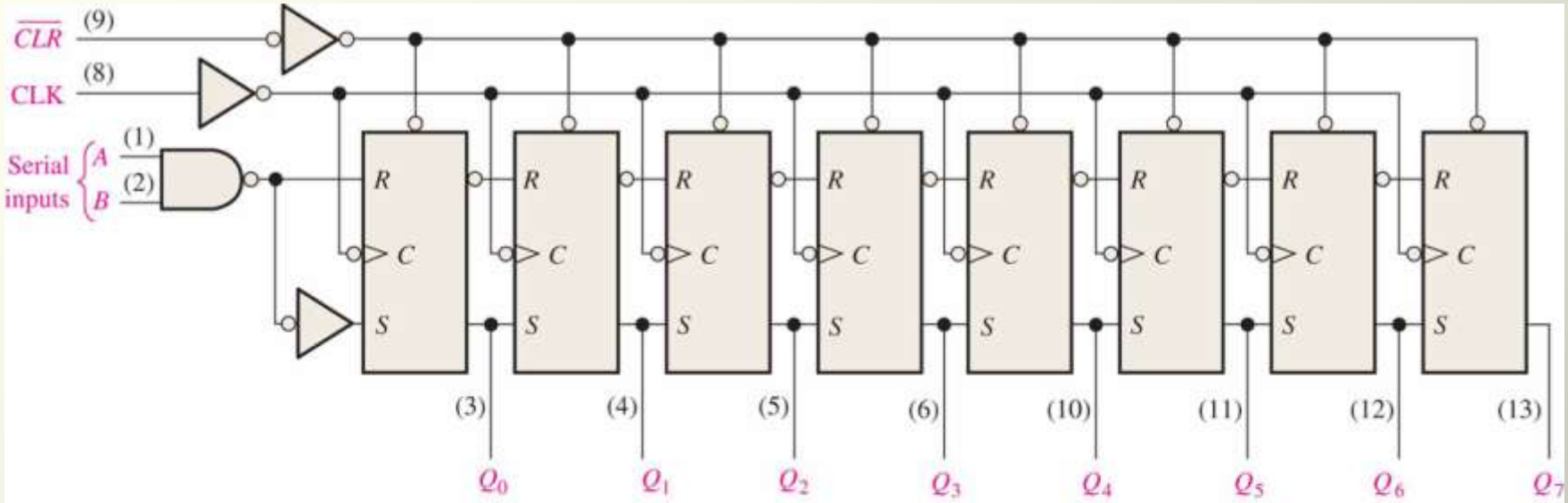
Example :- Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms. The register initially contains all 1s.



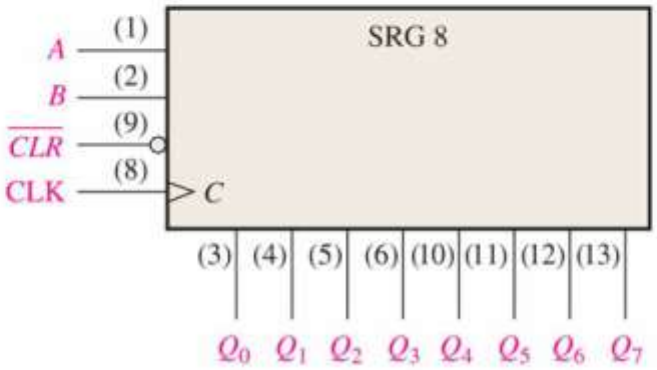


Solution :- The register contains 0110 after four clock pulses

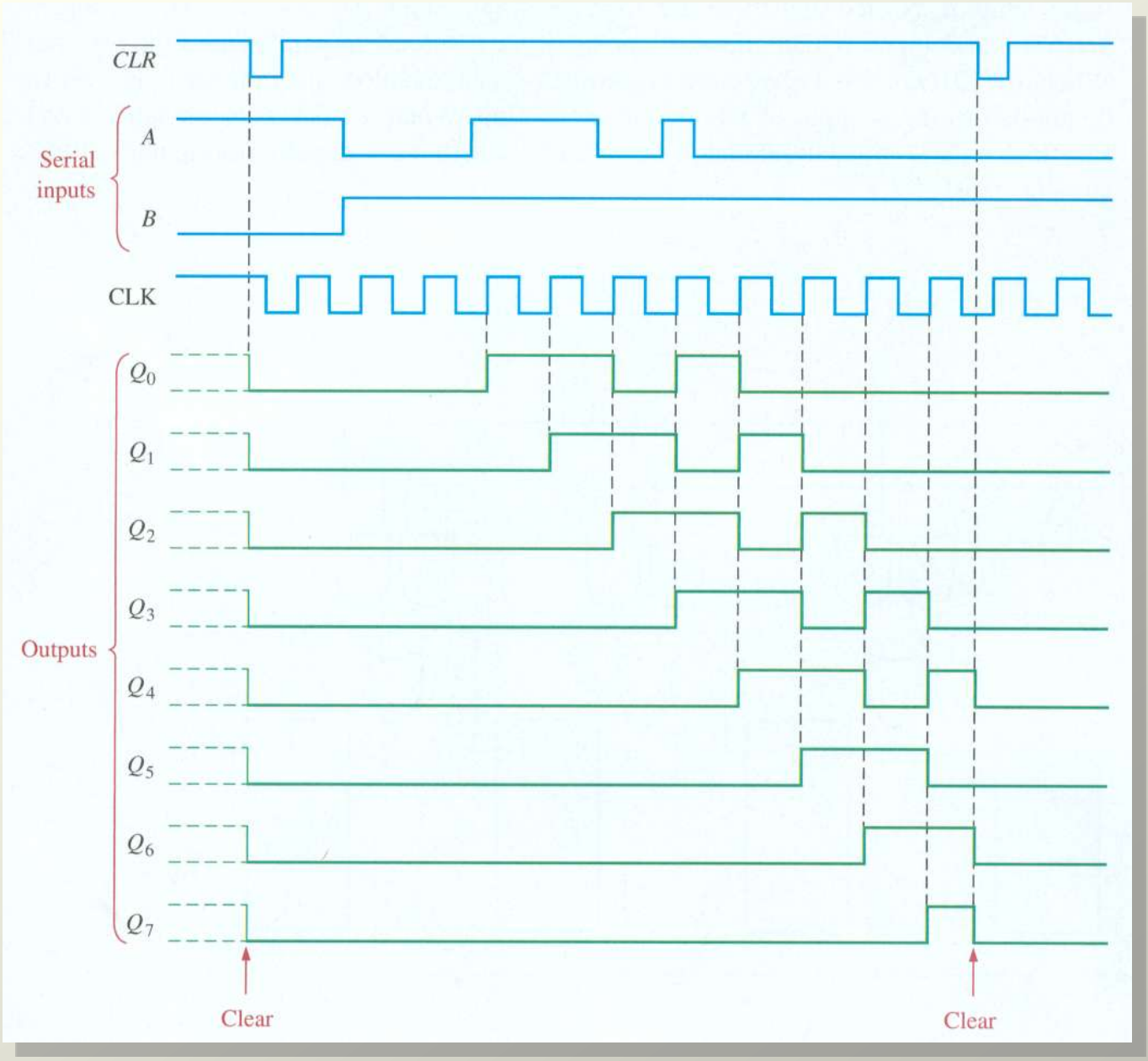
The 74HC164 8-bit serial in/parallel out shift register.



(a) Logic diagram



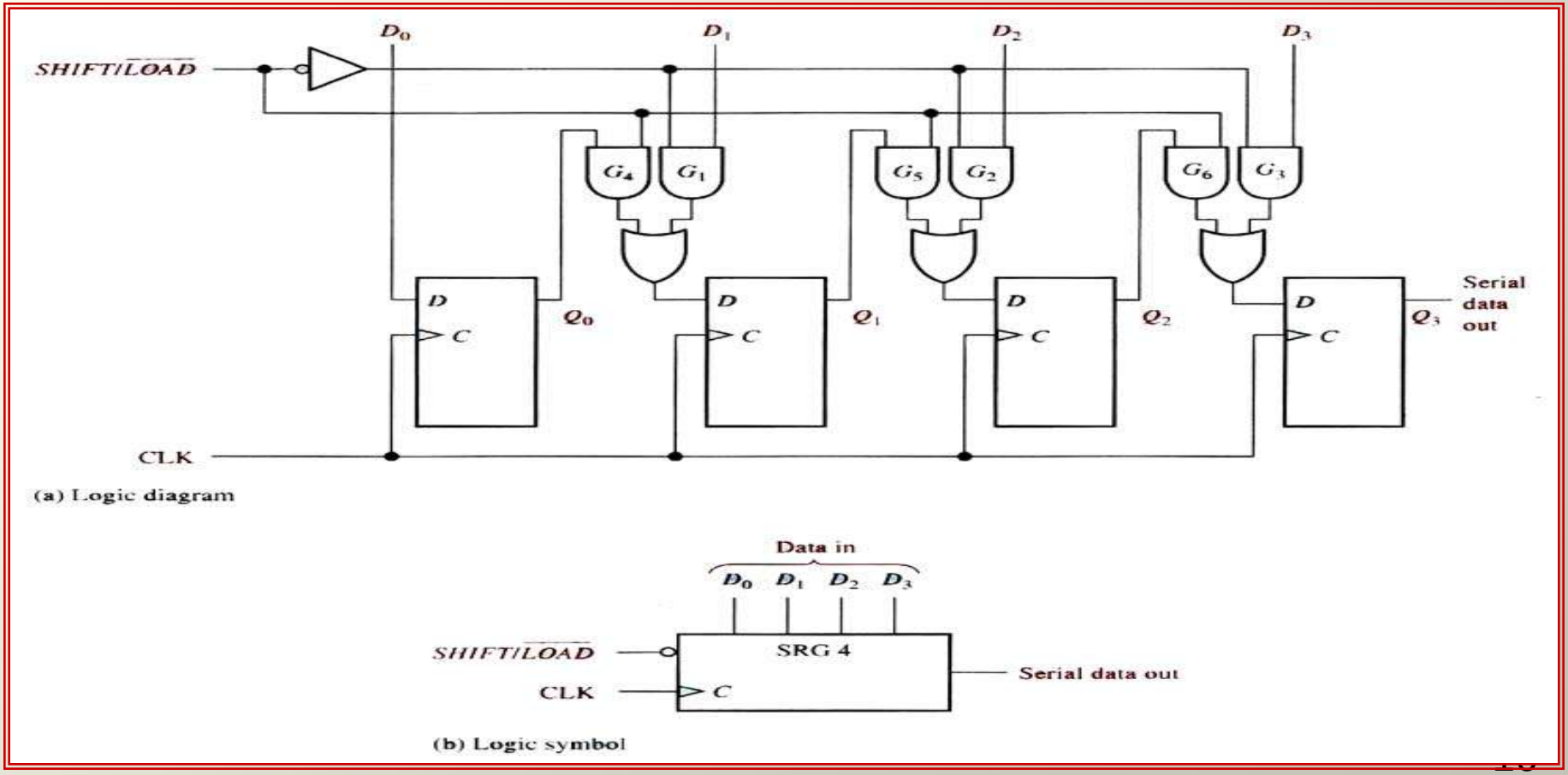
(b) Logic symbol



Timing Diagram

4. Parallel In/ Serial Out Shift Registers

For a register with parallel data inputs, the bits are entered simultaneously into their respective stages on parallel lines rather than on a bit-by-bit basis on one lines as with serial data inputs.

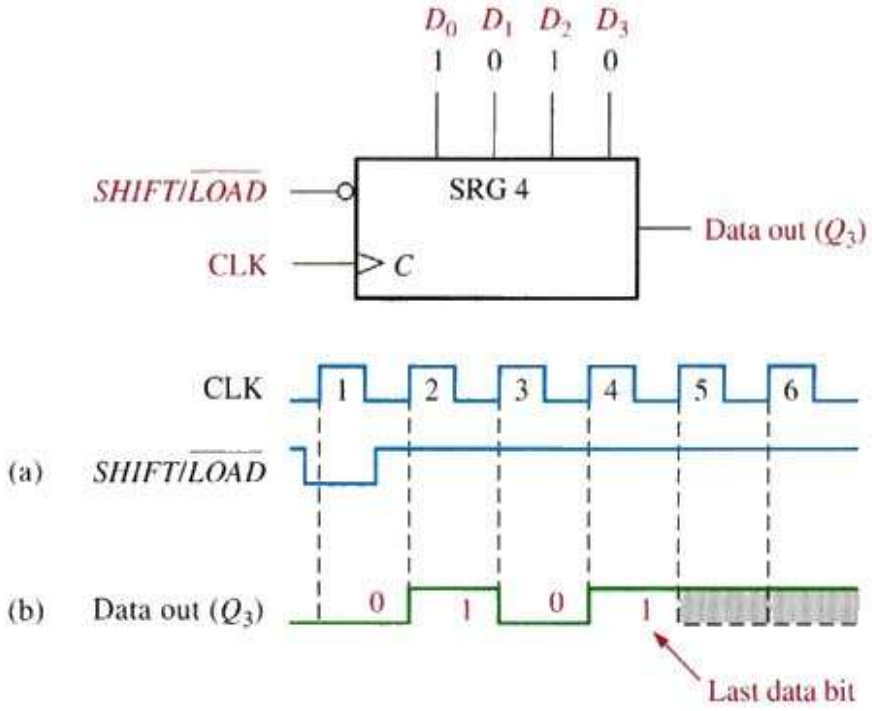


The previous figure shows a 4-bit Parallel In/Serial Out shift register and a typical logic symbol. There are four data lines D0, D1, D2, D3 and a SHIFT/LOAD' input, which allows four bits of data to load in parallel into the register. When Shift/Load' is LOW, gates G1 through G3 are enabled, allowing each data bit to be applied to the D input of its respective flip-flop. When a clock pulse, the flip-flops with D=1 will set and those with D= 0 will reset, thereby storing all four bits simultaneously.

When Shift/Load' is HIGH, gates G1 through G3 are disabled and gates G4 through G6 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which AND gates are enabled by the level on the Shift/Load' input.

EXAMPLE

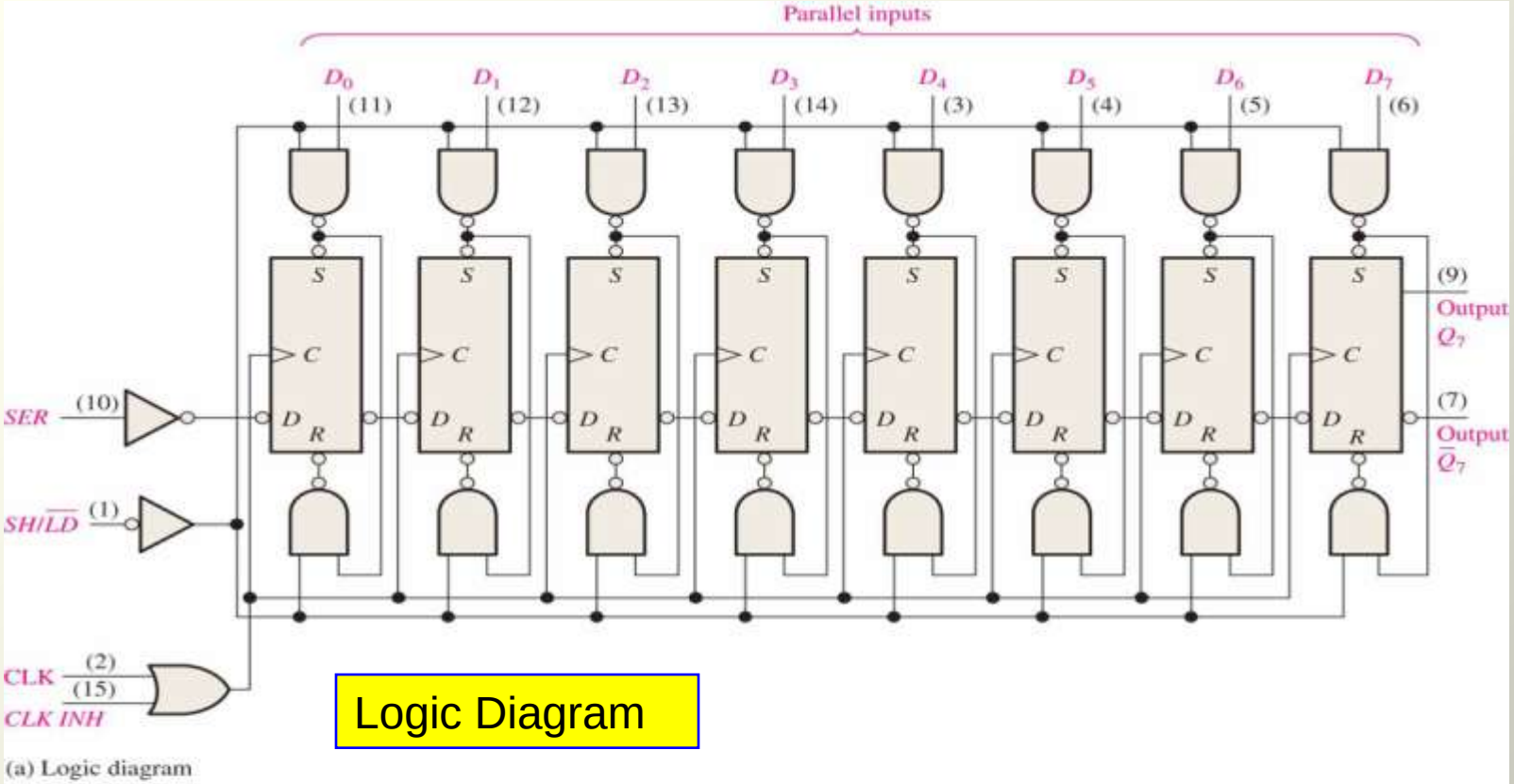
Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT/$\overline{LOAD}$* waveforms



Solution On clock pulse 1, the parallel data ($D_0D_1D_2D_3 = 1010$) are loaded into the register, making Q_3 a 0. On clock pulse 2 the 1 from Q_2 is shifted onto Q_3; on clock pulse 3 the 0 is shifted onto Q_3; on clock pulse 4 the last data bit (1) is shifted onto Q_3; and on clock pulse 5, all data bits have been shifted out, and only 1s remain in the register (assuming the D input remains a 1).

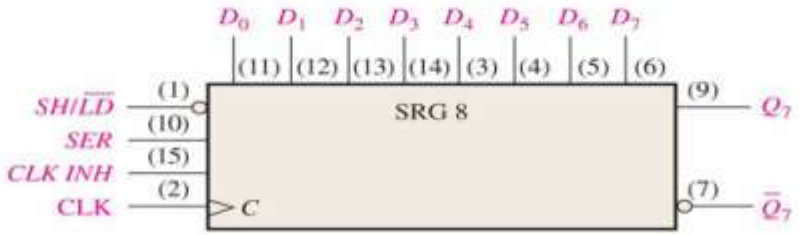
The 74HC165 8-bit parallel load shift register.

- 8-bit version



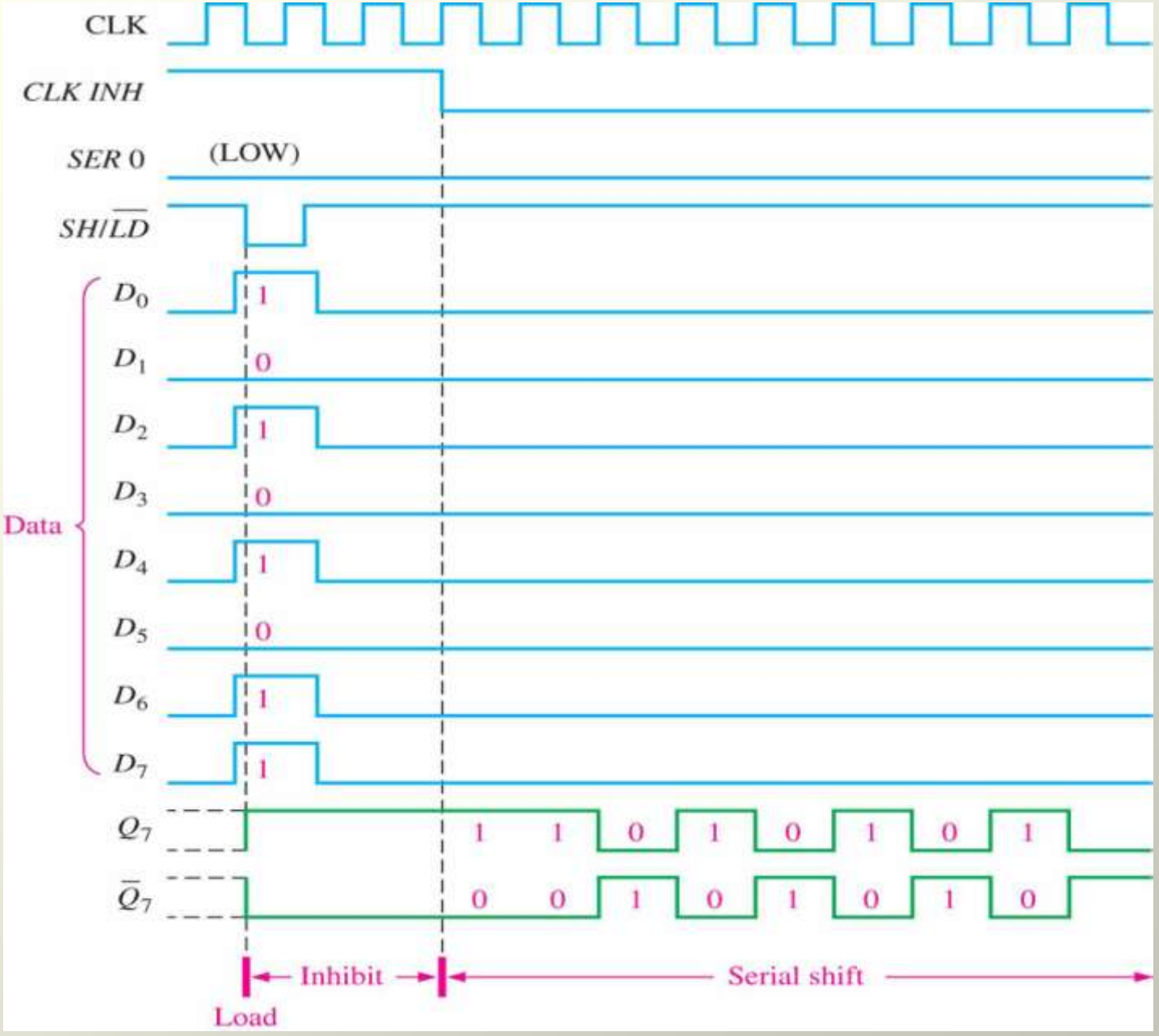
Logic Diagram

(a) Logic diagram



Logic symbol

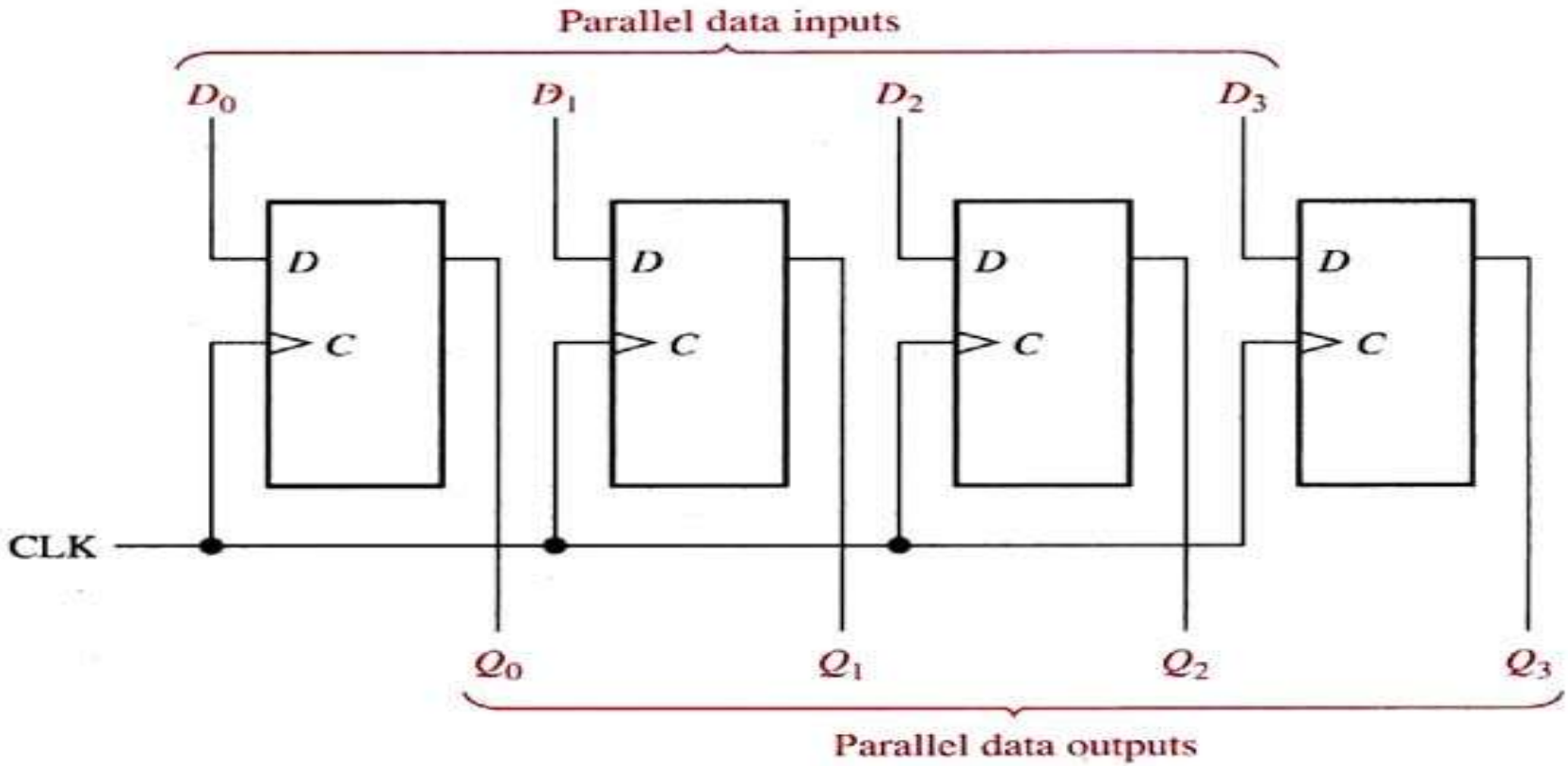
(b) Logic symbol



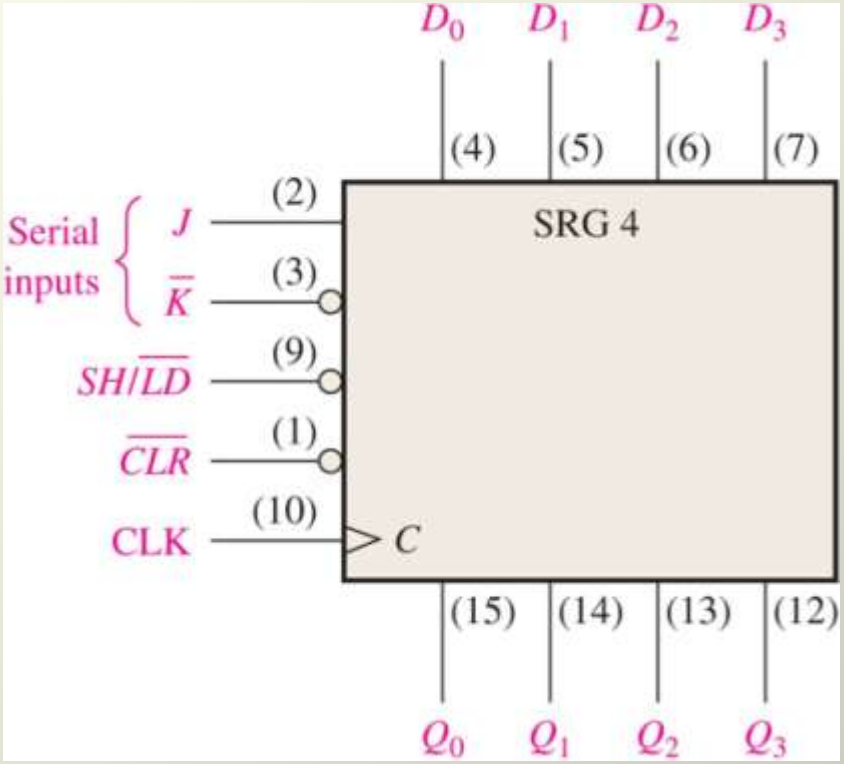
Sample Timing Diagram

5. Parallel In/ Parallel Out Shift Registers

The Parallel in/ Parallel out register employs both Parallel entry and Parallel output of data. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.



The 74HC195 4-bit parallel-access shift register.
4-bit parallel in /parallel out SR



Logic symbol

Sample timing diagram for a 74HC165 shift register.
4-bit parallel/parallel out SR
synchronous CLR, asynchronous LD