

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information				
معلومات المادة الدراسية				
Module Title	Logic Design I		Module Delivery	
Module Type	C		<input checked="" type="checkbox"/> Theory <input checked="" type="checkbox"/> Lecture <input checked="" type="checkbox"/> Lab <input type="checkbox"/> Tutorial <input type="checkbox"/> Practical <input type="checkbox"/> Seminar	
Module Code	CSDC112			
ECTS Credits	6			
SWL (hr/sem)	150			
Module Level	UGI	Semester of Delivery		one
Administering Department	CSIT	College	Type College Code	
Module Leader	Wesam Mohammed Jasim Abid Alrawi		e-mail	co.wesam.jasim@uoanbar.edu.iq
Module Leader's Acad. Title	Professor	Module Leader's Qualification	Ph.D.	
Module Tutor	Name (if available)		e-mail	E-mail
Peer Reviewer Name	Name		e-mail	E-mail
Scientific Committee Approval Date	01/06/2023	Version Number	1.0	

Relation with other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents

أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية

Module Objectives أهداف المادة الدراسية	1- The student should understand number systems and codes and conversion between them. 2- The student should understand the Boolean expression and how to apply it. 3- The student should recognize among different logic gates and how to use them. 4- The student should understand how to design a logic circuit. 5- The student should understand using K-map for simplification.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	Demonstrate a solid understanding of digital logic principles, including Boolean algebra, logic gates, truth tables, and the concept of binary representation.
Indicative Contents المحتويات الإرشادية	Introduction to Digital Logic Combinational Logic Design Arithmetic circuits Sequential Logic Design Circuit Testing and Verification

Learning and Teaching Strategies

استراتيجيات التعلم والتعليم

Strategies	Conceptual Understanding Problem-Solving Approach Hands-on Laboratory Experience Design Projects Simulation and Modeling Problem-Based Learning
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Student Workload (SWL)

الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation					
تقييم المادة الدراسية					
		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	Midterm Exam	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)	
المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction to number system
Week 2	Conversion between systems
Week 3	Codes and conversion among them
Week 4	Codes and conversion among them1
Week 5	Boolean expression
Week 6	Logic gates
Week 7	Mid-term Exam
Week 8	Logic gates design
Week 9	Circuit Design
Week 10	Second month exam
Week 11	NAND gates
Week 12	NOR gates
Week 13	Sum of product form
Week 14	Product Of sum form
Week 15	K-map
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus)

المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	Codes and conversion among them
Week 2	Codes and conversion among them1
Week 3	Boolean expression
Week 4	Logic gates
Week 5	Circuit Design
Week 6	Second month exam
Week 7	NAND gates & NOR gates
Week 8	Sum of product form
Week 9	Product Of sum form
Week 10	K-map

Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	An Introduction to Logic Technology by Luoish Nashlsky	Yes
Recommended Texts	Fundamentals of logic design by J. Roth	No
Websites		

Grading Scheme

مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	A - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 - 49)	FX – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.