MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Logic Design II**			**Module Delivery**	
Module Type	**C**			☒**Theory** ☒**Lecture** ☒**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	**CSDC122**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	UGI		**Semester of Delivery**	2	
Administering Department	CSIT		**College**	Type College Code	
Module Leader	Name		**e-mail**	E-mail	
Module Leader's Acad. Title	Professor		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date	01/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	CSDC112	**Semester**	1
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	- The student should understand encoder , decoder and multiplexers - The student should understand synchronous logic circuit - The student should understand flip-flops and how to use them - The student should understand registers and their types - The student should understand counters and their types - The student should understand ROM and PLA implementation
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	- The student should understand encoder, decoder and multiplexers - The student should understand flip-flops and how to use them. - The student should understand registers and their types. - The student should understand counters and their types. - The student should understand ROM and PLA implementation.
Indicative Contents المحتويات الإرشادية	This course covers the logic design advanced concepts. It starts with combinational logic circuit design. From these designs are adder and subtractor. This course also covers the explanation of different circuit such as decoder, encoder and multiplexers. At the end of course, the flip-flop, latches and counter are covered

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	- The student should use utilities in the lab to apply scientific experiment - The ability to design a logic circuit.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	Midterm Exam	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Synchronous logic gates
Week 2	Adder and subtractor circuits
Week 3	Comparator circuits
Week 4	Encoders
Week 5	Multiplexers
Week 6	Flip-flops
Week 7	Mid-term Exam
Week 8	SR flip flop and j k flip flop
Week 9	T flip flop and D flip flop
Week 10	Second month exam
Week 11	Registers design
Week 12	Counters design
Week 13	ROM
Week 14	PLA
Week 15	State plan
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Synchronous logic gates
Week 2	Adder and subtractor circuits
Week 3	Comparator circuits
Week 4	Encoders
Week 5	Multiplexers
Week 6	Flip-flops
Week 7	SR flip flop and j k flip flop
Week 8	T flip flop and D flip flop
Week 9	Second month exam
Week 10	Registers design
Week 11	Counters design
Week 12	ROM
Week 13	PLA
Week 14	State plan

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	- "Digital Design" 4th Edition by M. Morris Mano and Michael D. Ciletti - Fundamentals of logic design by J. Roth	No
Recommended Texts		
Websites		

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings

	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.