	Ministry of Higher Education and Scientific Research. University of Anbar. Department of Information System.	

MODULE DESCRIPTOR FORM

Module Information					
Module Title	Logic Design II		**Module Type**	TYPE B	
Module Code	CSIT111		**ECTS Credits**	6	
Module Level	UGI		**Semester of Delivery**	Two	
Administering Department	IS		**Faculty**	CSIT	
Module Leader	Muntaser AbdulWahed Salman Abdulaziz		**e-mail**	co.montasser.salman@uoanbar.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	PhD.	
Module Tutor			**e-mail**		
Peer Reviewer Name	/		**e-mail**	/	
Review Committee Approval	DD/MM/YY		**Version Number**	2.0	

Relation With Other Modules	
Pre-requisites	CSIT109
Co-requisites	

Module Aims, Learning Outcomes and Indicative Contents	
Module Aims	● The student should understand encoder, decoder and multiplexers ● The student should understand synchronous logic circuit ● The student should understand flip-flops and how to use them ● The student should understand registers and their types ● The student should understand counters and their types ● The student should understand ROM and PLA implementation
Module Learning Outcomes	A1. The student should understand encoder, decoder and multiplexers A2. The student should understand flip-flops and how to use them.

	A3. The student should understand registers and their types. A4. The student should understand counters and their types. A5. The student should understand ROM and PLA implementation.
Indicative Contents	

Learning and Teaching Strategies

Strategies	The main strategy that will be adopted in delivering this module are: 1. Power point presentation (Data show). 2. Explanation on the white board using different color markers. 3. Discussions with the student during teaching. 4. Interaction with students through daily problems practice through lecture. 5. Solve different problems with more exercises. 6. Submit assignment that develop student learning.

Module Delivery

Structured workload (h/w)	4.4
Unstructured workload (h/w)	5.6
Total workload (h/w)	10

Module Evaluation

	Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Quizzes	3	6% (6)	3,7 and 11	
Assignments	2	6% (6)	2 and 12	
Projects / Lab.	1	15% (15)	Continuous	
Report	1	5% (5)	13	
Midterm Exam	2 hr	18% (18)	7	
Final Exam	3 hr	50% (50)	16	
Total		100% (100 Marks)		

Learning and Teaching Resources

	Text	Available in the

		Library?
Required Texts		Yes/No
Recommended Texts		Yes/No
Websites		

Delivery Plan (Weekly Syllabus)	
	Material Covered
Week 1	Synchronous logic gates
Week 2	Adder and subtractor circuits
Week 3	Comparator circuits
Week 4	Encoders and multiplexers
Week 5	Multiplexers
Week 6	First month exam
Week 7	**Mid-Term Exam**
Week 8	Flip-flops
Week 9	SR flip flop and j k flip flop
Week 10	T flip flop and D flip flop
Week 11	Second month exam
Week 12	Registers design
Week 13	Counters design
Week 14	ROM PLA State plan
Week 15	**Preparatory Week**

Week 16	Final Exam

APPENDIX:

UNIVERSITYof Anbar				
GRADING SCHEME				
Group	**ECTS Grade**	**% of Students/Marks**	**Definition**	**GPA**
Success Group (50 - 100)	**A** - Excellent	Best 10%	Outstanding Performance	**5**
	B - Very Good	Next 25%	Above average with some errors	**4**
	C - Good	Next 30%	Sound work with notable errors	**3**
	D - Satisfactory	Next 25%	Fair but with major shortcomings	**2**
	E - Sufficient	Next 10%	Work meets minimum criteria	**1**
Fail Group (0 – 49)	**FX** – Fail	(45-49)	More work required but credit awarded	
	F – Fail	(0-44)	Considerable amount of work required	
Note:				

NB Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The university has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.