University of Anbar
College of Engineering
Dept. of Electrical Engineering

Fundumantal of Electronic II

Second Class

Chapter05: BJT AC Analysis

Lec05_p1

Munther N. Thiyab

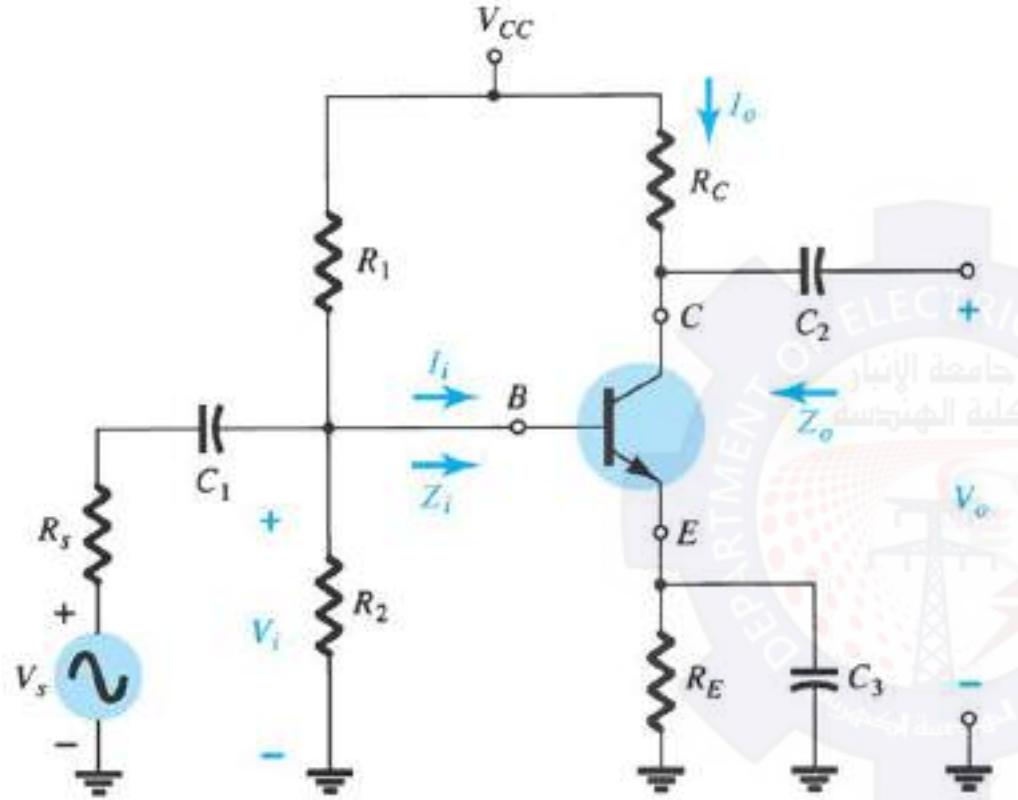
2019-2020

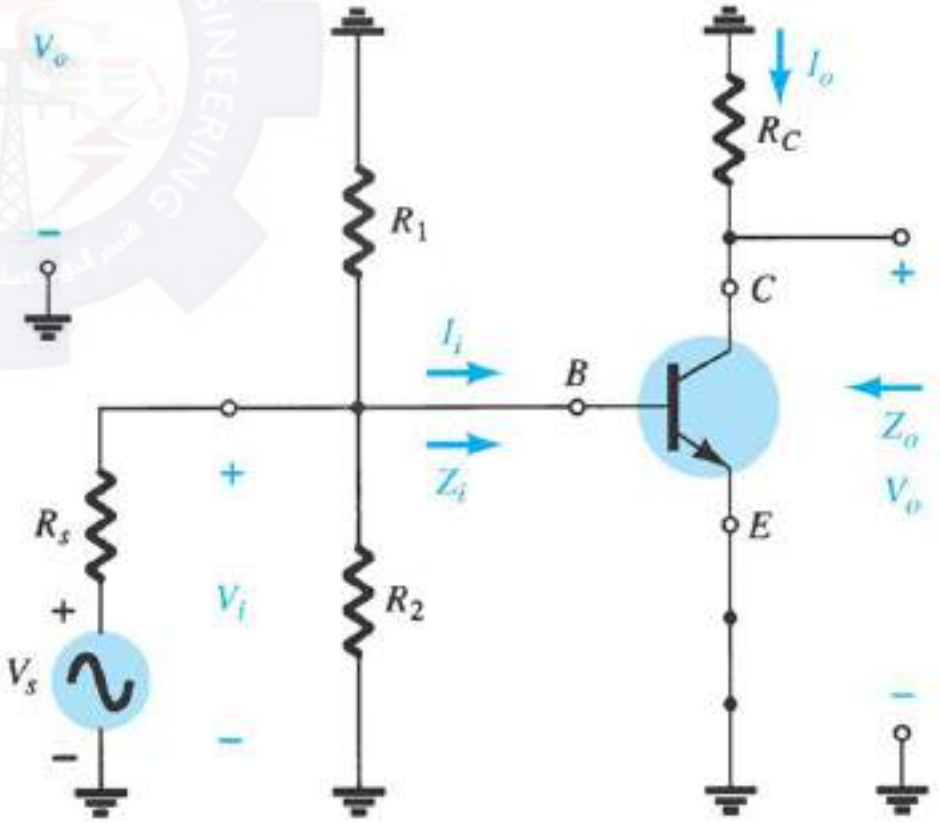
BJT Transistor Modeling

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- A model uses circuit elements that approximate the behavior of the transistor.
- There are two models commonly used in small signal AC analysis of a transistor:
  - **r_e model**
  - **Hybrid equivalent model**

BJT Transistor Modeling

Capacitors chosen with very small reactance at the frequency of application → replaced by low-resistance or short circuit.

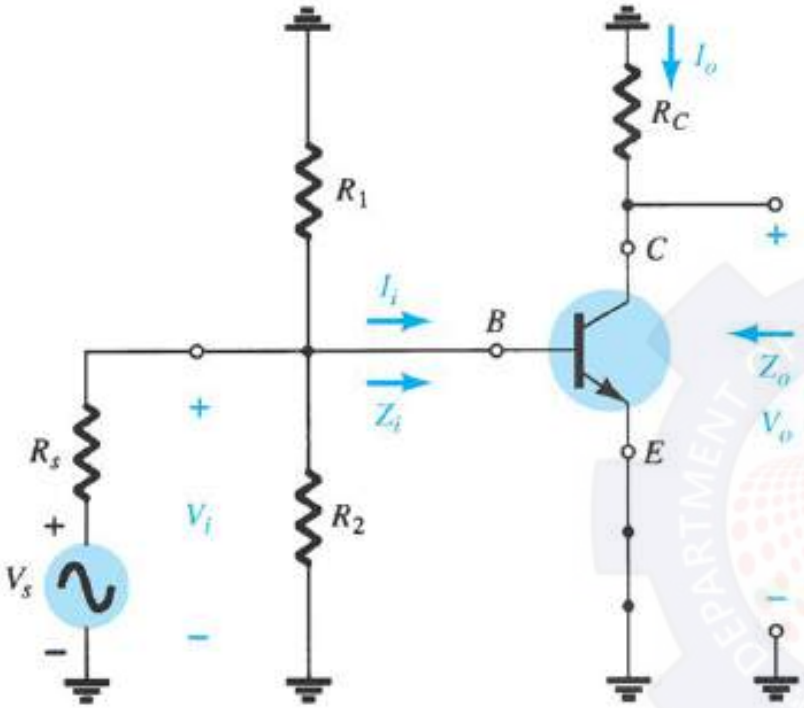




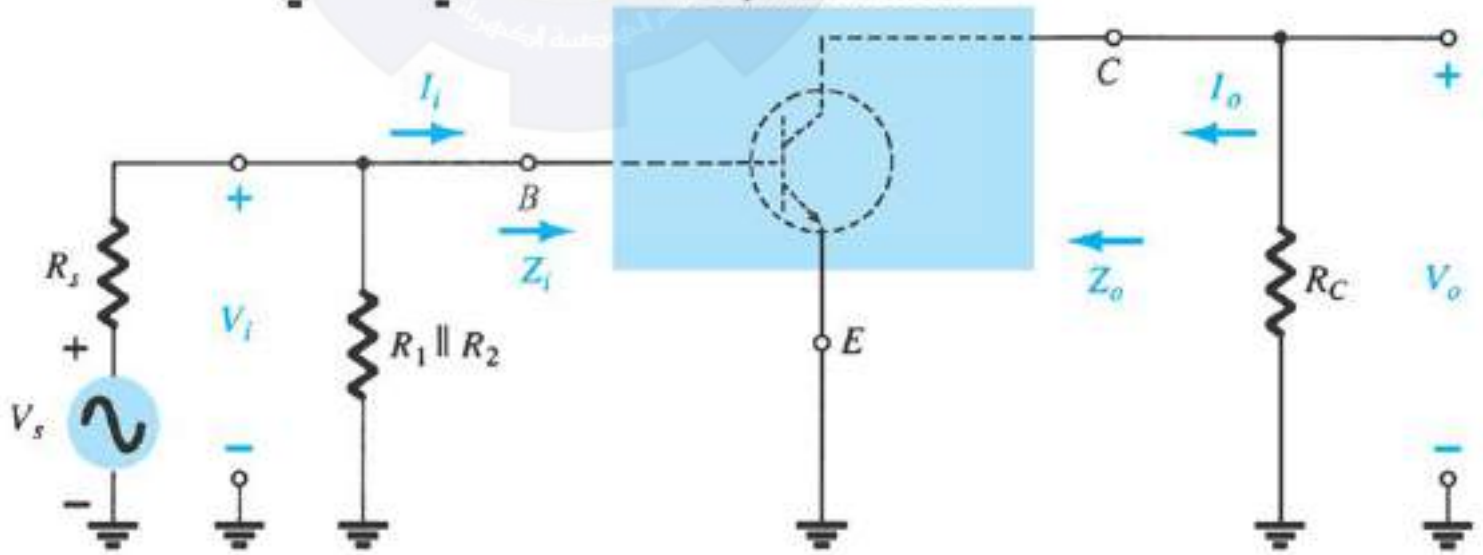
Removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

BJT Transistor Modeling

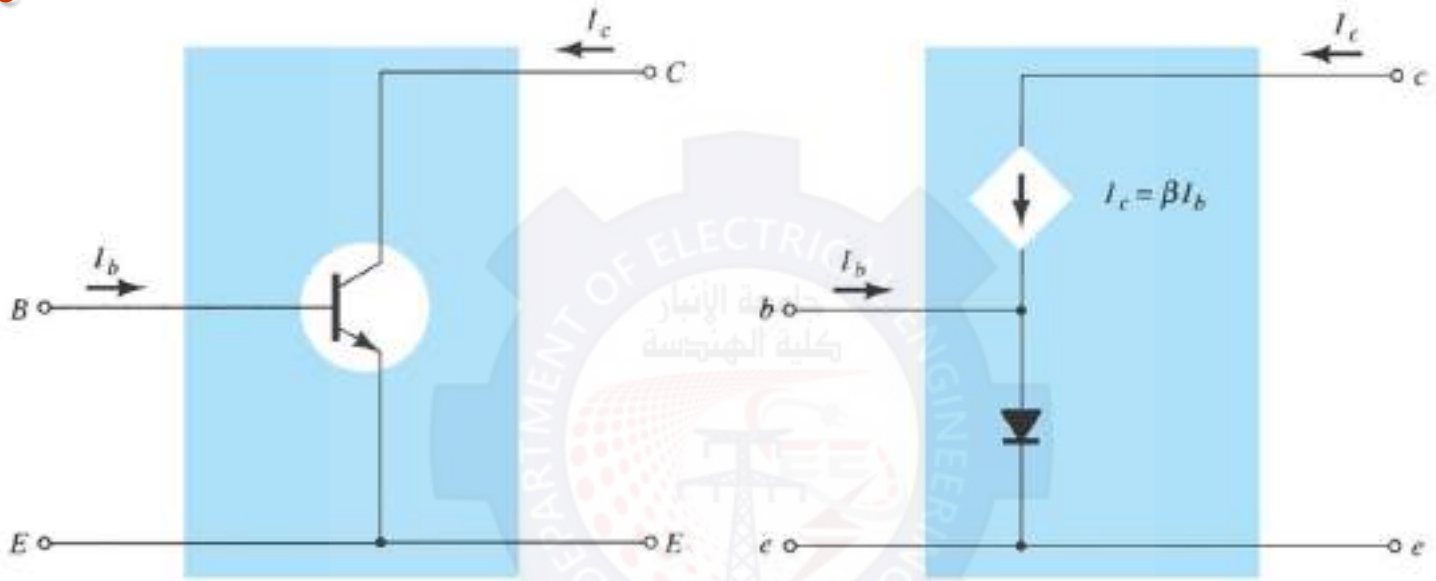
Circuit redrawn for small-signal ac analysis



Transistor small-signal ac equivalent circuit



The r_e Transistor Model Common Emitter Configuration

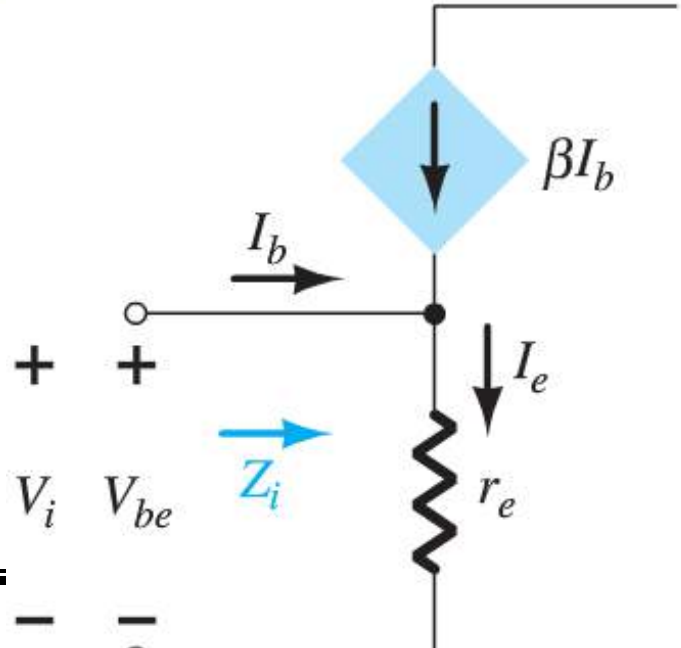


$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$

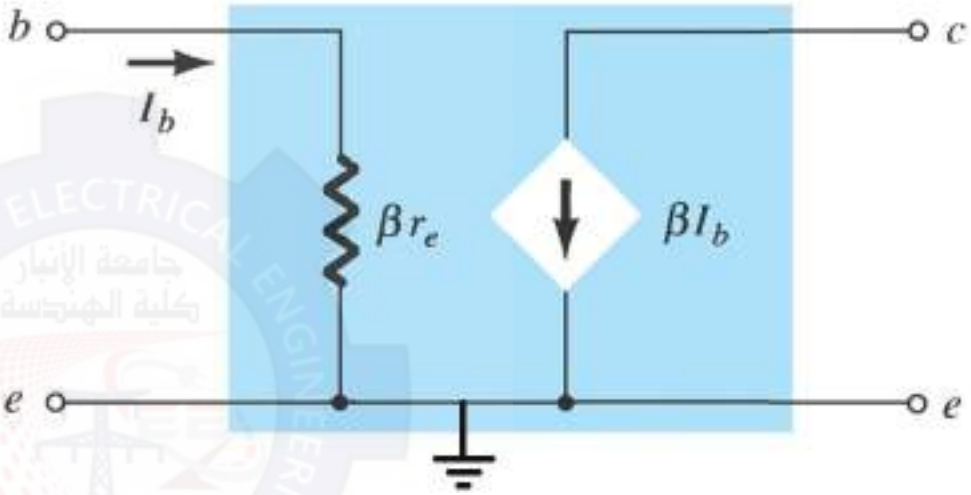
$$= (\beta + 1) I_b r_e$$

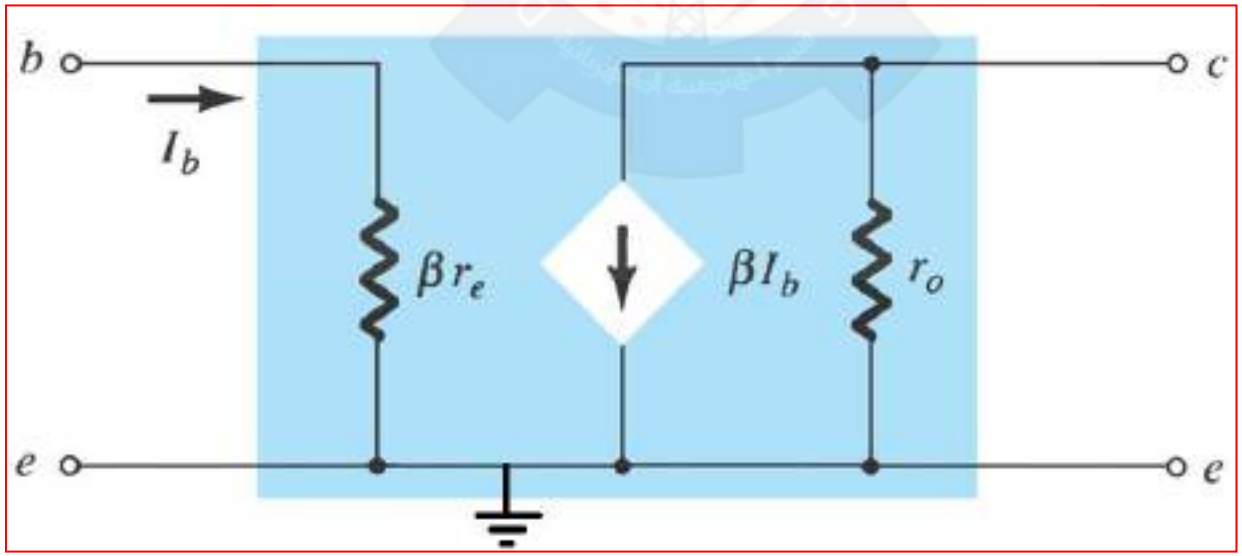
$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b} = (\beta + 1) r_e \simeq \beta r_e$$



The r_e Transistor Model Common Emitter Configuration

$$r_e = \frac{26\ mV}{I_E}$$





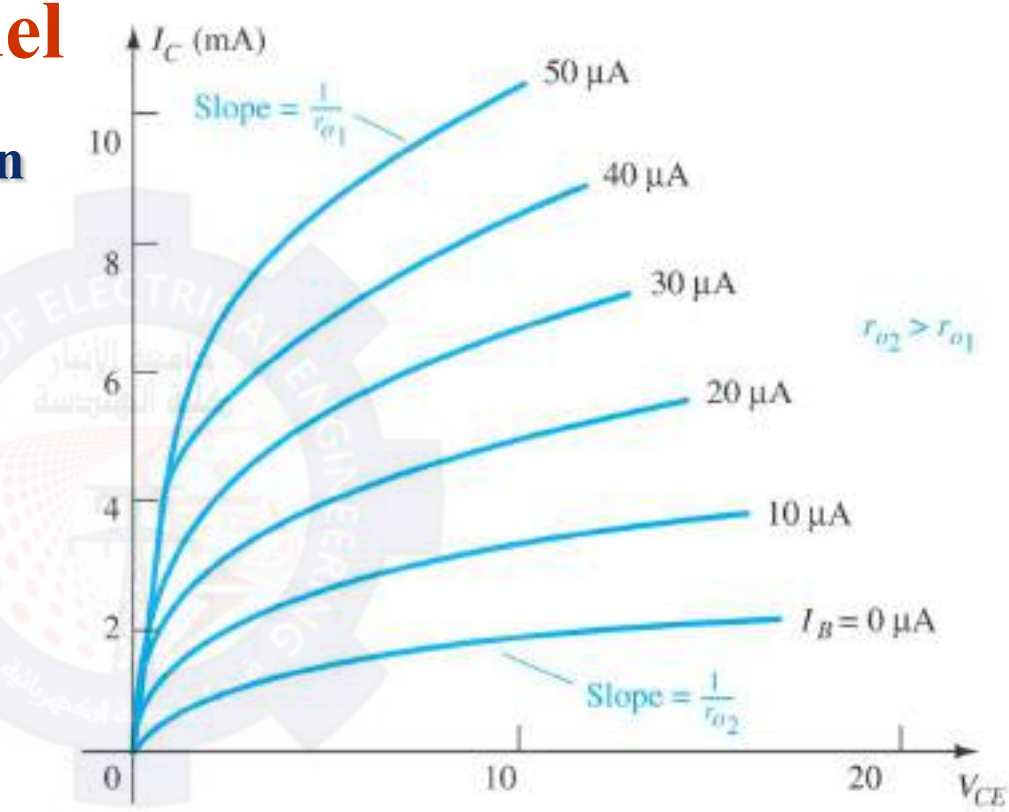
The r_e Transistor Model

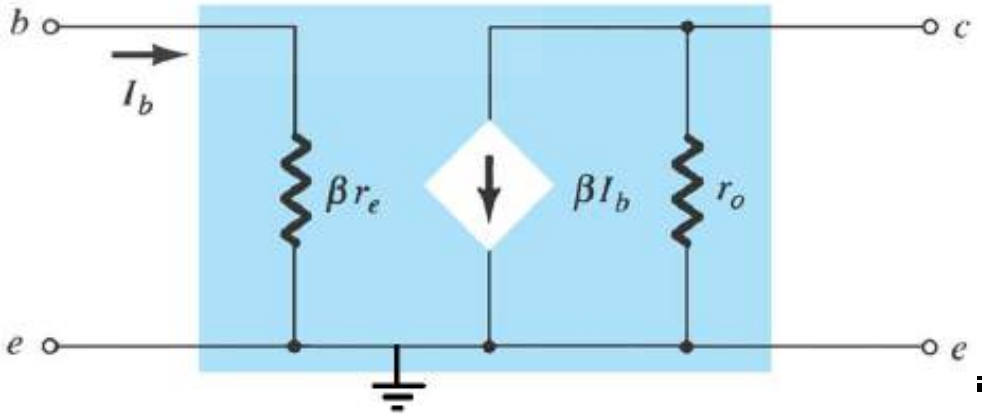
Common Emitter Configuration

$$slope = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_0}$$

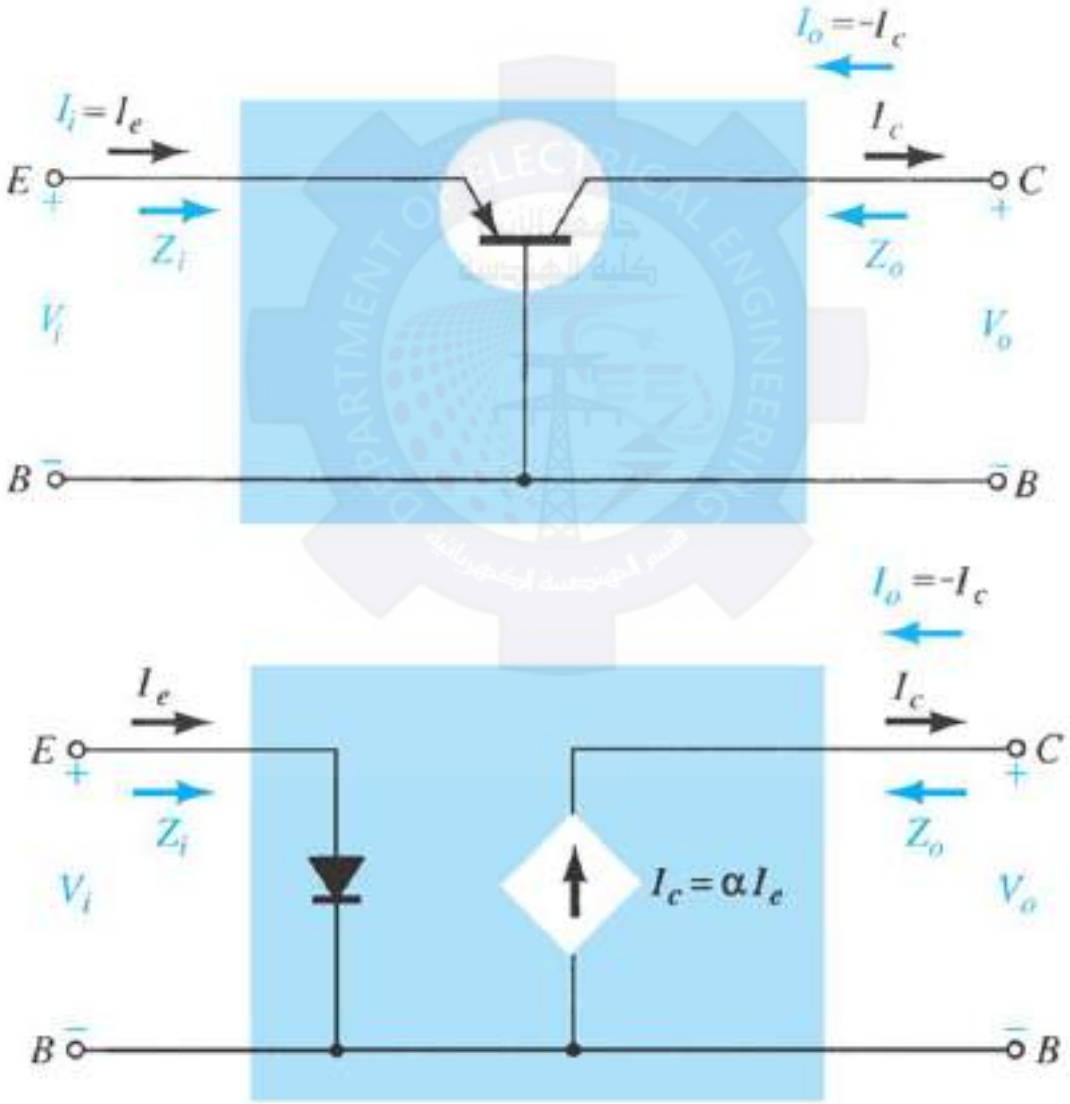
$$r_0 = \frac{\Delta V_{CE}}{\Delta I_C}$$

The output resistance r is typically in the range of 40 kΩ to 50 kΩ

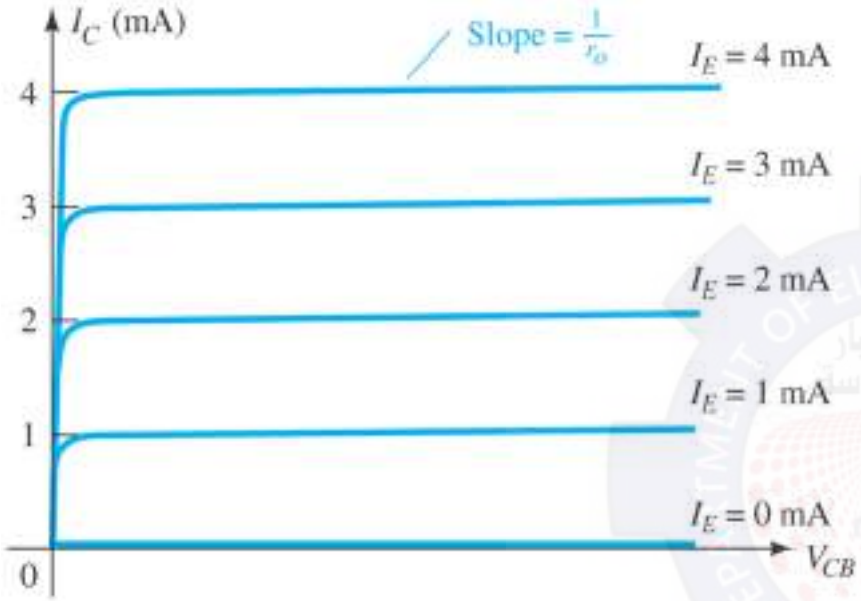


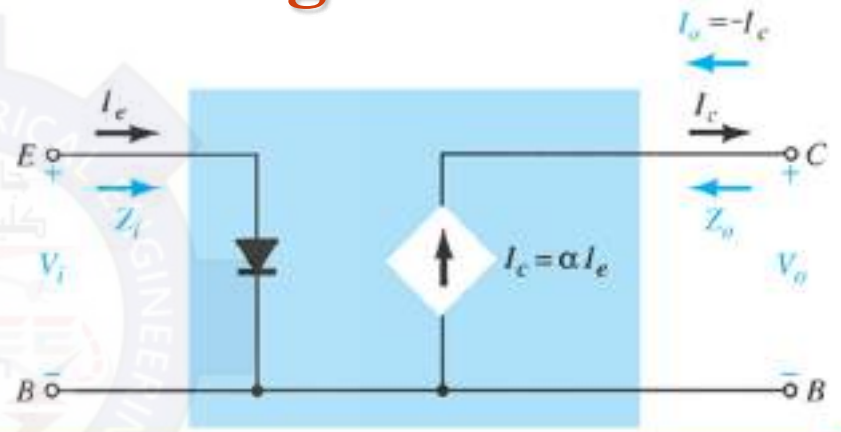


Common-Base Configuration



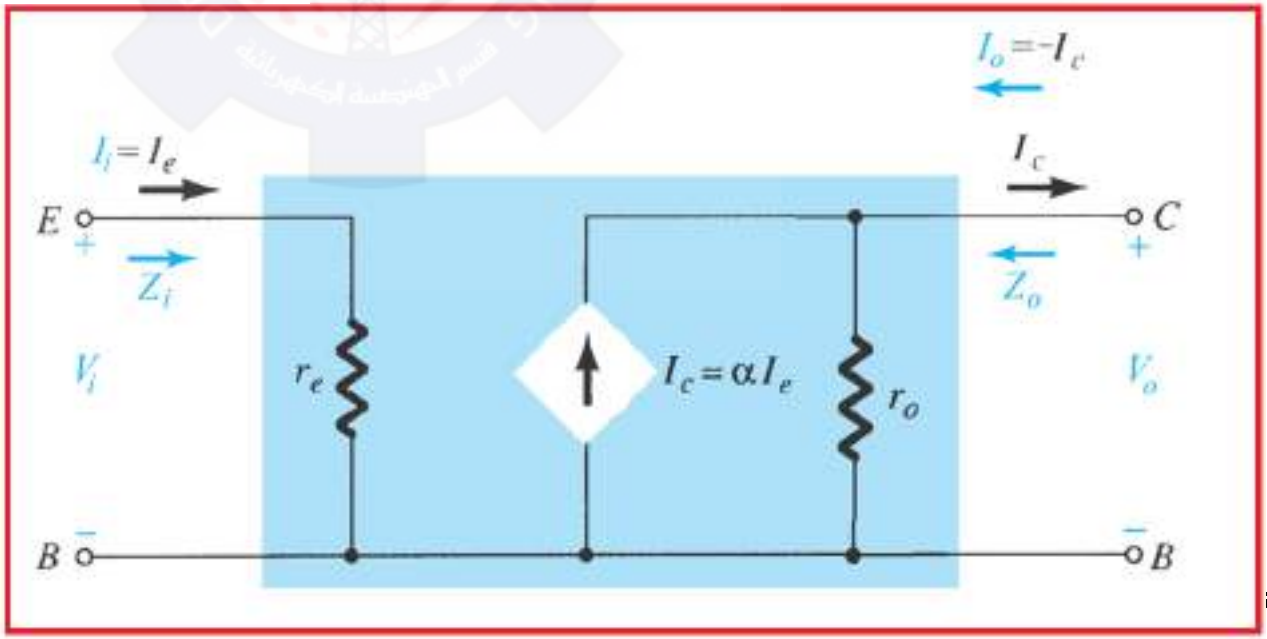
Common-Base Configuration



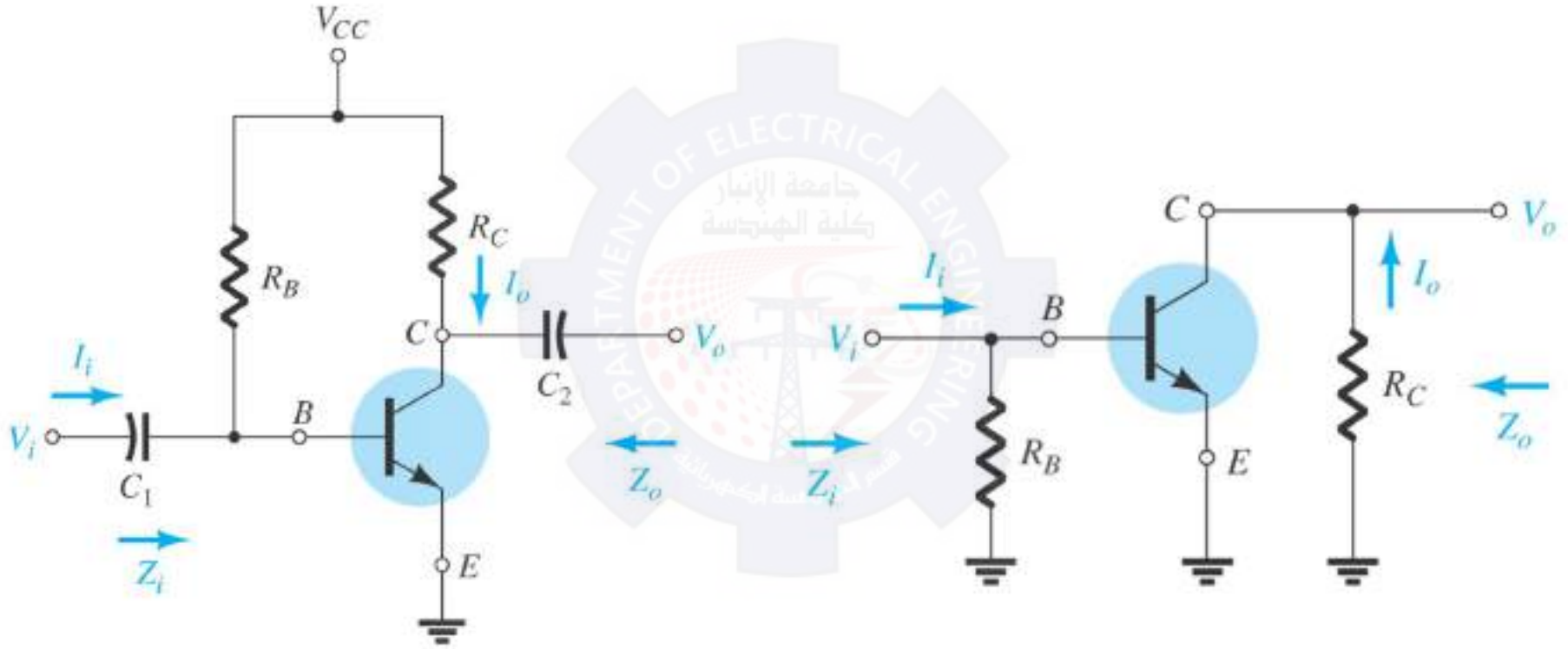


The output resistance r_o is quite high. typically extend into the megaohm range.

Common Base r_e equivalent circuit



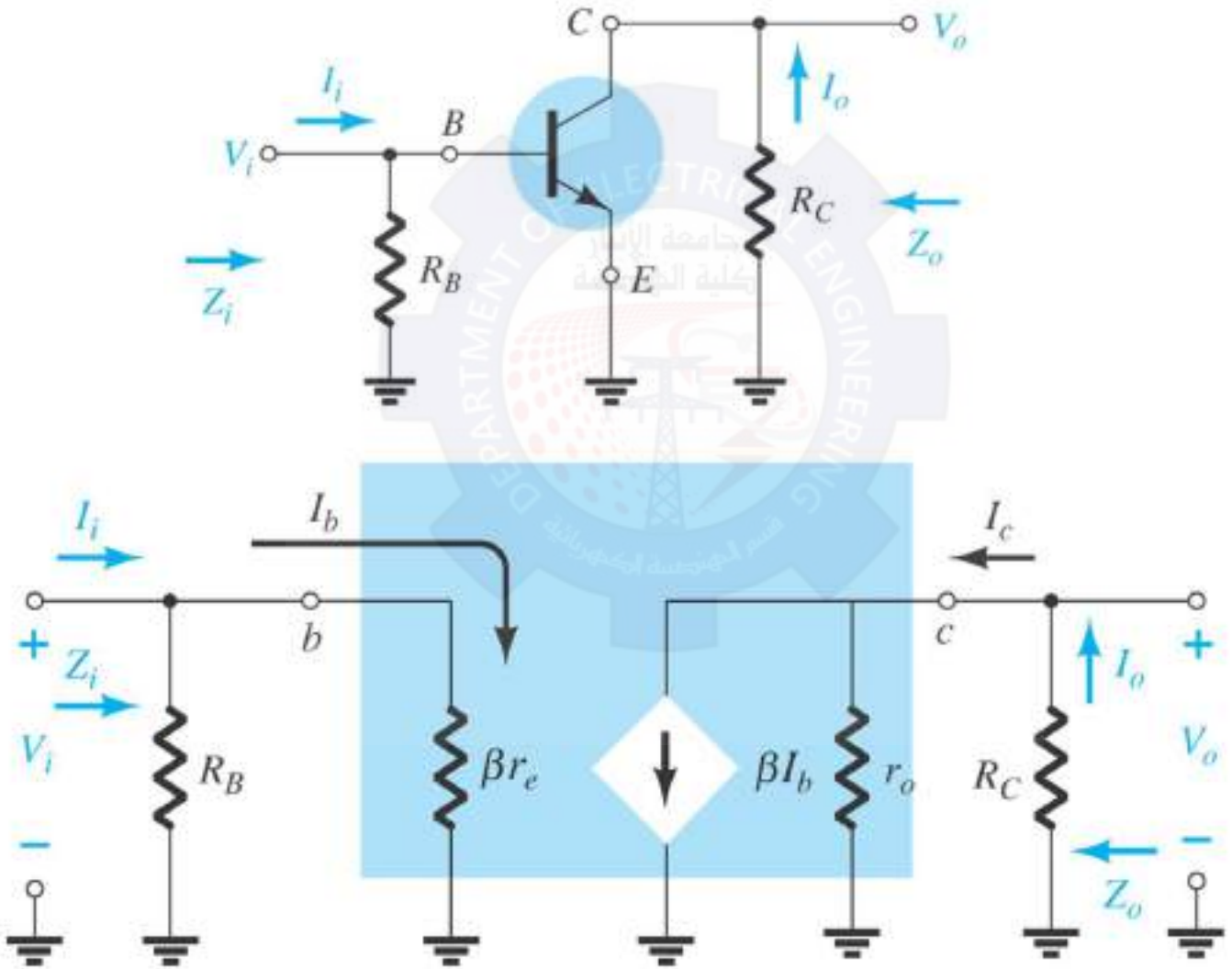
Common Emitter Fixed Bias Configuration



Common-emitter fixed-bias configuration.

Network after the removal of the effects of V_{CC}, C_1 and C_2.

Common Emitter Fixed Bias Configuration



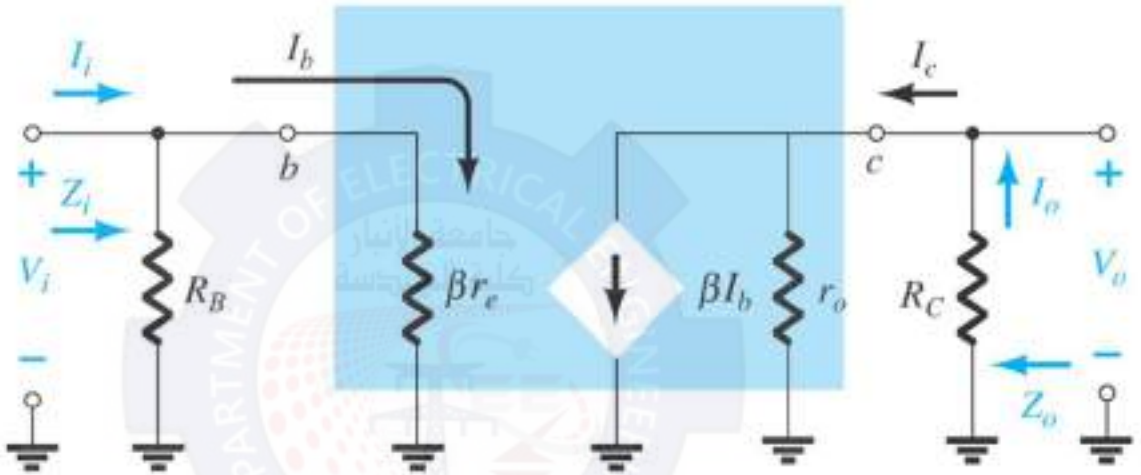
Substituting the r_e model into the network.

Common Emitter Fixed Bias Configuration

Input impedance:

$$Z_i = R_B \,||\, \beta r_e$$

$$Z_i \cong \beta r_e \Big| \; R_E \geq 10\beta r_e$$



Output impedance:

$$Z_o = R_C \,||\, r_O$$

$$Z_o \cong R_C \Big| \; r_o \geq 10R_C$$

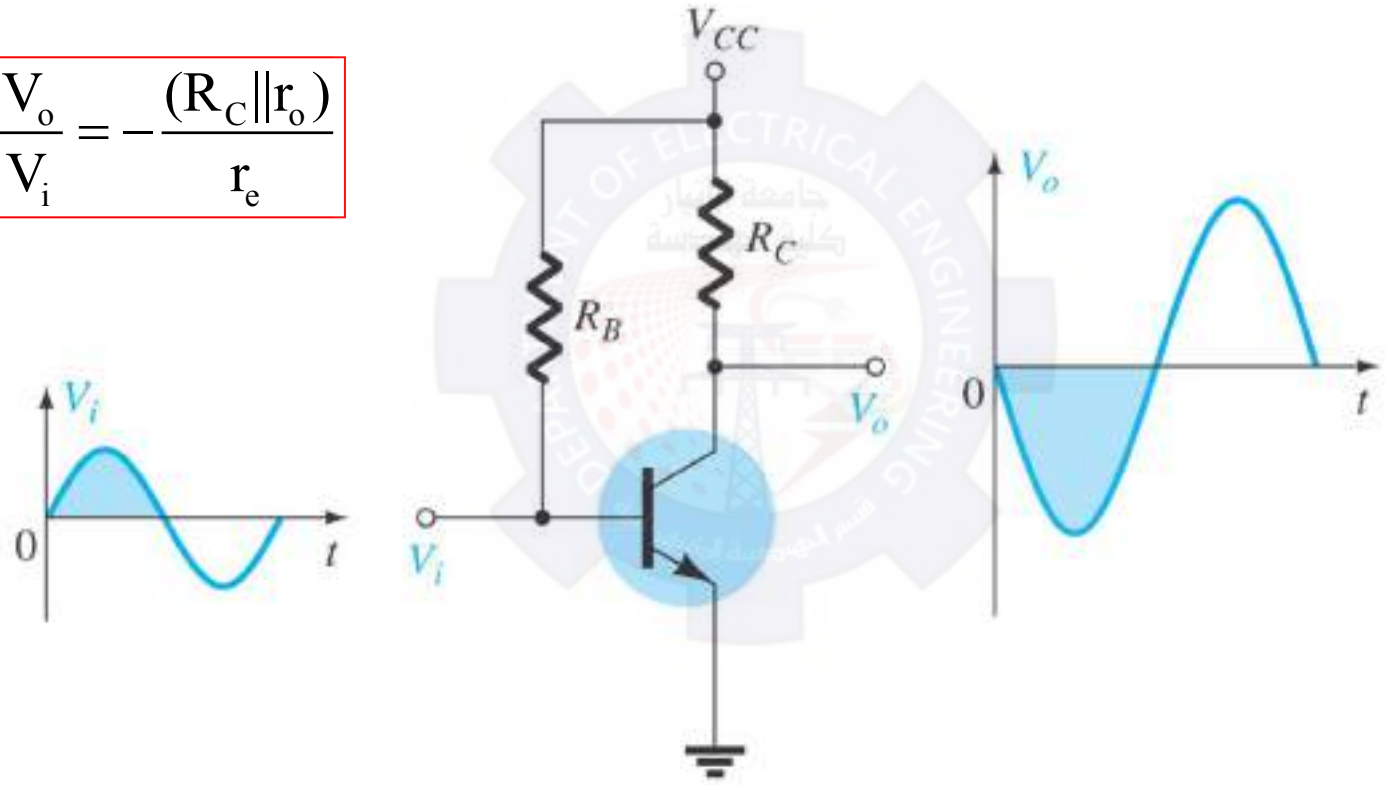
Voltage gain:

$$V_o = -\beta I_b (R_C || r_o) \;,\; I_b = \frac{V_i}{\beta r_e} \;,\; V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C || r_o)$$

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C || r_o)}{r_e} \quad , \quad A_v = -\frac{R_C}{r_e} \Big| \; r_o \geq 10R$$

Common Emitter Fixed Bias Configuration

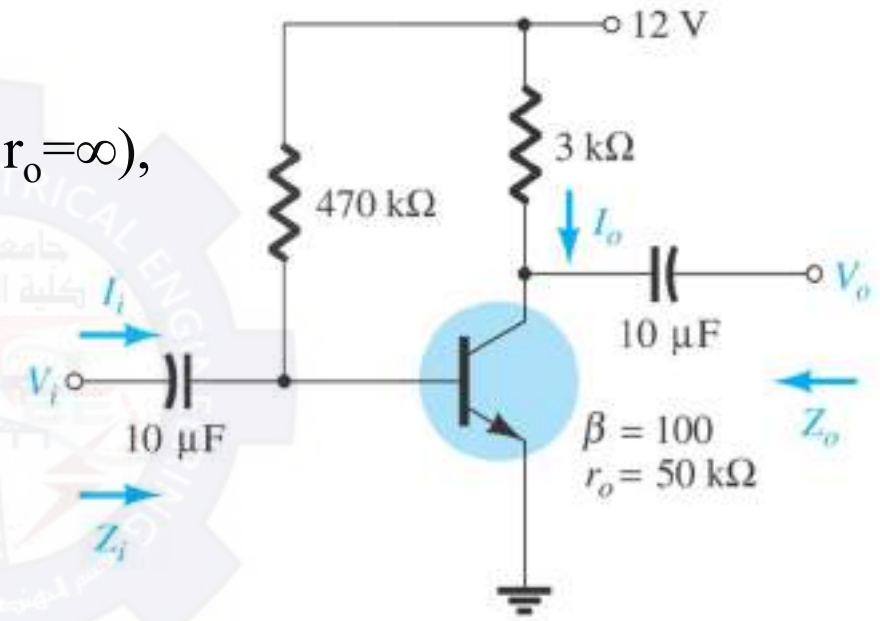
$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}$$



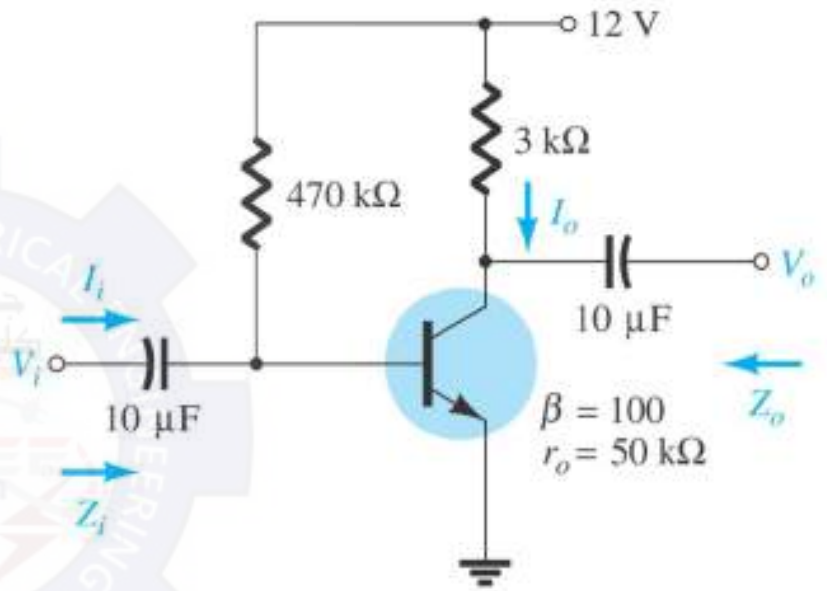
Demonstrating the 180° phase shift between input and output waveforms.

Example 5.1

Determine r_e, Z_i (with $r_o=\infty$), Z_o (with $r_o=\infty$), A_v (with $r_o=\infty$).
Repeat with $r_o=50$ kΩ.



Example 5.1 - Solution



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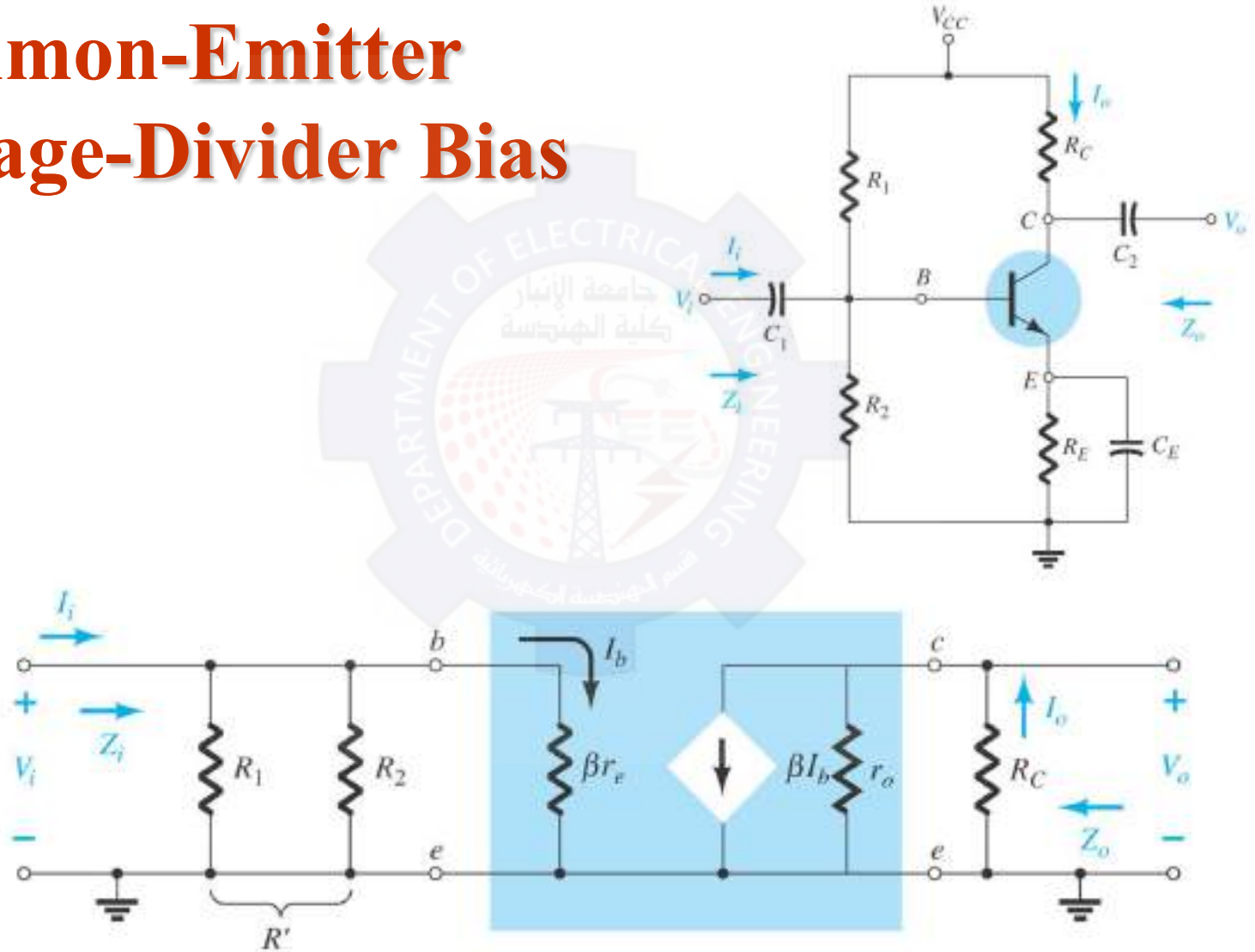
Common-Emitter Voltage-Divider Bias



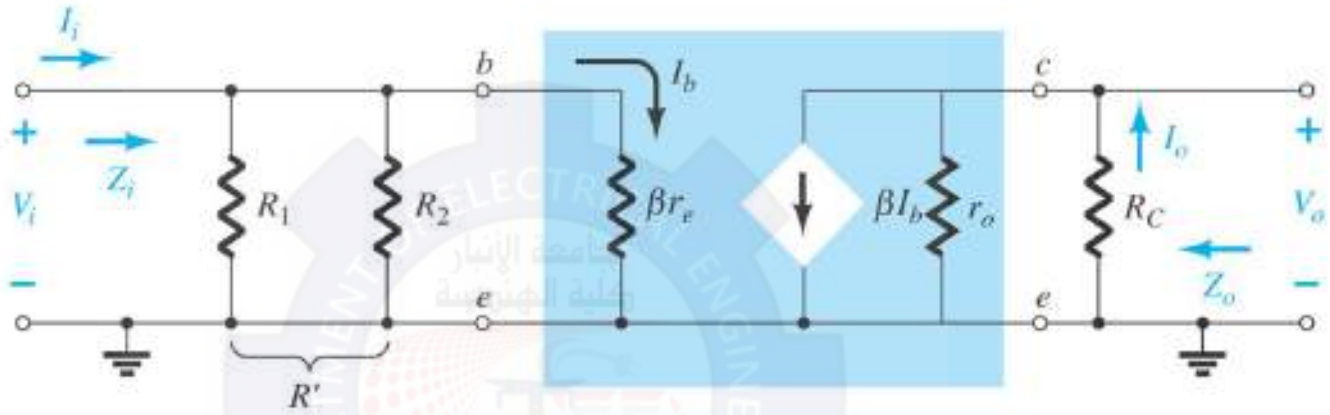
r_e model requires you to determine β, r_e, and r_o.

Common-Emitter Voltage-Divider Bias

Input impedance:

$$\mathbf{R' = R_1 \,||\, R_2}$$

$$\mathbf{Z_i = R' \,||\, \beta r_e}$$



Output impedance:

$$\mathbf{Z_o = R_C \,||\, r_o}$$

$$\mathbf{Z_o \cong R_C \big|_{r_o \geq 10R_C}}$$

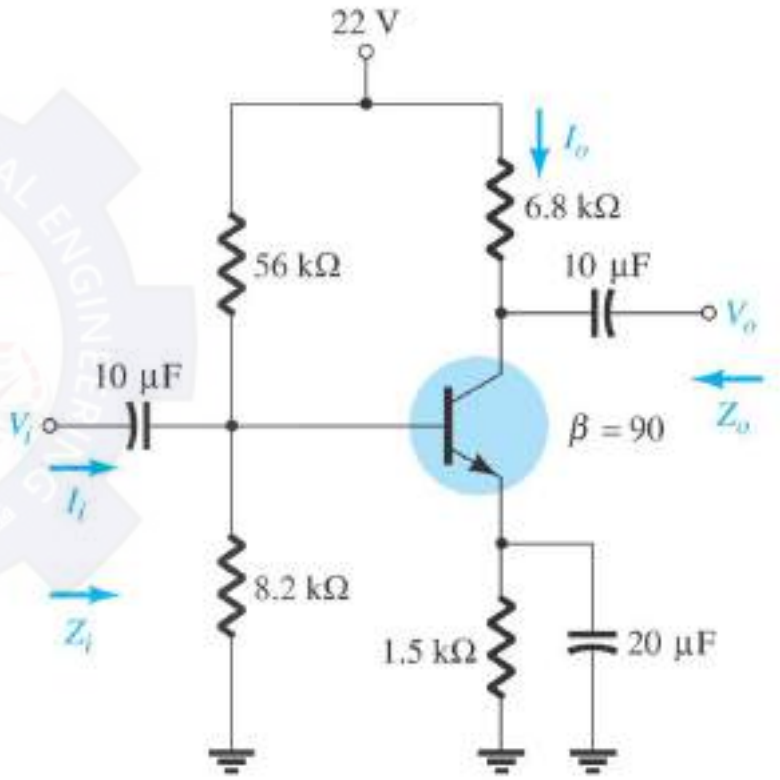
Voltage gain:

$$V_o = -\ I_b(R_C \| r_o)\ ,\ I\ = \frac{V_i}{r_e}\ ,\ V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

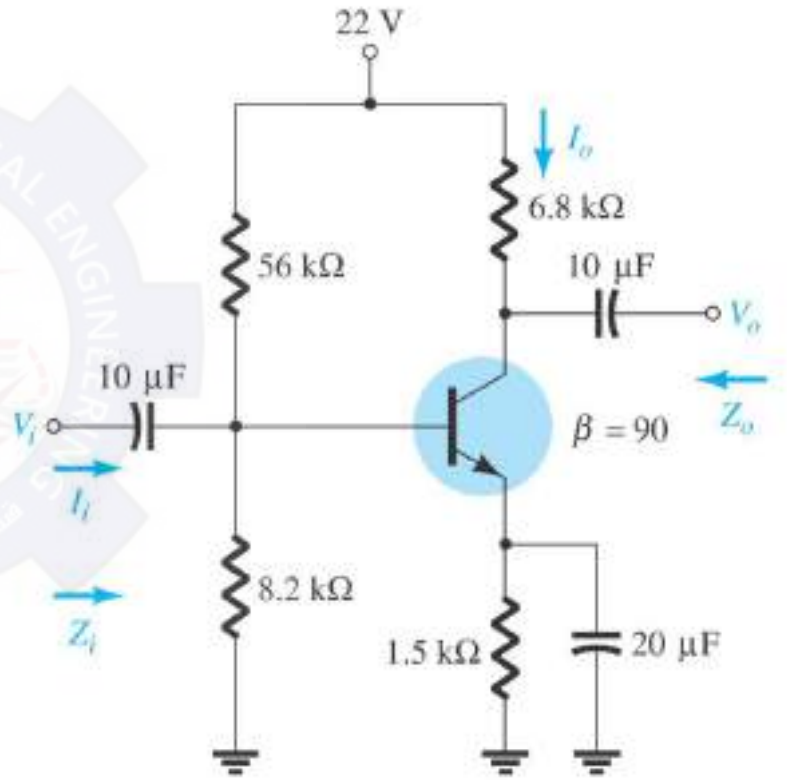
$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e} \quad , \quad A_v = -\frac{R_C}{r_e}\Big|_{r_o \geq 10R}$$

Example 5.2

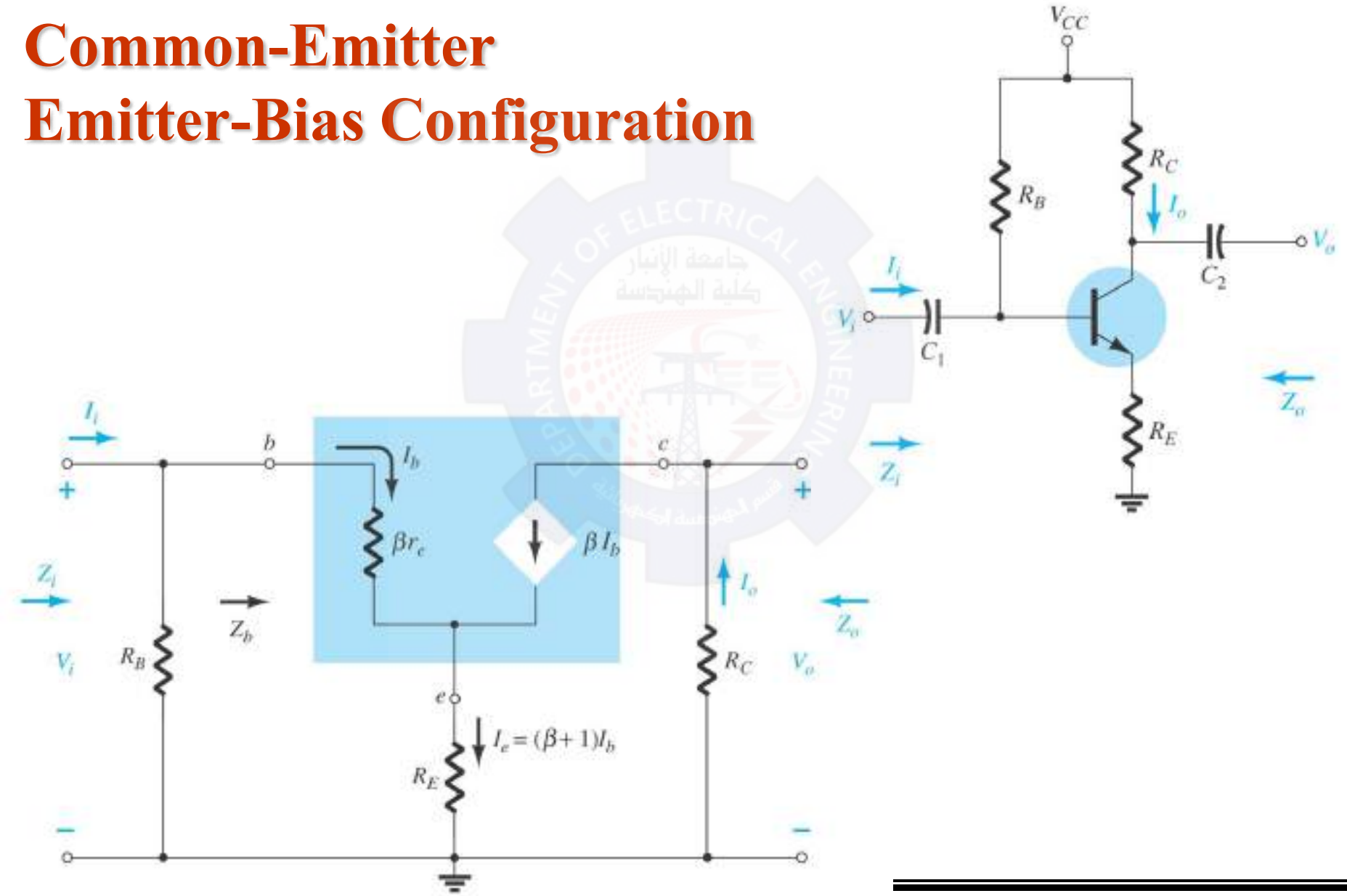
Determine r_e, Z_i , Z_o (with $r_o=\infty$), A_v (with $r_o=\infty$). Repeat with $r_o=50$ kΩ.



Example 5.2 - Solution



Common-Emitter
Emitter-Bias Configuration



Impedance Calculations

Input impedance:

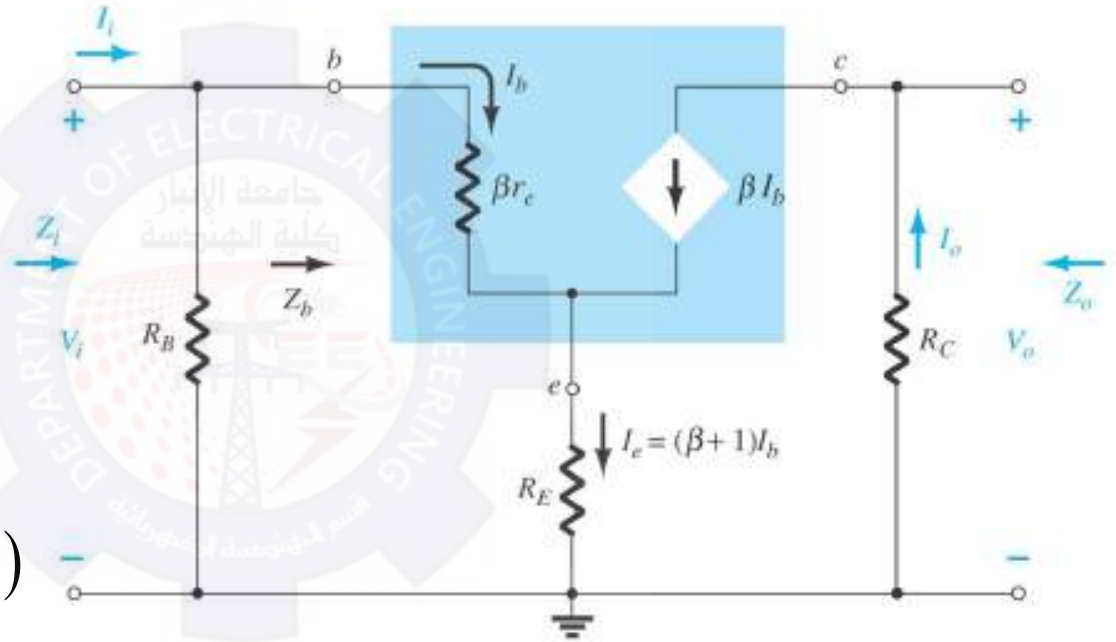
$$V_i = I_b \beta r_e + I_e R_E$$

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

$$Z_b \cong \beta r_e + \beta R_E = \beta (r_e + R_E)$$

$$Z_b \cong \beta R_E \quad \text{for } R_E >> r_e$$



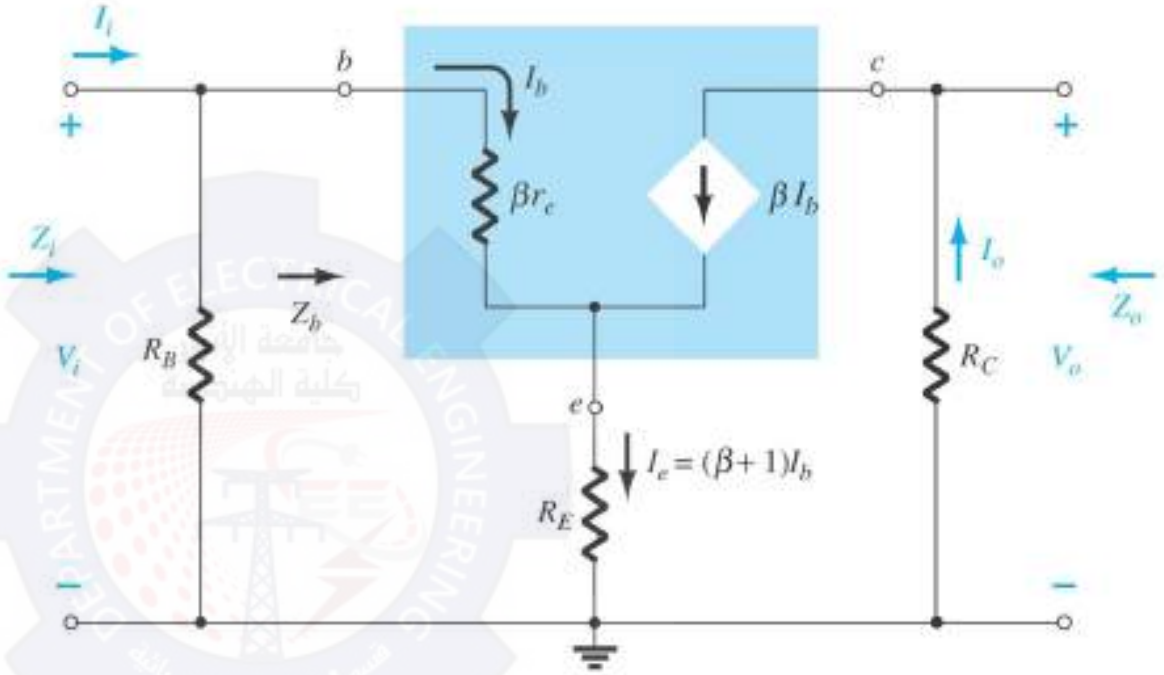
$$Z_i = R_B \| Z_b$$

Output impedance:

$$Z_o = R$$

Gain Calculations

Voltage gain:



$$V_o = -I_o R_C = -\beta I_b R_C$$

$$V_o = -\beta \left(\frac{V_i}{Z_b} \right) R_C$$

$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$$

substituting $Z_b \cong \beta(r_e + R_E)$

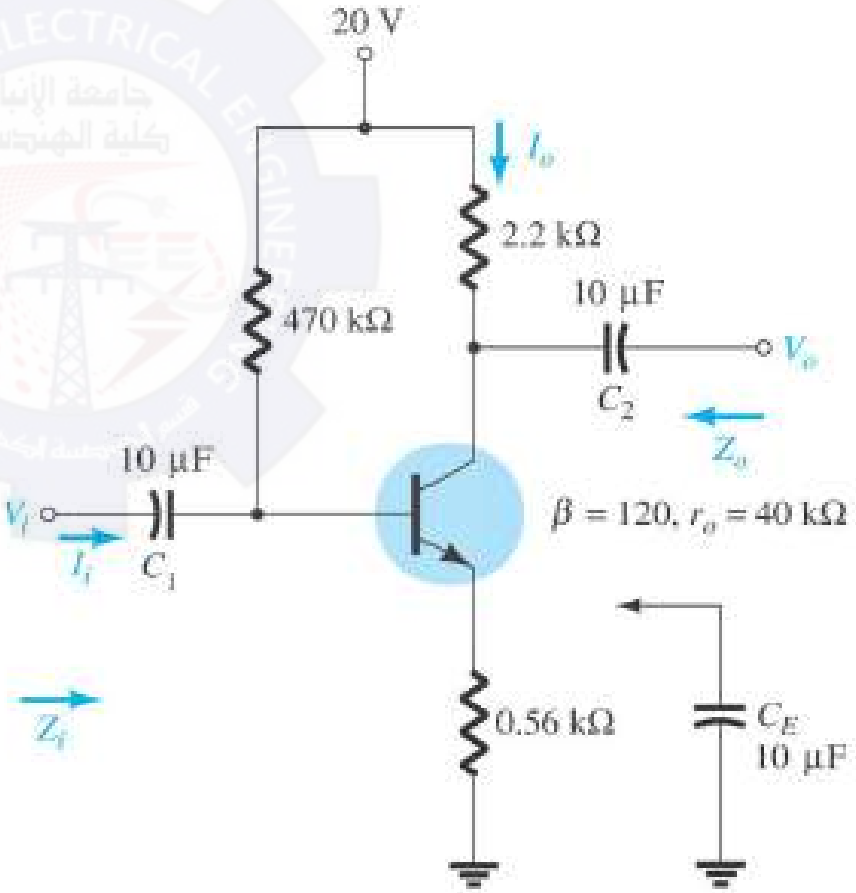
$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}$$

and for the approximation $Z_b \cong \beta R$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R}{R_E}$$

Example 5.3 Without C_E (unbypassed):

Determine r_e, Z_i , Z_o , A_v . ignore r_o for $r_o \geq 10(R_C+R_E)$



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Chapter05: BJT AC Analysis

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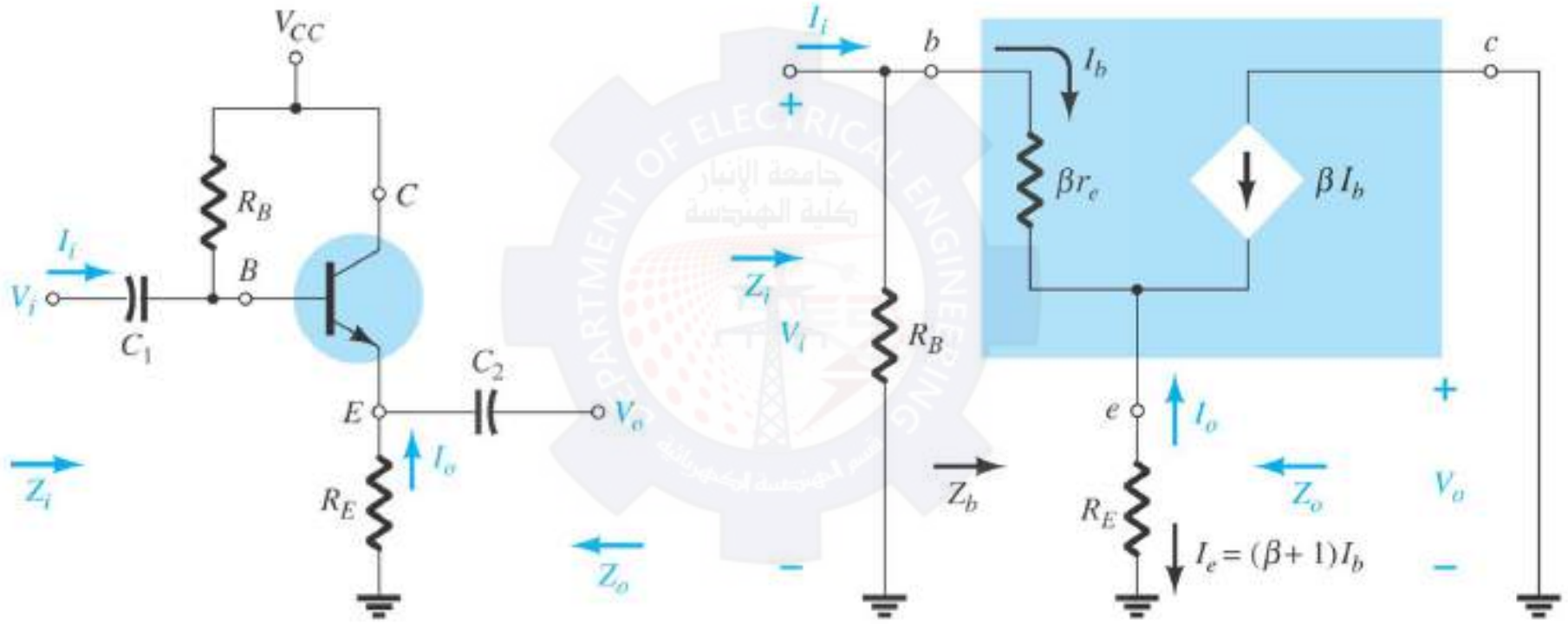
Emitter-Follower Configuration



- This is also known as the common-collector configuration.
- The input is applied to the base and the output is taken from the emitter.
- There is no phase shift between input and output.

Impedance Calculations

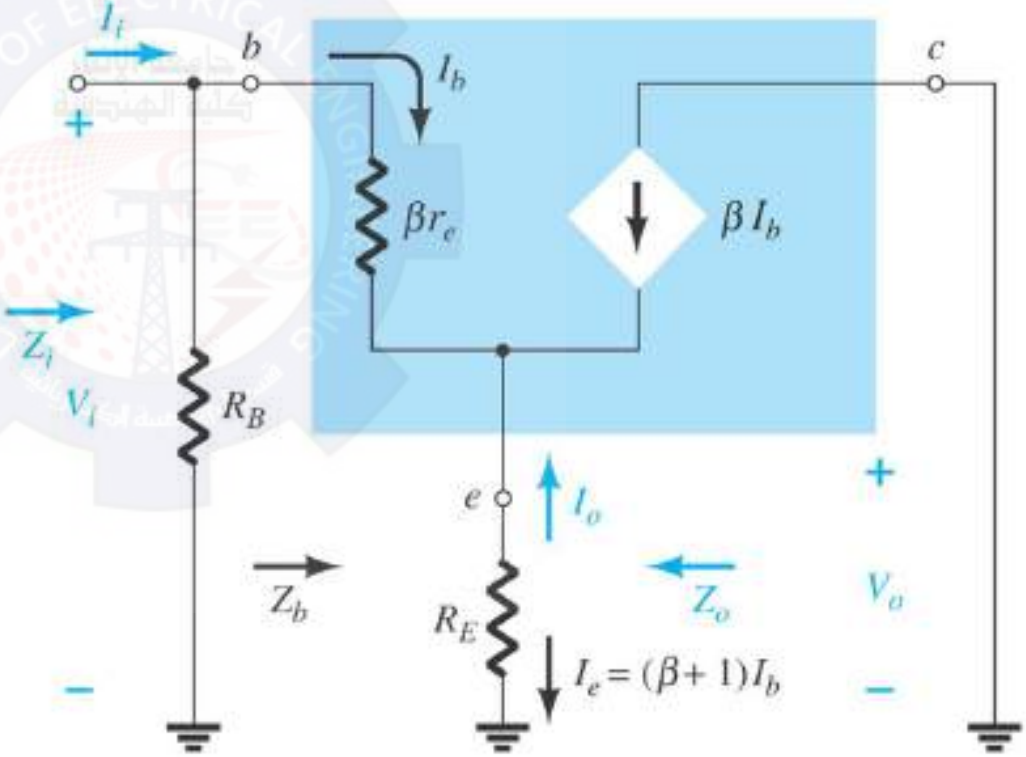
Input impedance:

$$Z_i = R_B \| Z_b$$

$$Z_b = \beta r_e + (\quad +1) R_E$$

$$Z_b \cong \beta (r_e \quad R_E)$$

$$Z_b \cong \beta R_E \quad (\text{for } R_E >> r_e)$$



Impedance Calculations

Output impedance:

$$I_b = \frac{V_i}{Z_b} \quad , \mathrm{I_e} = (\beta+1)\mathrm{I_b}$$

$$= (\beta+1)\frac{V_i}{Z_b}$$

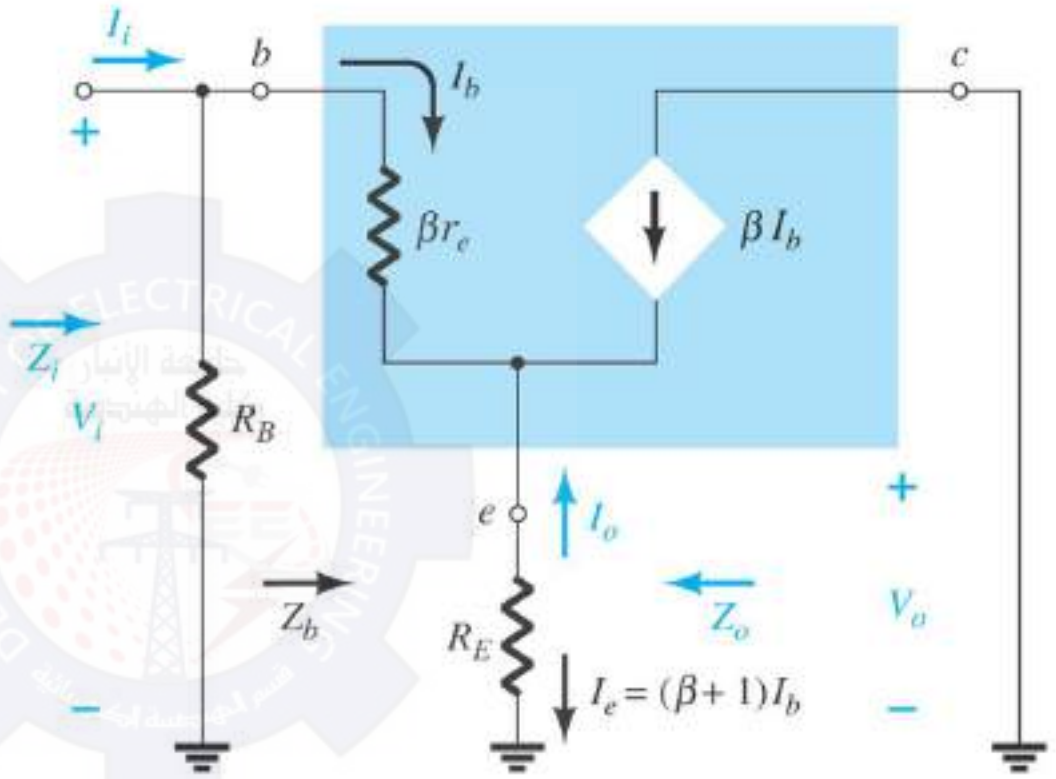
$$I_e = \frac{(\beta+1)V_i}{\beta r_e + (\beta+1)R_E}$$

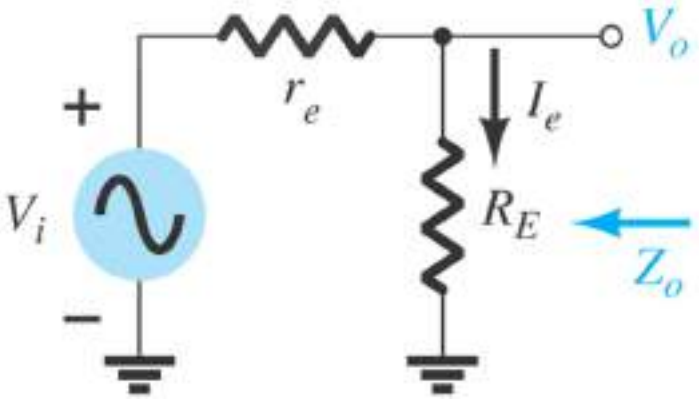
$$\text{since } (\beta+1) \cong \beta$$

$$I_e = \frac{V_i}{r_e + R}$$

To determine $\mathrm{Z_o}$, V_i is set to zero

$$\mathrm{Z_o = R_E \| r_e} \quad , \quad \mathrm{Z_o} \quad \mathrm{r_e} \Big|_{\mathrm{R_E >> r_e}}$$





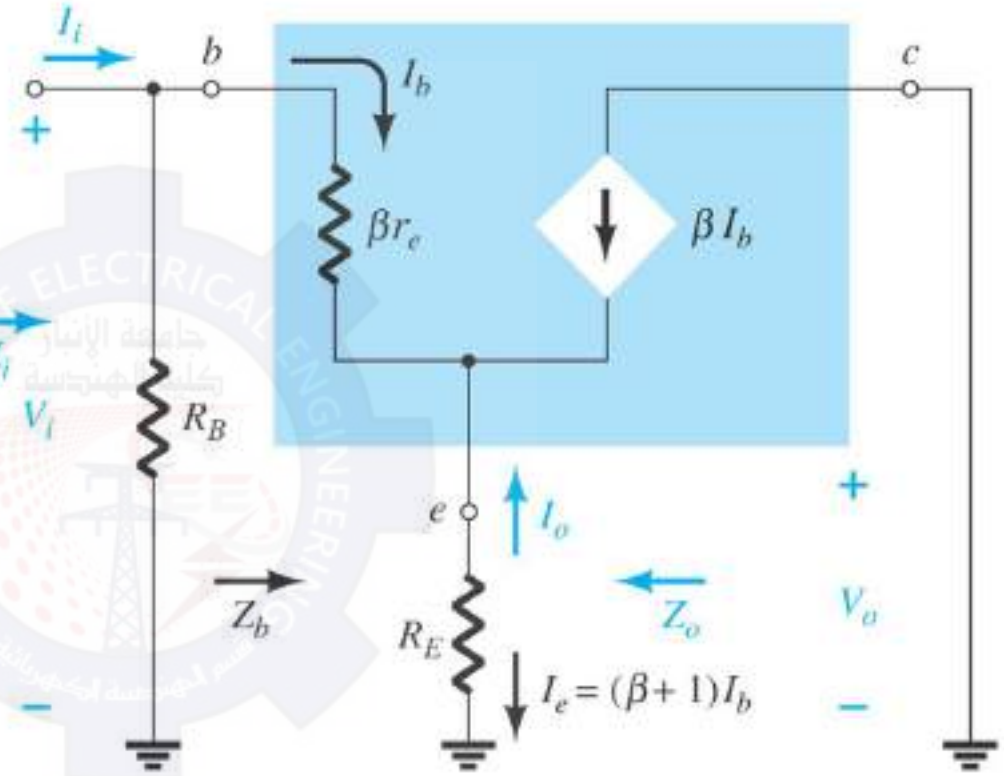
Gain Calculations

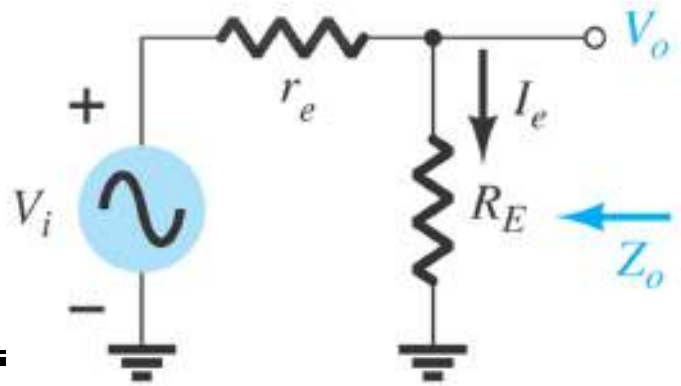
Voltage gain:

$$V_o = \frac{R_E}{R_E + r_e} V_i$$

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

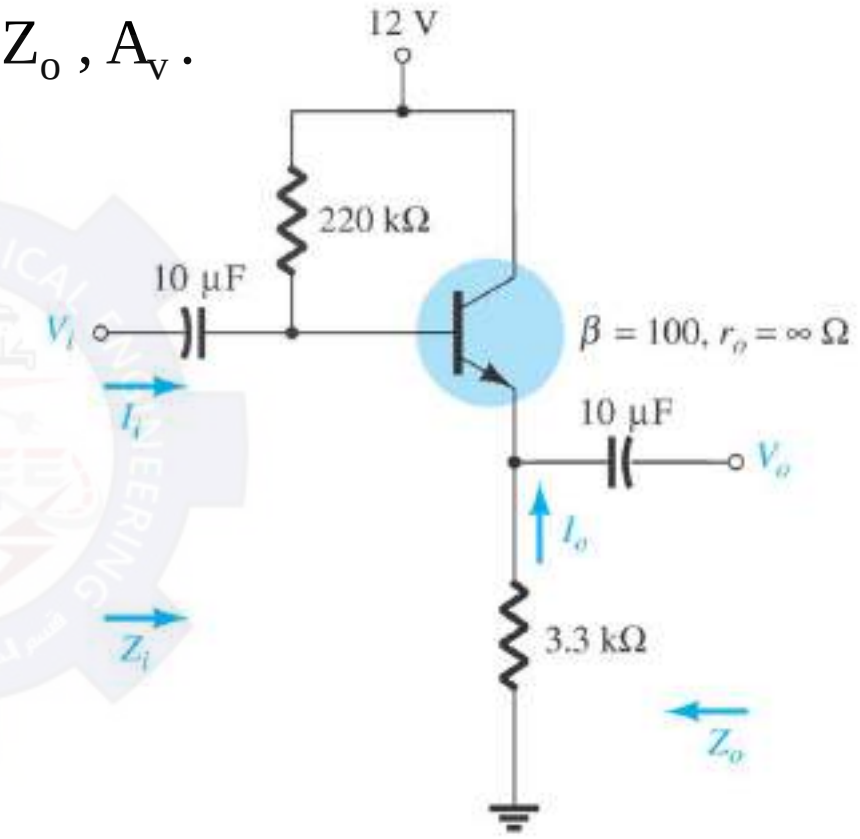
$$A_v \quad \frac{V_o}{V_i} \cong 1 \Big| \quad R_E >> r_e,\ R_E + r_e \cong R_E$$



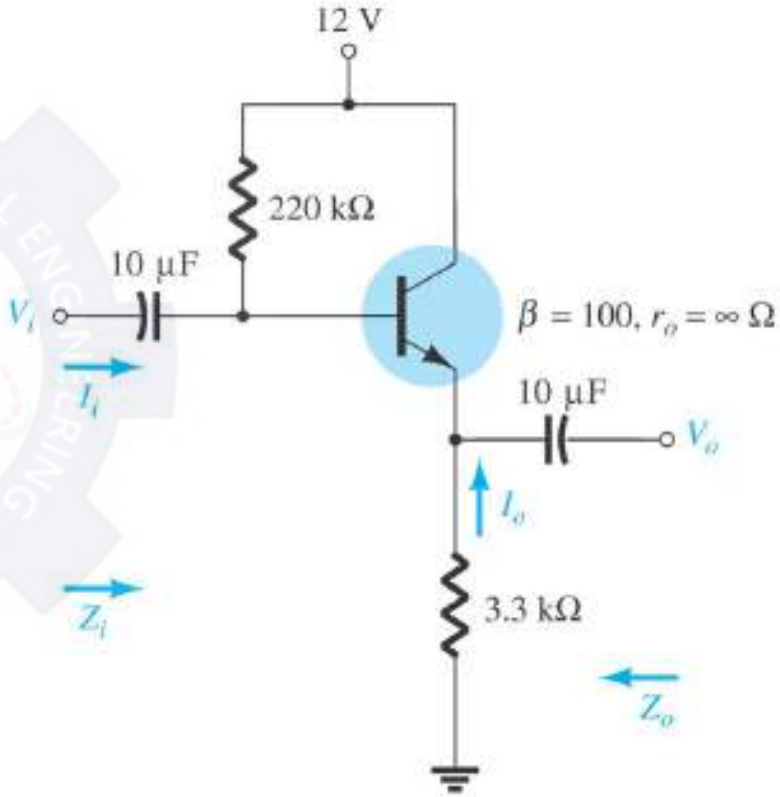


Example 5.7

Determine r_e, Z_i , Z_o , A_v .



Example 5.7 - solution



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Chapter05: BJT AC Analysis

Lec05_p4

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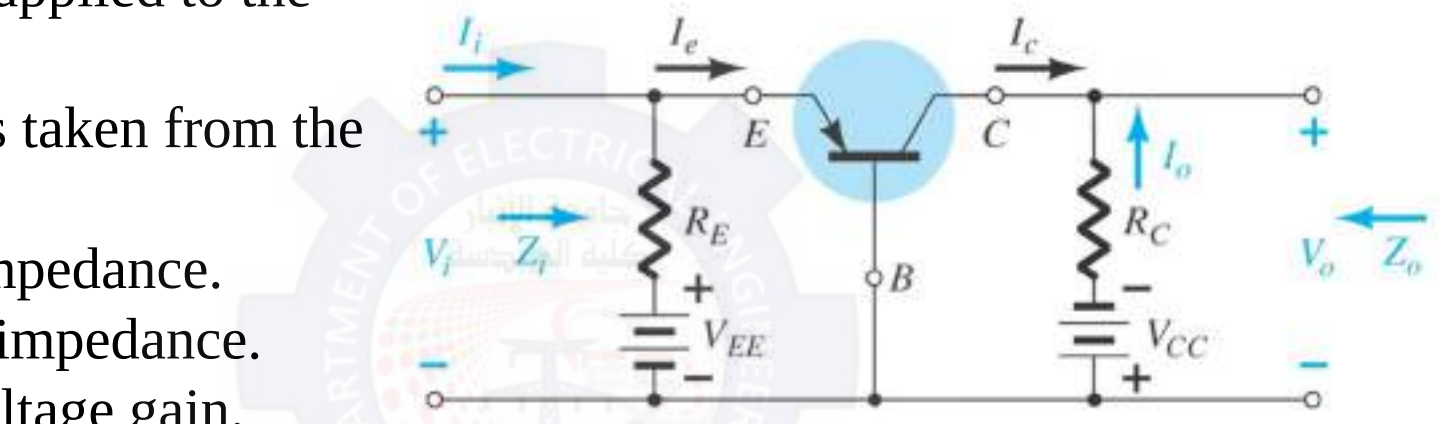
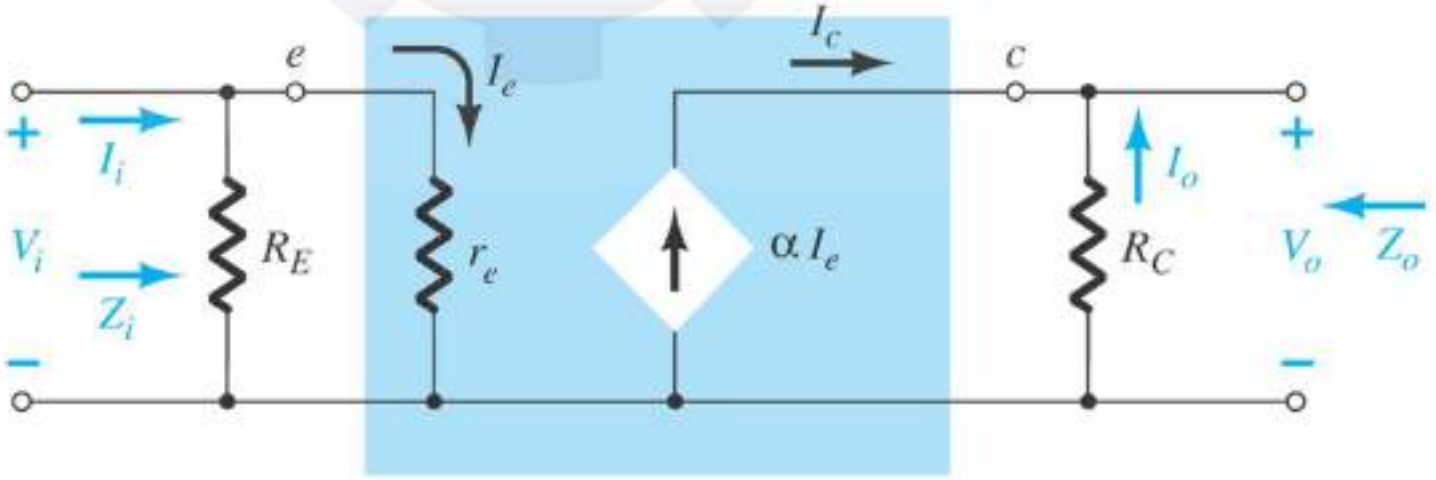
Common-Base Configuration

- The input is applied to the emitter.
- The output is taken from the collector.
- Low input impedance.
- High output impedance.
- Very high voltage gain.
- No phase shift between input and output.





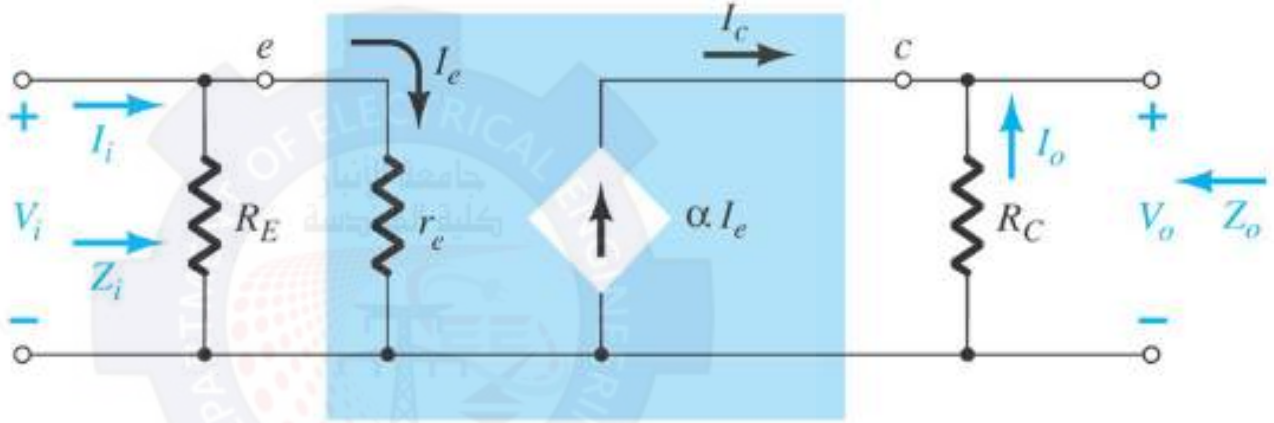
Calculations

Input impedance:

$$\mathbf{Z_i = R_E \,||\, r_e}$$

Output impedance:

$$\mathbf{Z_o = R_C}$$



Voltage gain:

$$V_o = -I_o R_C = -(-I_C)R_C$$
$$= \alpha I_e R_C$$

$$I_e = \frac{V_i}{e} \rightarrow V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

A_v positive… V_i and V_o in phase.

Current gain:

Assuming $R_E >> r_e$

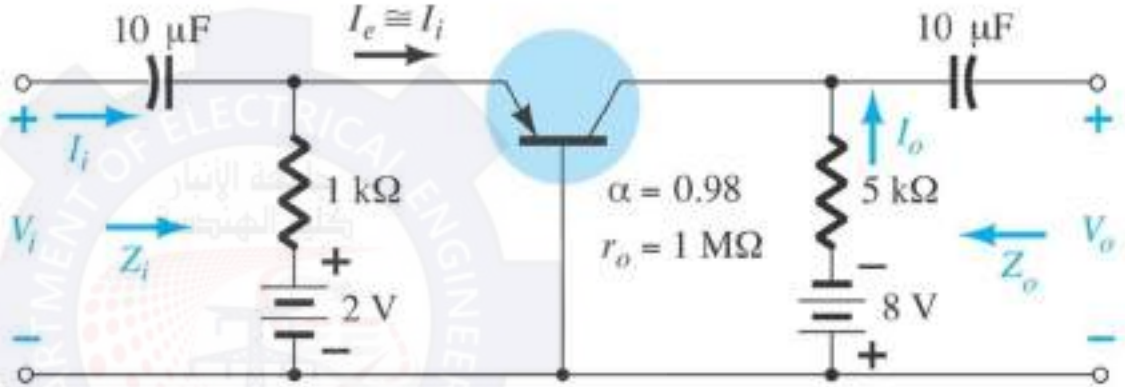
$$I_e = I_i$$

$$I_o = - \quad I_e = -\alpha I_i$$

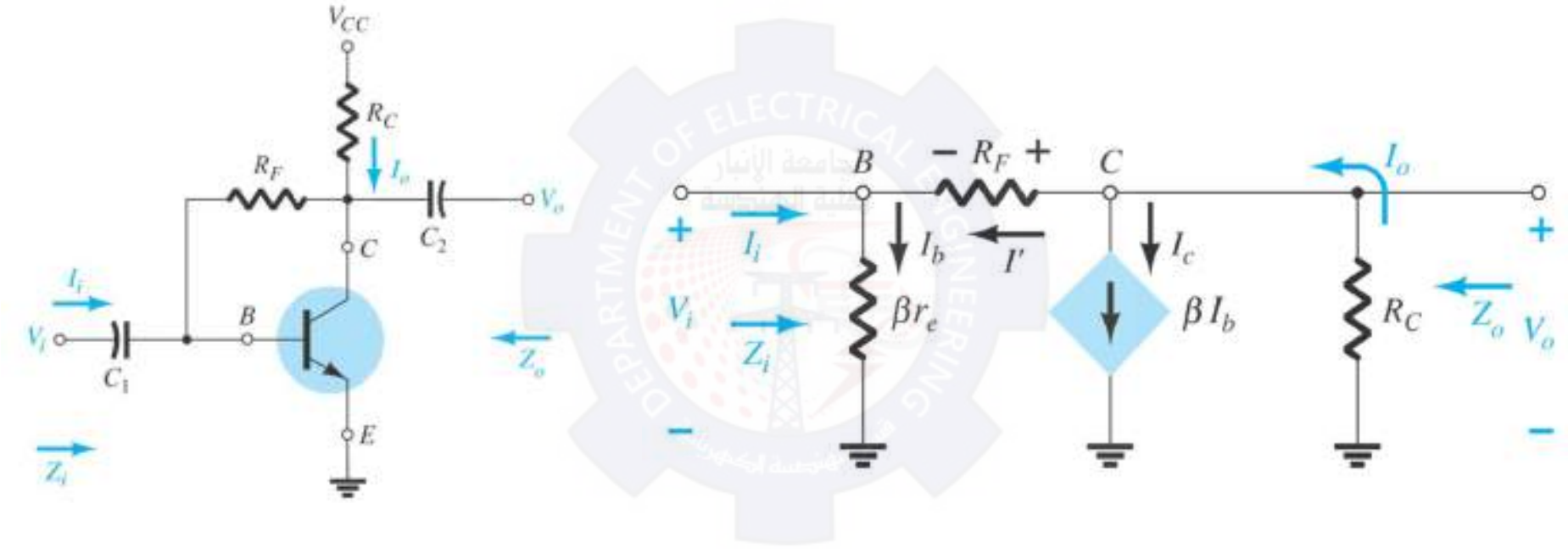
$$A_i = \frac{I_o}{I_i} = -\alpha \cong -$$

Example 5.8

Determine r_e, Z_i , Z_o , A_v , A_i



Common-Emitter Collector Feedback Configuration



- **This is a variation of the common-emitter fixed-bias configuration**
- **Input is applied to the base**
- **Output is taken from the collector**
- **There is a 180° phase shift between input and output**

Calculations

Output impedance:

$$Z_o \cong R_C \| R_F$$

Voltage gain:

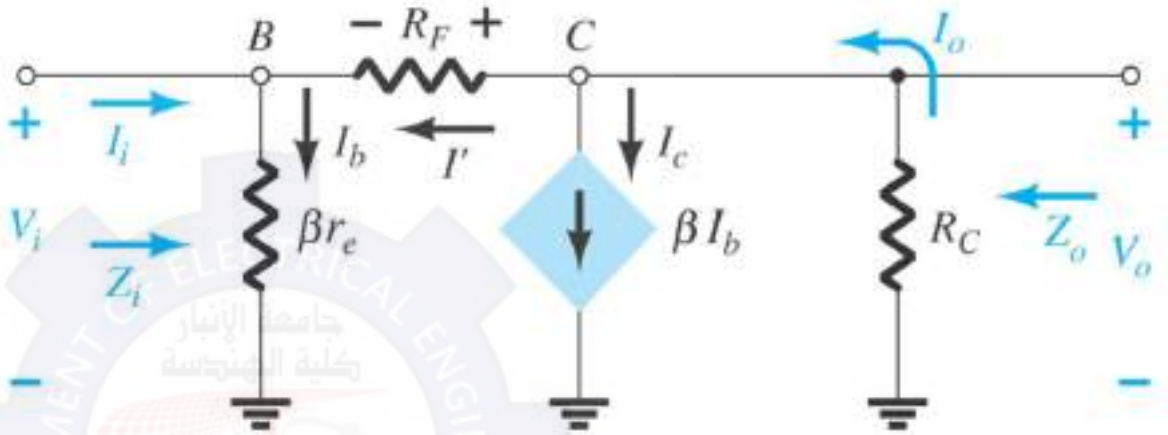
$$I_o = \beta I_b + I'$$

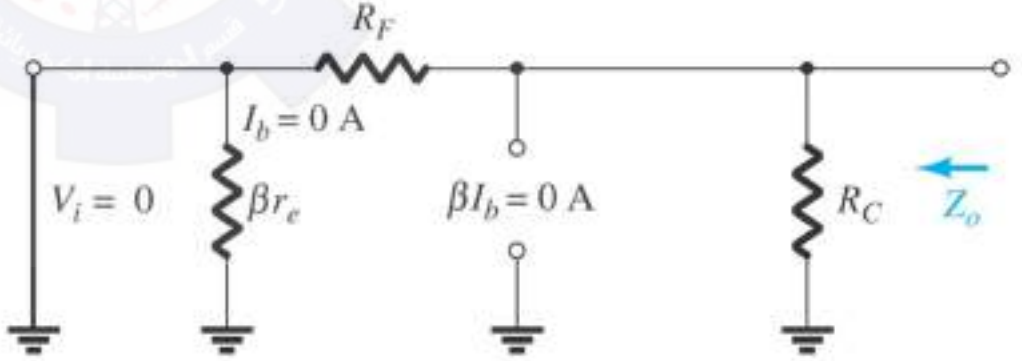
$$For\ \beta I_b >> I' \rightarrow I_o \cong \beta I_b$$

$$V_o = -I_o R_C = -(\beta I_b) R_C$$

$$I_b = \frac{V_i}{\beta r_e} \rightarrow V_o = -\beta \frac{V}{\beta r_e} R_C$$

$$A_v = \frac{V_o}{V_i} = -\frac{R}{r_e}$$





Defining Z_o

Calculations

Input impedance:

$$Z_i = \frac{V_i}{I_i}, \quad V_o = -\frac{V_i}{r_e} R_C$$

$$I' = \frac{V_o - V_i}{R_F} = \frac{V_o}{R_F} - \frac{V_i}{R_F} = -\frac{R_C V_i}{r_e R_F} - \frac{V_i}{R_F} = -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] V_i$$

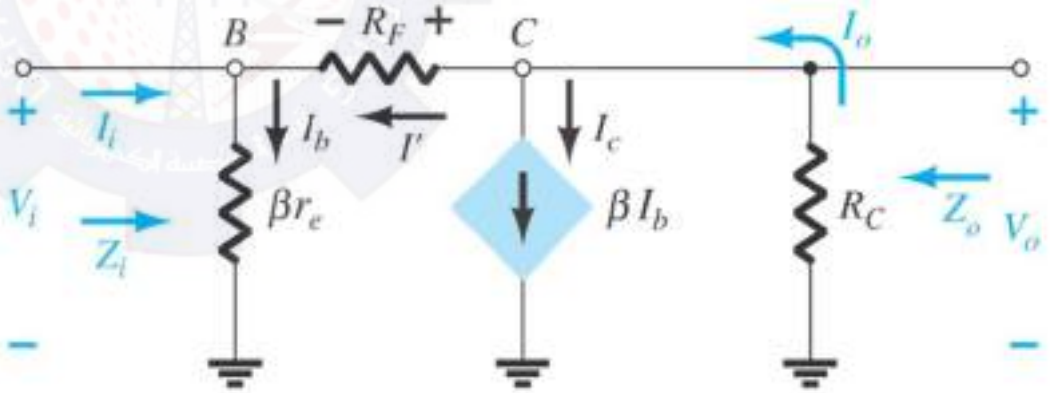
$$V_i = I_b \beta r_e = (I_i + I')\beta r_e = I_i \beta r_e + I' \beta r_e$$

$$V_i = I_i \beta r_e - \frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] \beta r_e V_i$$

$$or \quad V_i\left[1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]\right] = I_i \beta r_e$$

$$Z_i = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]}$$

$$1 + \frac{R_C}{r_e} \cong \frac{R_C}{r_e} \rightarrow Z_i = \frac{\beta r_e}{1 + \frac{\beta R_C}{R_F}}$$



$$\mathbf{Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$$

Determining the current gain using the voltage gain

$$\text{Current Gain } A_i = \frac{I_o}{I_i} \quad , \quad I_i = \frac{V_i}{Z_i} \quad , \quad I_o = -\frac{V_o}{R_L}$$

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\frac{V_o}{R_L}}{\frac{V_i}{Z_i}} = -\frac{V_o}{V_i}.\frac{Z_i}{R_L}$$

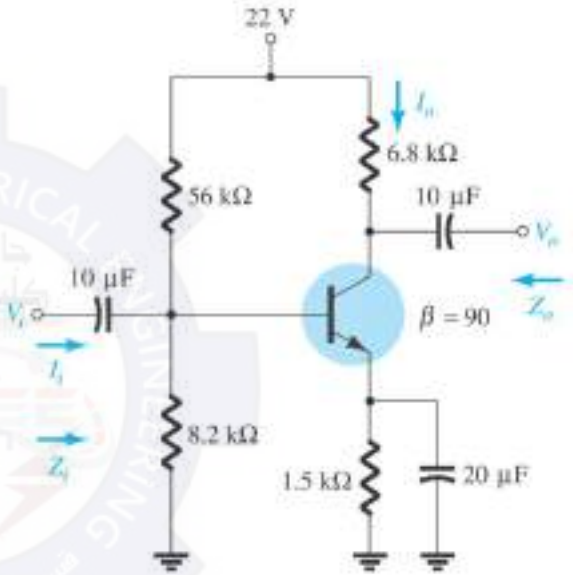
$$A_i = -A_{v_L}\frac{Z_i}{R_L}$$

Determining the current gain using the voltage gain

From example 5.2

Z_i=1.35 kΩ.

A_v=-368.76

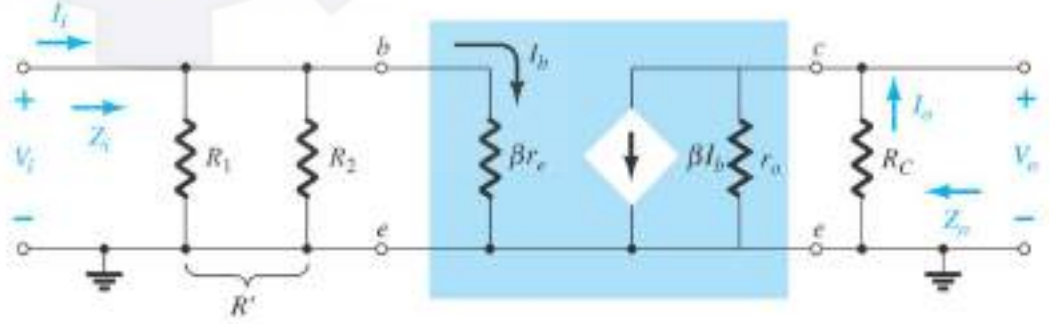


Current Gain $A_i = \dfrac{I_o}{I_i}$,

$$I_i = \frac{V_i}{1.35k} \quad , \quad I_o = -\frac{V_o}{6.8k}$$

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\dfrac{V_o}{6.8k}}{\dfrac{V_i}{1.35k}} = -\frac{V_o}{V_i}.\frac{1.35k}{6.8k}$$

$$= -(-368.76)\frac{1.35k}{6.8k} = 73.2$$



or $A_i = -A_{v_L}\dfrac{Z_i}{R_L} = -(-368.76)\dfrac{1.35k}{6.8k} = 73.2$

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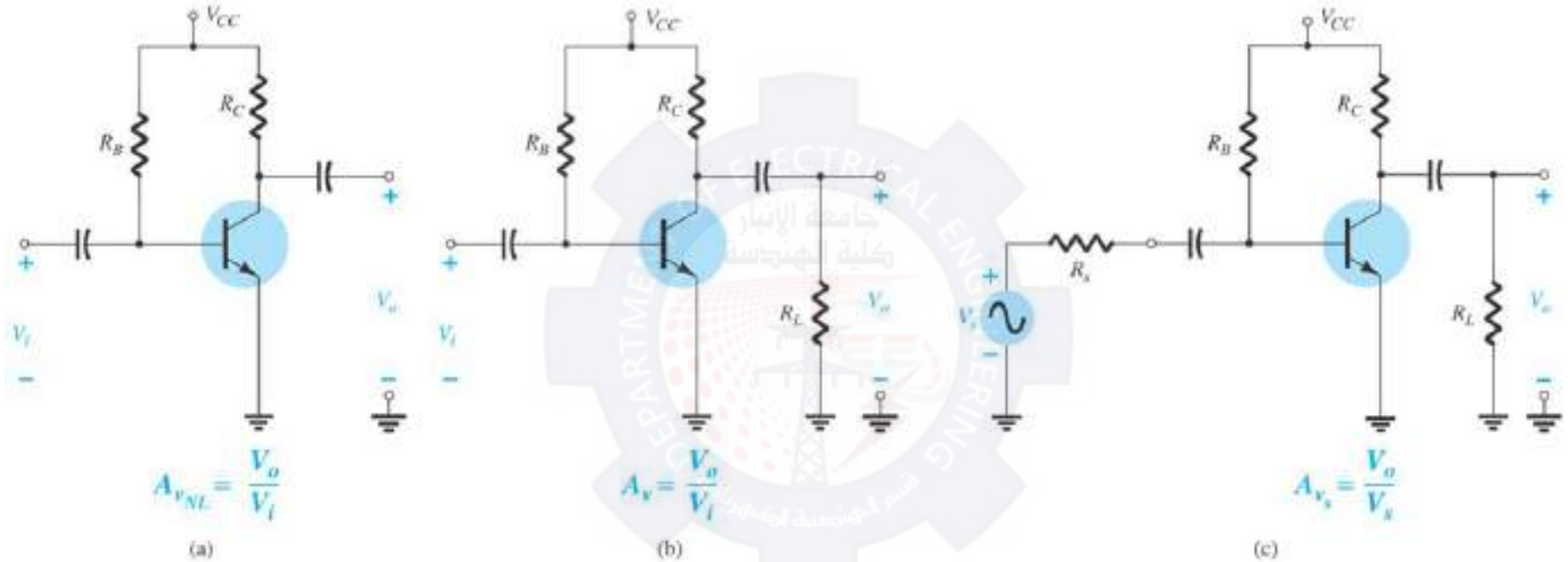
Chapter05: BJT AC Analysis

Lec05_p5

Munther N. Thiyab

2019-2020

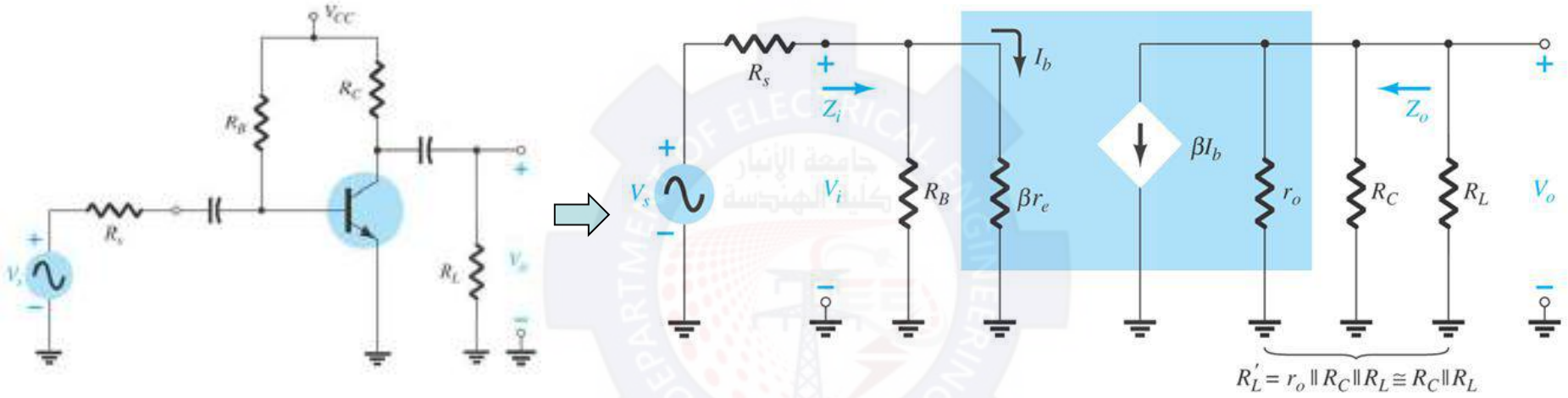
Effect of R_L and R_S



$$A_{vNL} \quad \frac{V}{V_i} \qquad , \qquad A_{vL} = \frac{V_o}{V_i} \ , \ \text{with } R_L$$

$$A_{vS} = \frac{V_o}{V_s} \ , \ \text{with } R_L \ \text{and } R_S$$

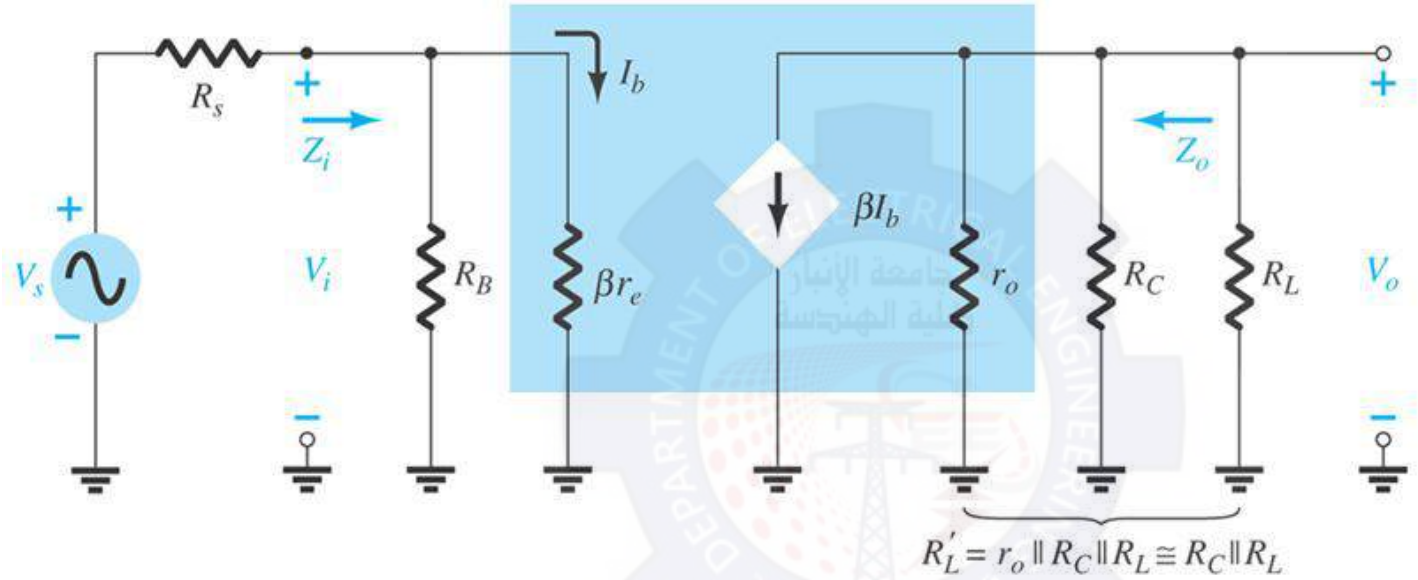
Effect of R_L and R_S



$$V_o = -\beta I_b (R_C \| r_o \| R_L) = -\beta I_b (R_C \| R_L), \quad I_b = \frac{V_i}{\beta r_e},$$

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| R_L) \Rightarrow A_{vL} = \frac{V}{V_i} = -\frac{(R_C \| R_L)}{r_e}$$

Effect of R_L and R_S



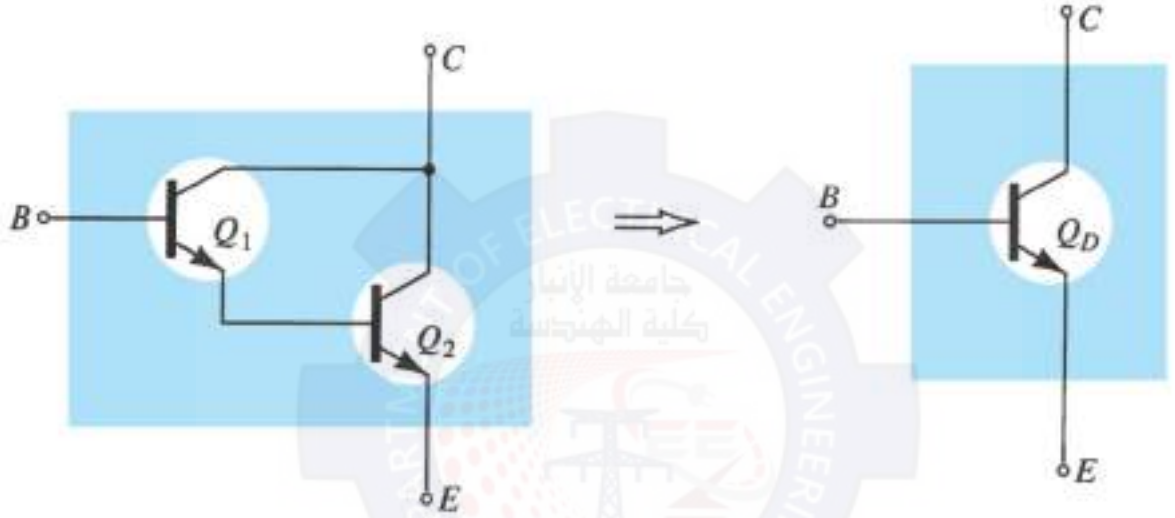
Input impedance: $Z_i = R_B \| \beta r_e$

Output Impedance: $Z_o = R_C \| r_o$

To find overall gain: $V_i = \dfrac{Z_i V_s}{Z_i + R_s}$, $\dfrac{V_i}{V_S} = \dfrac{Z_i}{Z_i + R_s}$

$$A_{vS} = \frac{V_o}{V_S} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_S} = A_{vL} \frac{Z_i}{Z_i + R_s} \quad \Rightarrow A_{vS} = \frac{Z_i}{Z_i + R_s} A_{vL}$$

Darlington Connection



- The Darlington circuit provides a very high current gain—the product of the individual current gains: $\beta_D = \beta_1\beta_2$
- A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand.
- Darlington pairs are available as complete packages.
- A Darlington pair is sufficiently sensitive to respond to the small current.

DC Bias of Darlington Circuits

Base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

Emitter current:

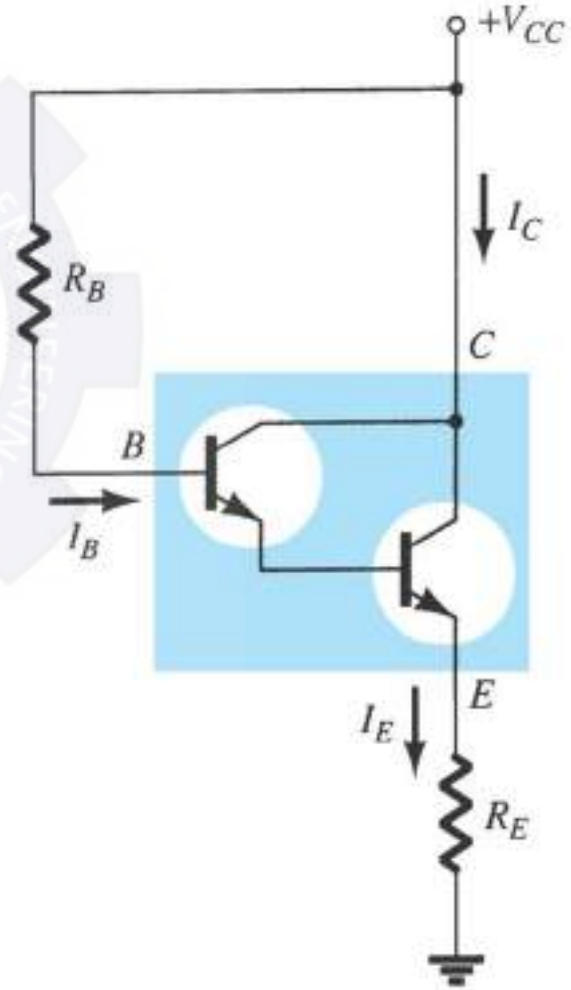
$$I_E = (\beta_D + 1) I_B \cong \beta_D I_B$$

Emitter voltage:

$$V_E = I_E R_E$$

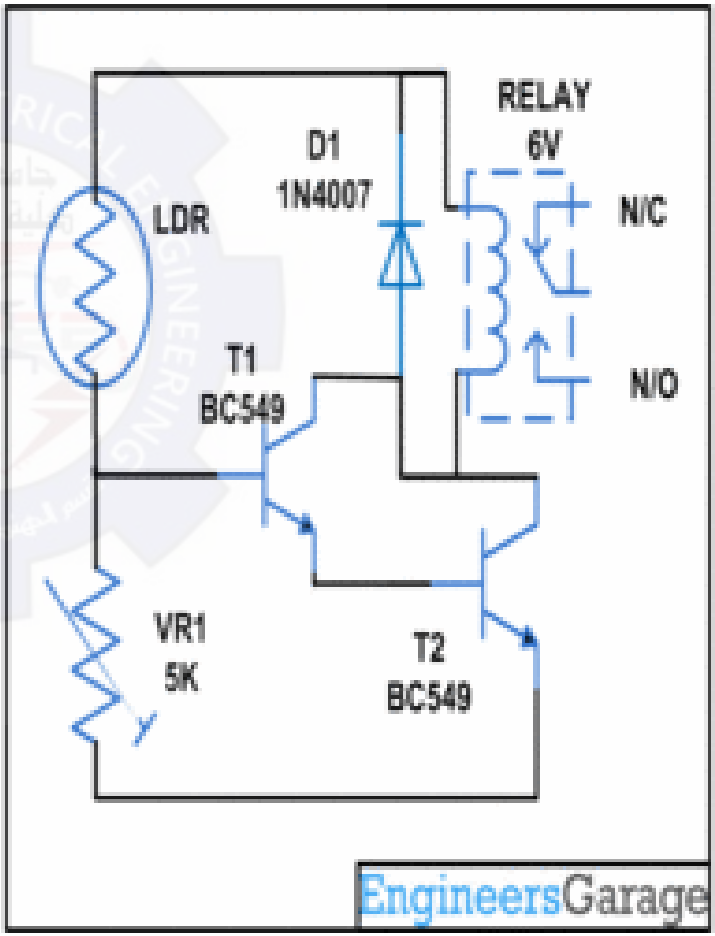
Base voltage:

$$V_B = V_E + V_{BE}$$



Darlington Circuits

- When light falls on the LDR, its resistance reduces.
- The bias voltage is supplied to the transistor and this voltage is enough to make the transistor and relay work.
- A variable resistor is also connected on the base of transistor to adjust the sensitivity.



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Chapter 6 : Field Effect Transistors
Lec06_p1

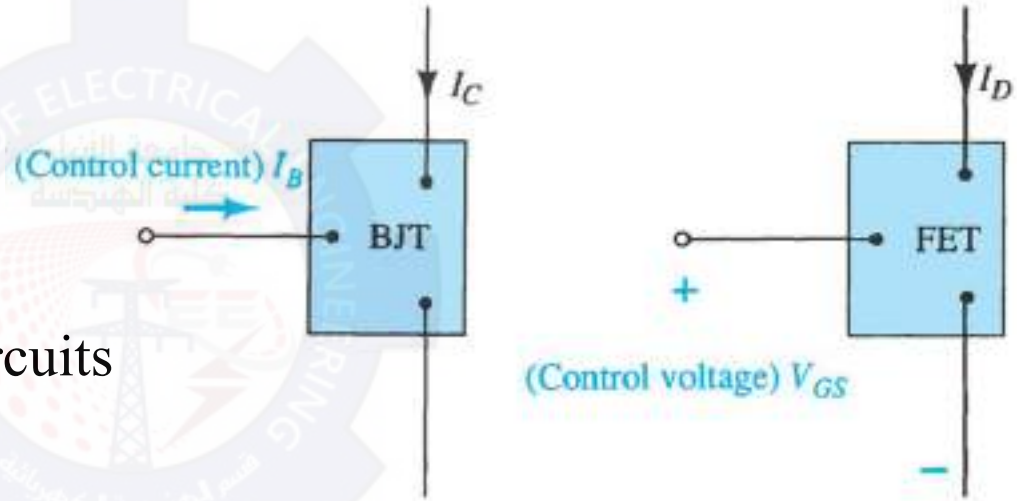
Munther N. Thiyab

2019-2020

FETs vs. BJTs

Similarities:

- Amplifiers
- Switching devices
- Impedance matching circuits



Differences:

- FETs are voltage controlled devices. BJTs are current controlled devices.
- FETs have a higher input impedance. BJTs have higher gains.
- FETs are less sensitive to temperature variations and are more easily integrated on ICs.

FET Types

- **JFET:** Junction FET
- **MOSFET:** Metal–Oxide–Semiconductor FET
  - **D-MOSFET:** Depletion MOSFET
  - **E-MOSFET:** Enhancement MOSFET

JFET Construction

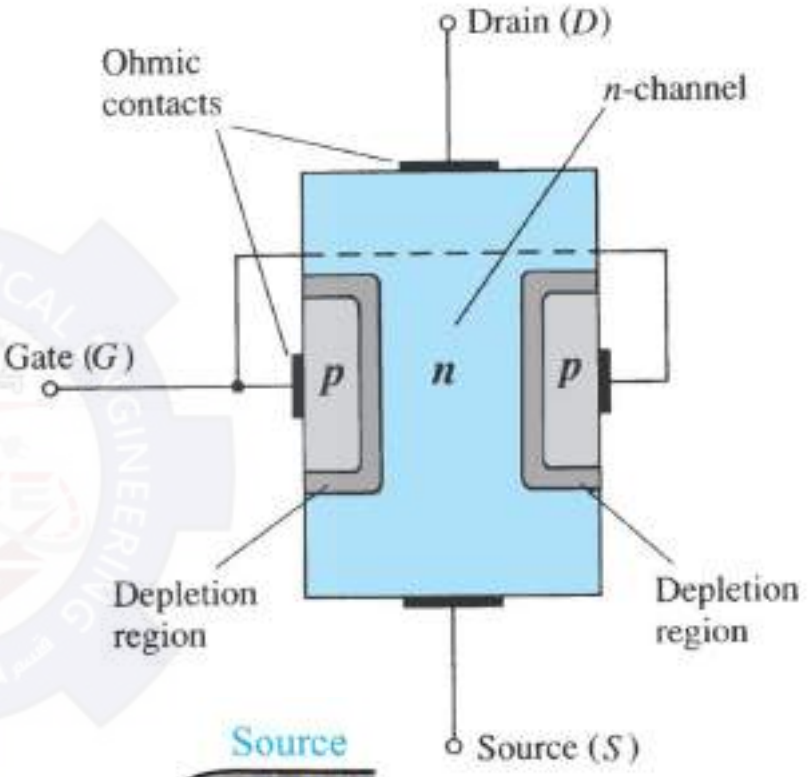
There are two types of JFETs

- ***n*-channel**
- ***p*-channel**

The n-channel is more widely used.

There are three terminals:

- **Drain (D) and Source (S) are connected to the *n*-channel**
- **Gate (G) is connected to the *p*-type material**



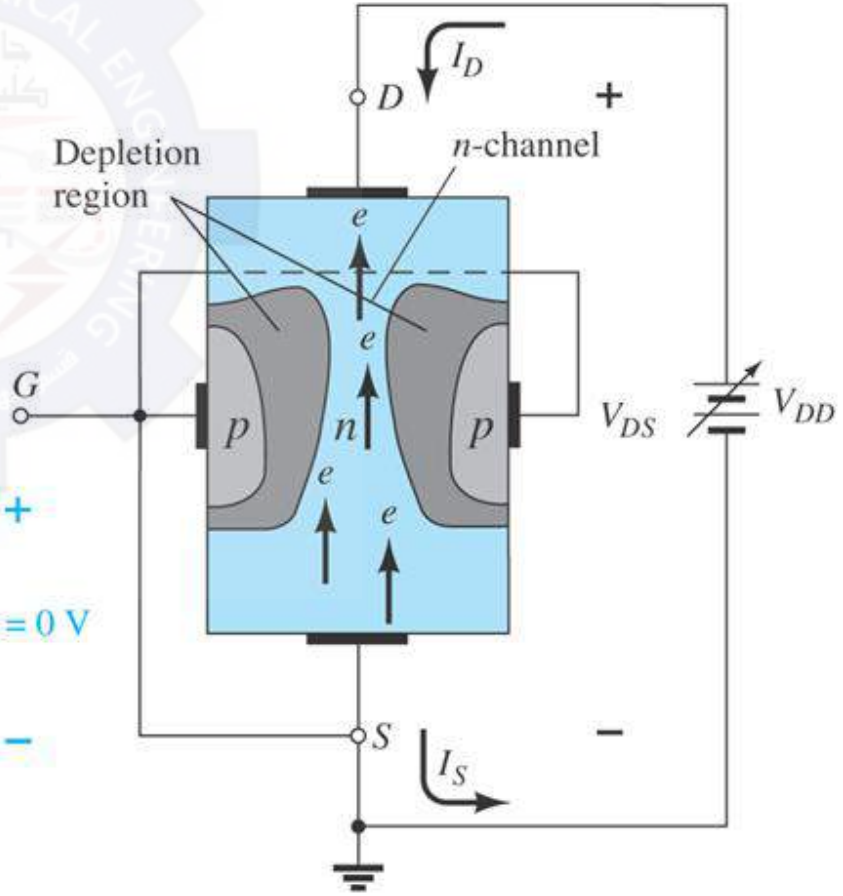
Water analogy for the JFET control mechanism.

JFET Operating Characteristics:

V_{GS} = 0 V , V_{DS} some positive value

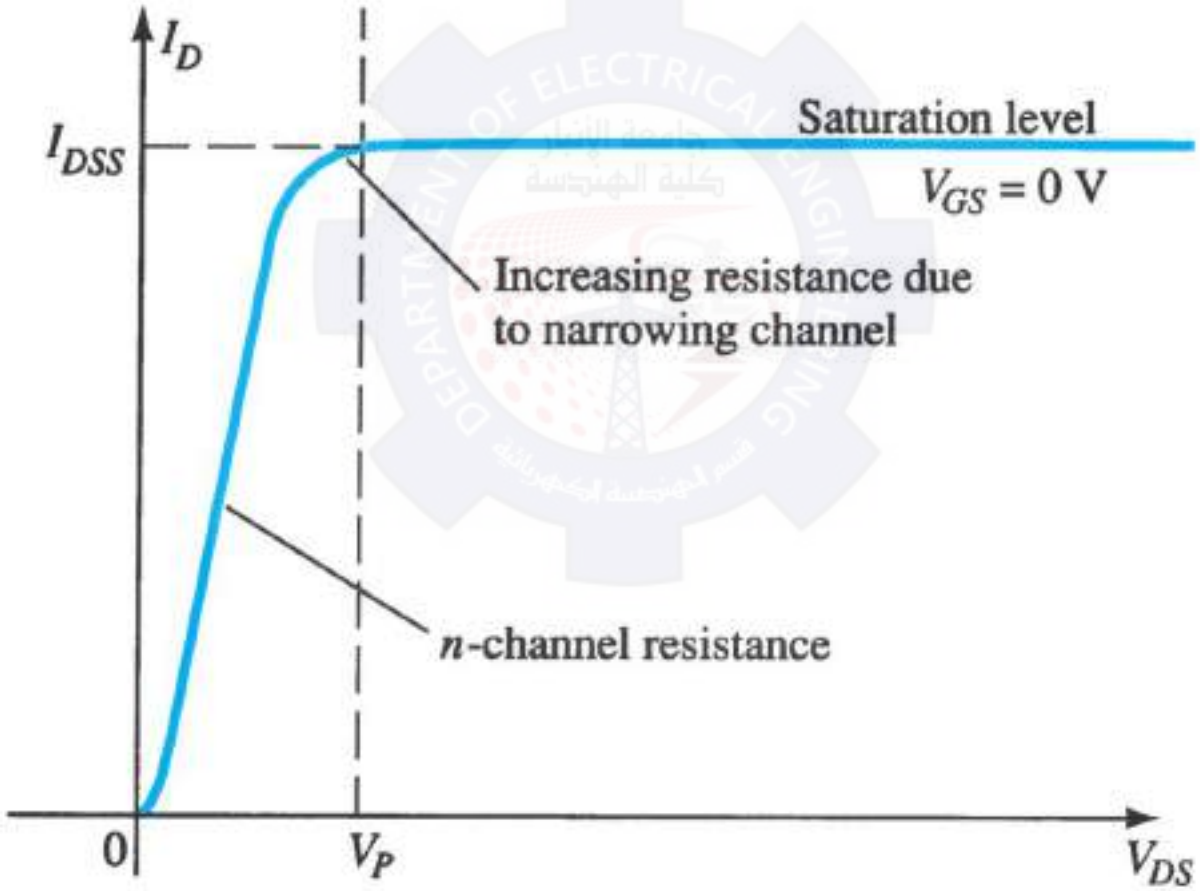
When V_{GS} = 0 and V_{DS} is increased from 0 to a more positive voltage:

- The depletion region between p-gate and n-channel increases.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.



JFET Operating Characteristics:

V_{GS} = 0 V , V_{DS} some positive value

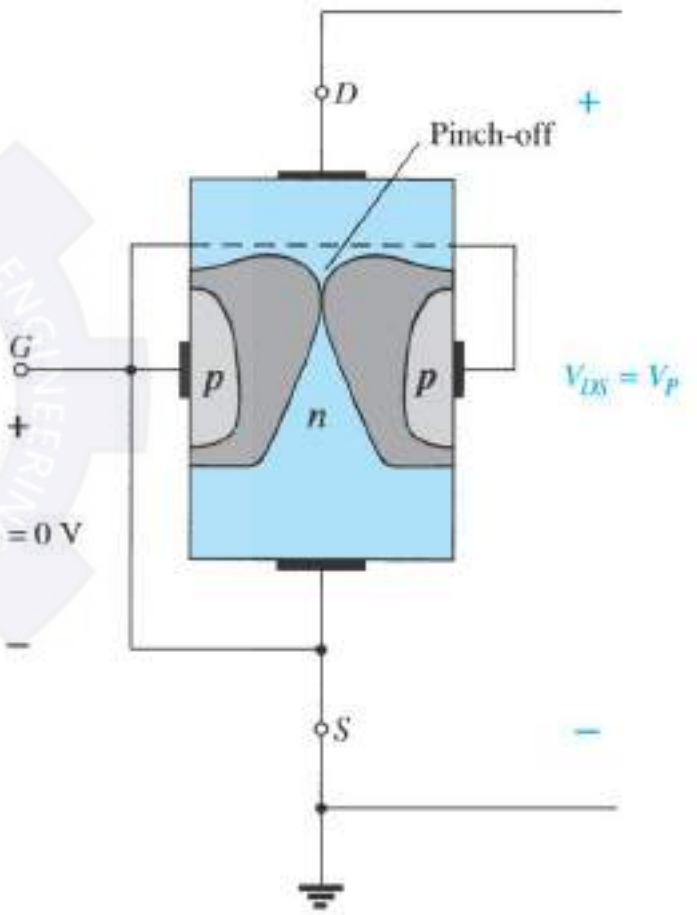


I_D versus V_{DS} for V_{GS} = 0 V.

JFET Operating Characteristics: Pinch Off

If $V_{GS} = 0$ and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.

As V_{DS} is increased beyond $|V_P|$, the level of I_D remains the same ($I_D=I_{DSS}$).

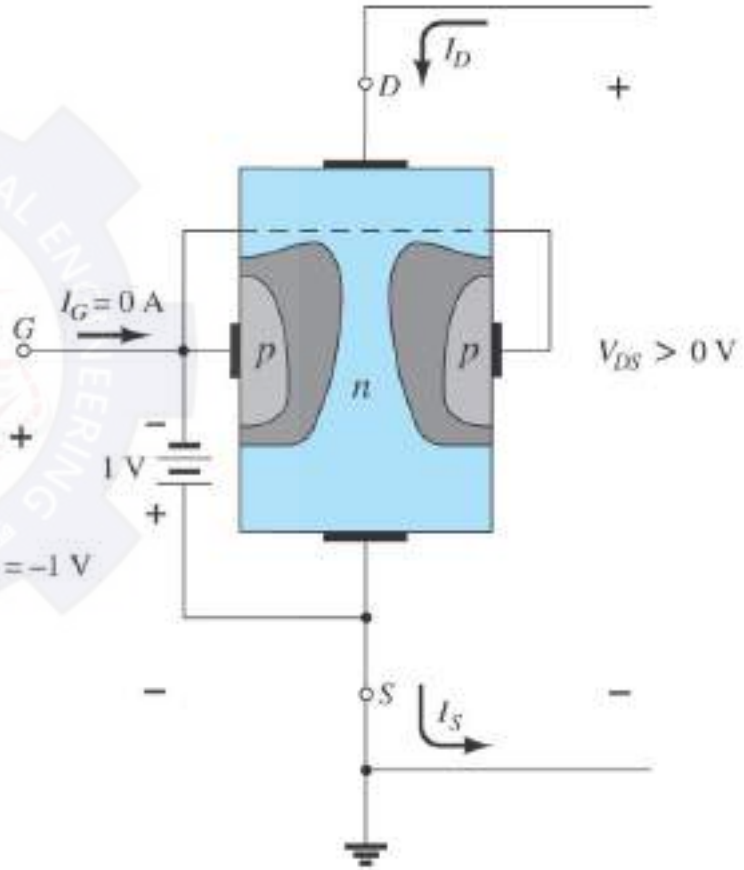


I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS}=0$ and $V_{DS} > |V_P|$.

JFET Operating Characteristics , $V_{GS}<0$

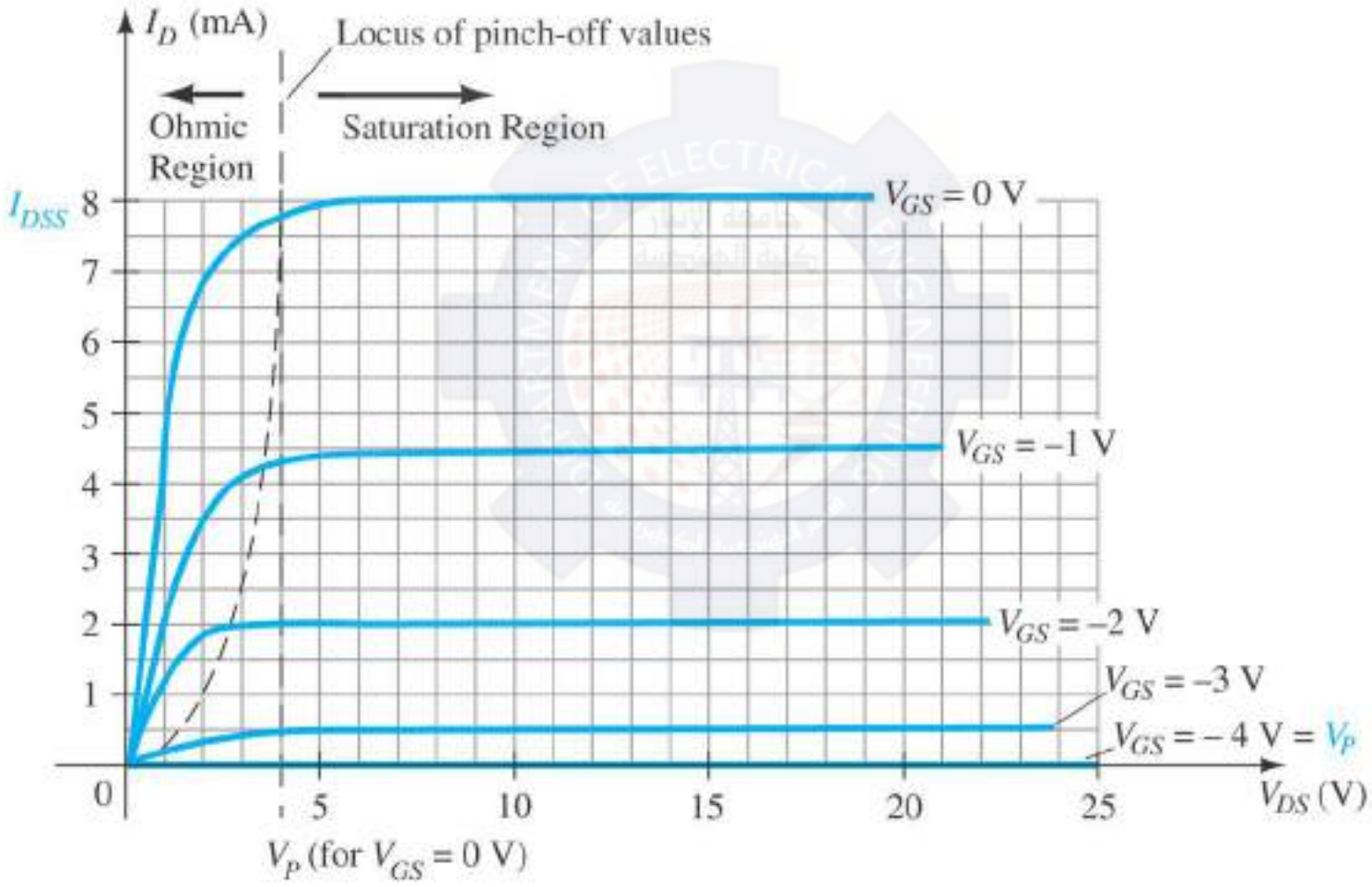
- As V_{GS} becomes more negative, the depletion region increases.
- The more negative V_{GS}, the resulting level for I_D is reduced.
- Eventually, when $V_{GS}=V_P$ (-ve) [$V_P=\mathbf{V_{GS(off)}}$], I_D is 0 mA. (the device is "***turned off***".

- The level of V_{GS} that results in $I_D=0$ mA is defined by $V_{GS}=V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.



Application of a negative voltage to the gate of a JFET.

JFET Operating Characteristics

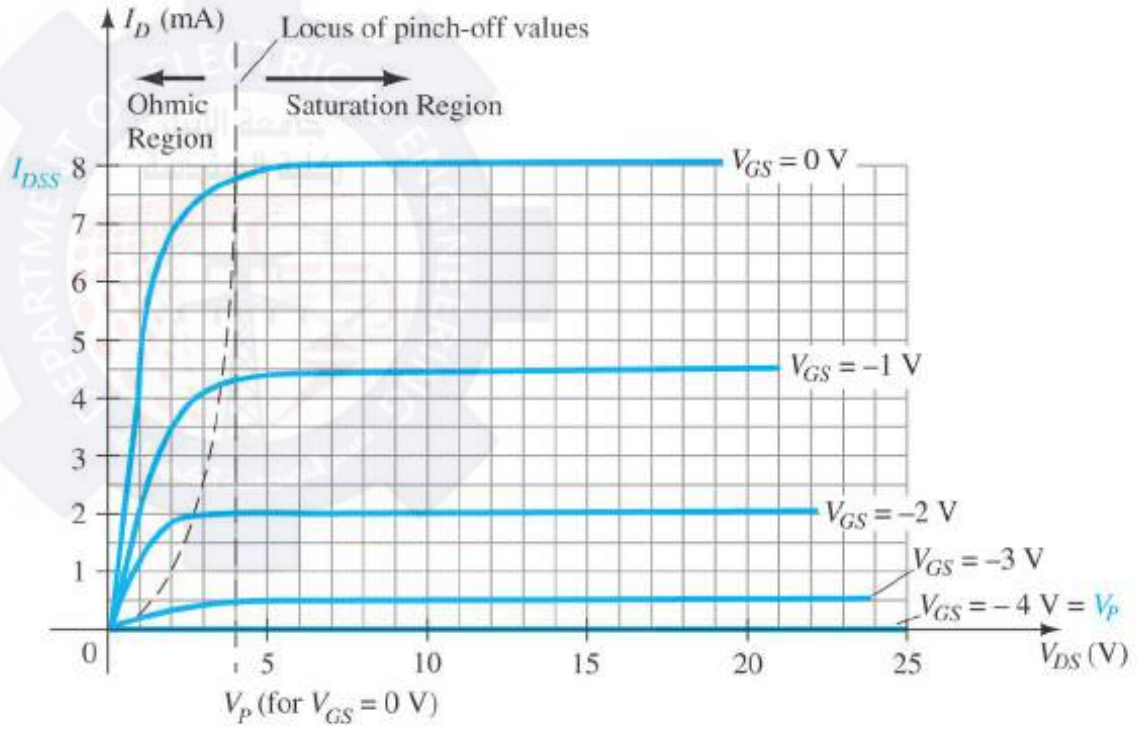


n-Channel JFET characteristics with I_{DSS} = 8 mA and V_P = -4 V.

JFET Operating Characteristics: Voltage-Controlled Resistor

•The region to the left of the pinch-off point is called the ohmic region.

•The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

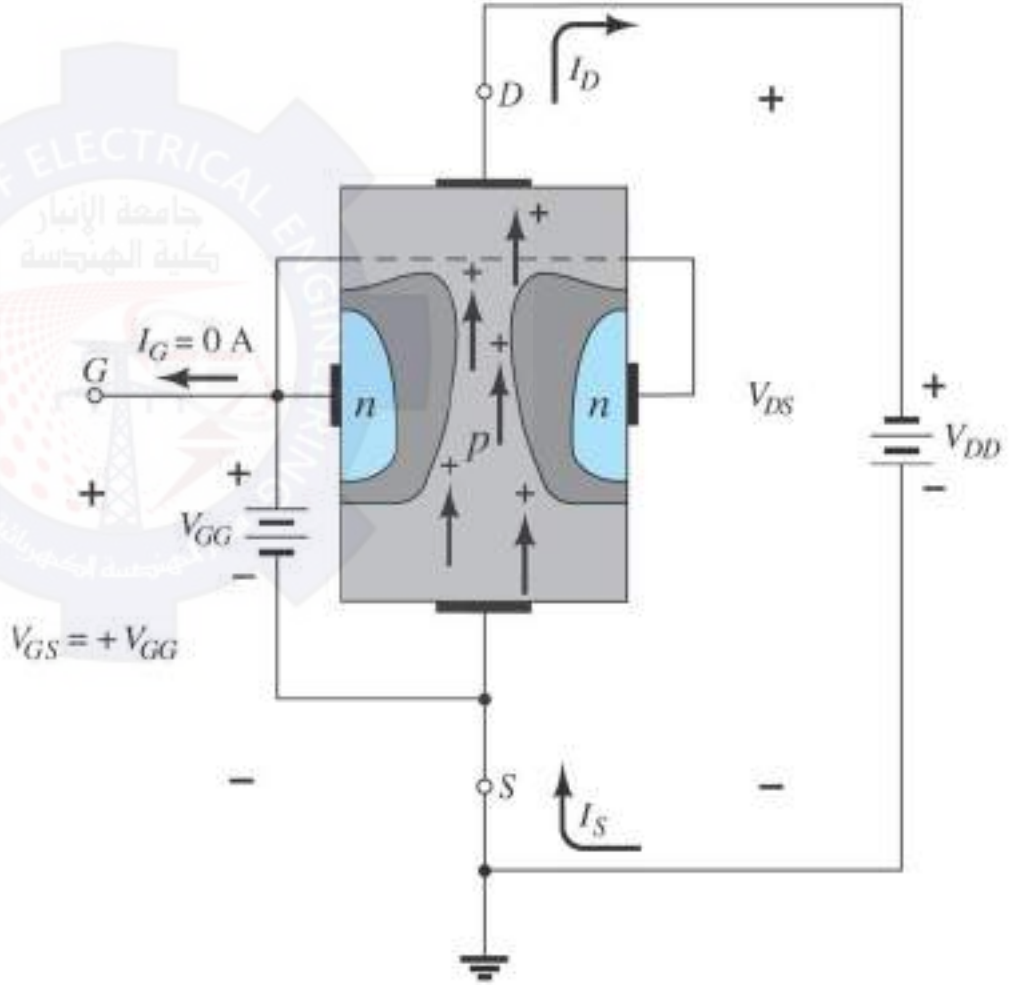


$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

where r_o is the resistance with V_{GS}=0 and r_d is the resistance at a particular level of V_{GS}.

p-Channel JFETS

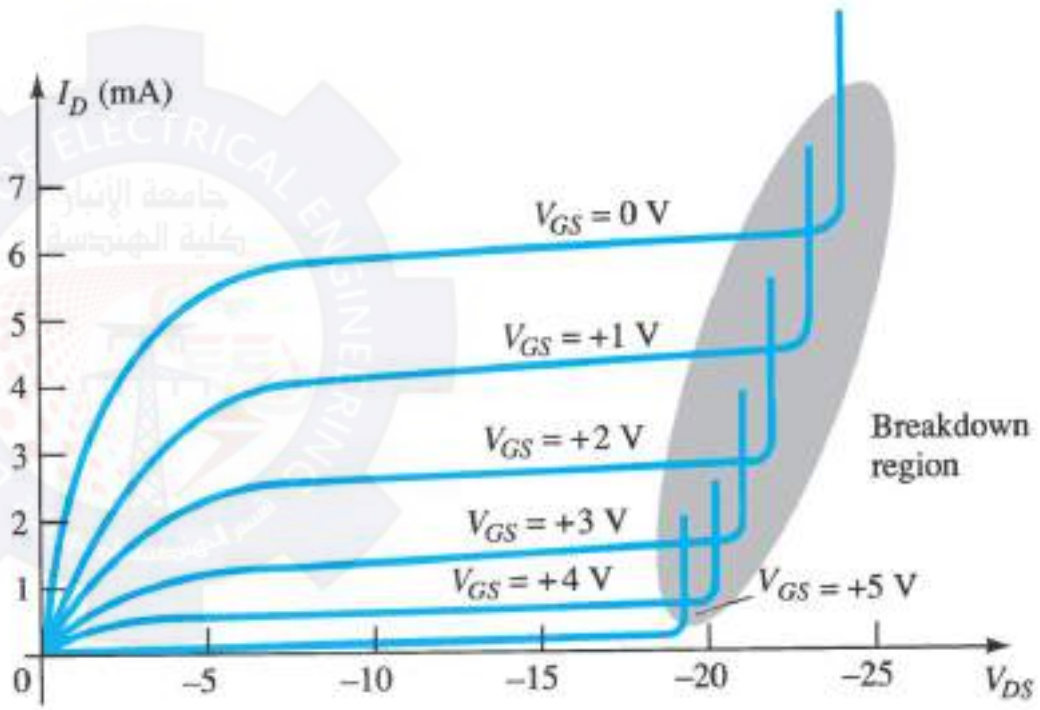
The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.



p-Channel JFET Characteristics

As V_{GS} increases more positively

- The depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- Eventually $I_D = 0$ A



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

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Chapter 6 : Field Effect Transistors
Lec06_p2

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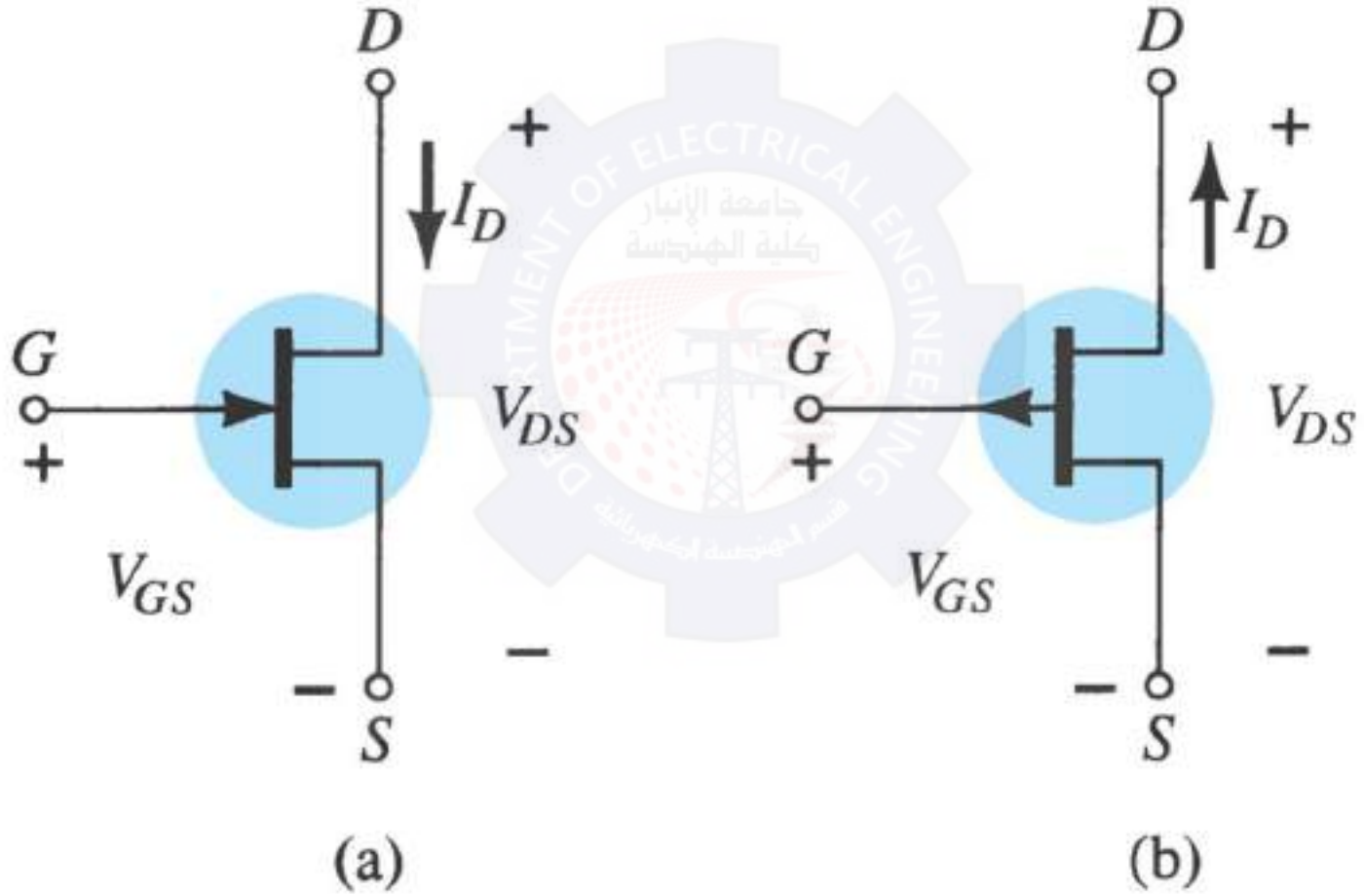
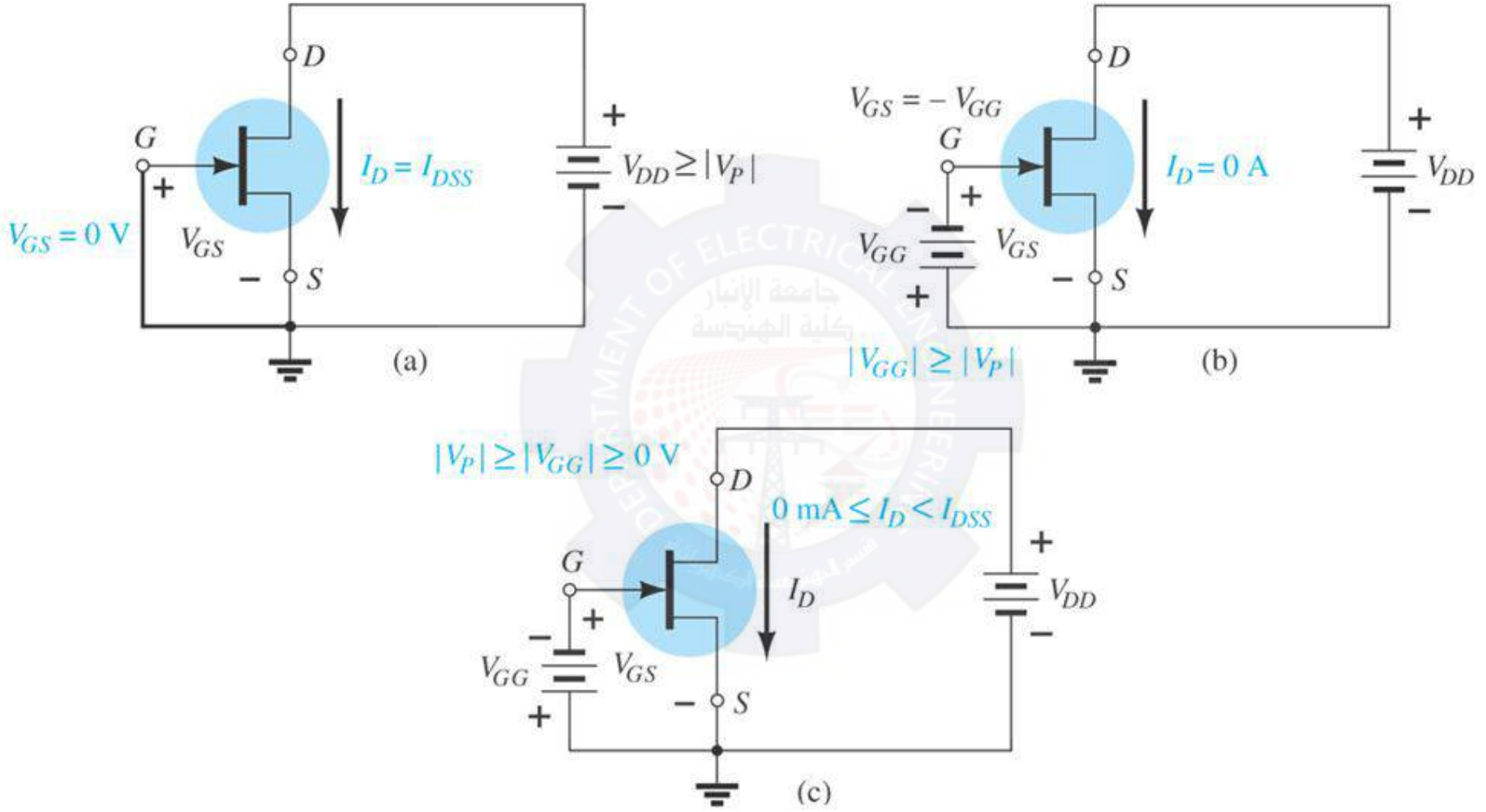
2019-2020

JFET Symbols



JFET symbols: (a) n-channel; (b) p-channel.



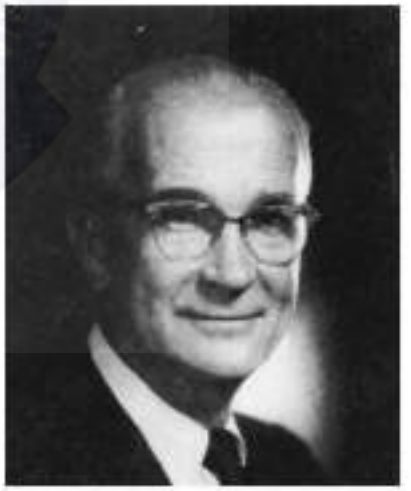
(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than (more negative than) the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

JFET Transfer Characteristics

In a BJT, β indicates the relationship between I_B (input) and I_C (output).

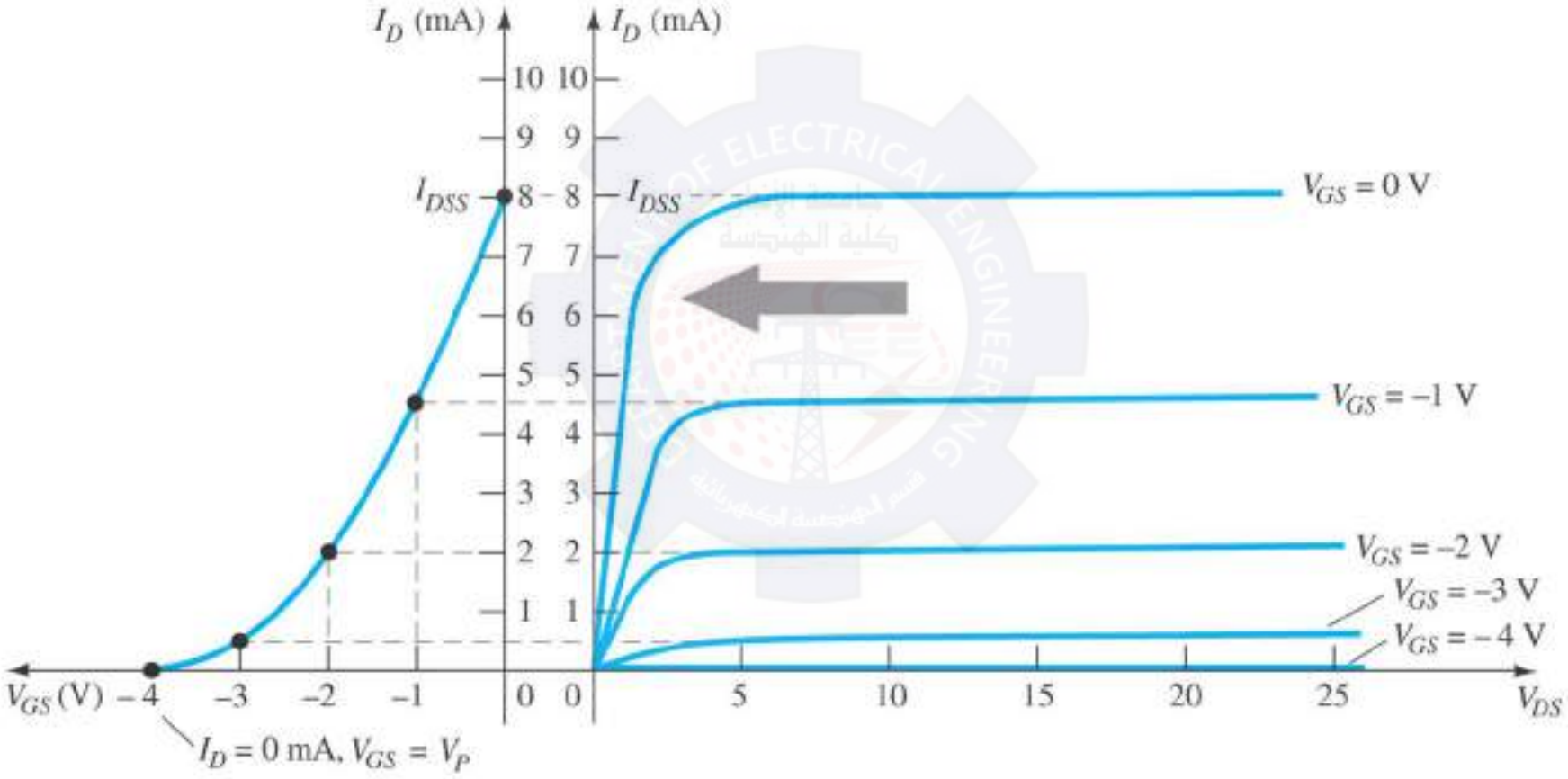
In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated (*Shockley's equation*):

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$



William Bradford Shockley
(1910–1989)

JFET Transfer Curve



This graph shows the value of I_D for a given value of V_{GS}.

Plotting the JFET Transfer Curve

Using I_{DSS} and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Solving for V_{GS} = 0V $\quad I_D = I_{DSS}$

Step 2

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Solving for $V_{GS} = V_p$ ($V_{GS(off)}$) $\quad I_D = 0A$

Step 3

Solving for V_{GS} = 0V to V_p $\quad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

i.e. For V_{GS} = -1 V $\quad I_D = 8mA\left(1-\frac{-1}{-4}\right)^2 = 4.5\text{mA}$

Conversely , for a given I_D, V_{GS} can be obtained:

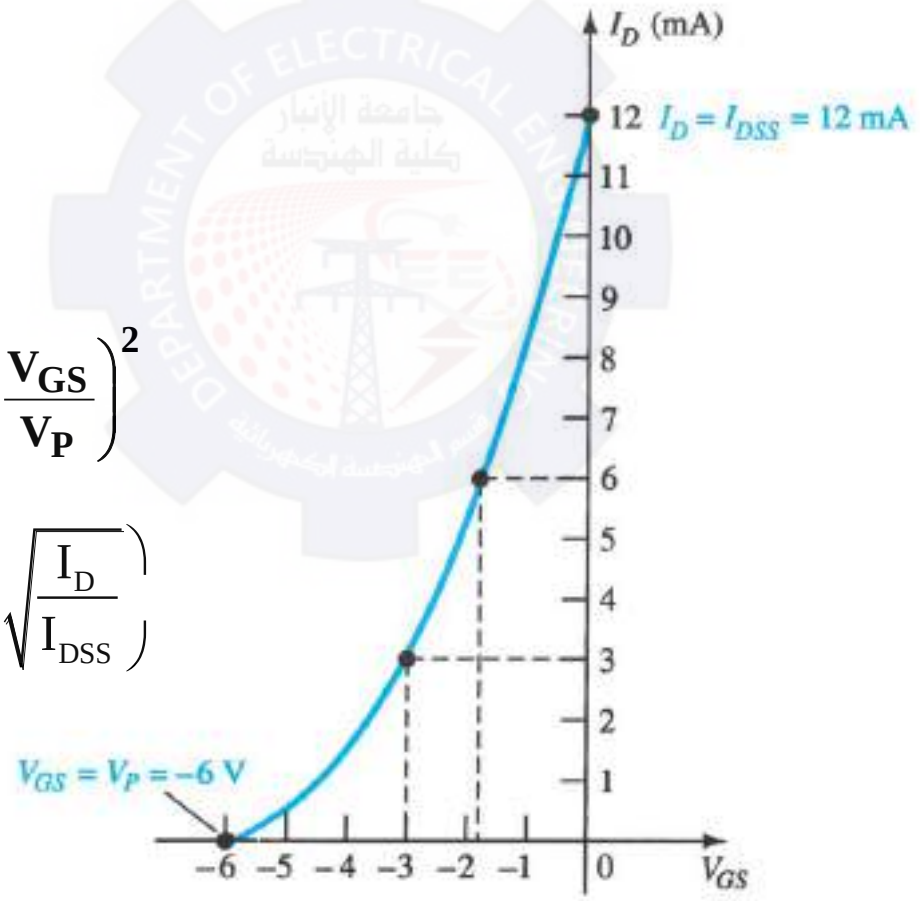
$$V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

Example 6.1

Sketch the transfer curve defined by I_{DSS}=12 mA and V_P=-6V.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$



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Chapter 6 : Field Effect Transistors

Lec06_p3

Munther N. Thiyab

2019-2020

MOSFETs

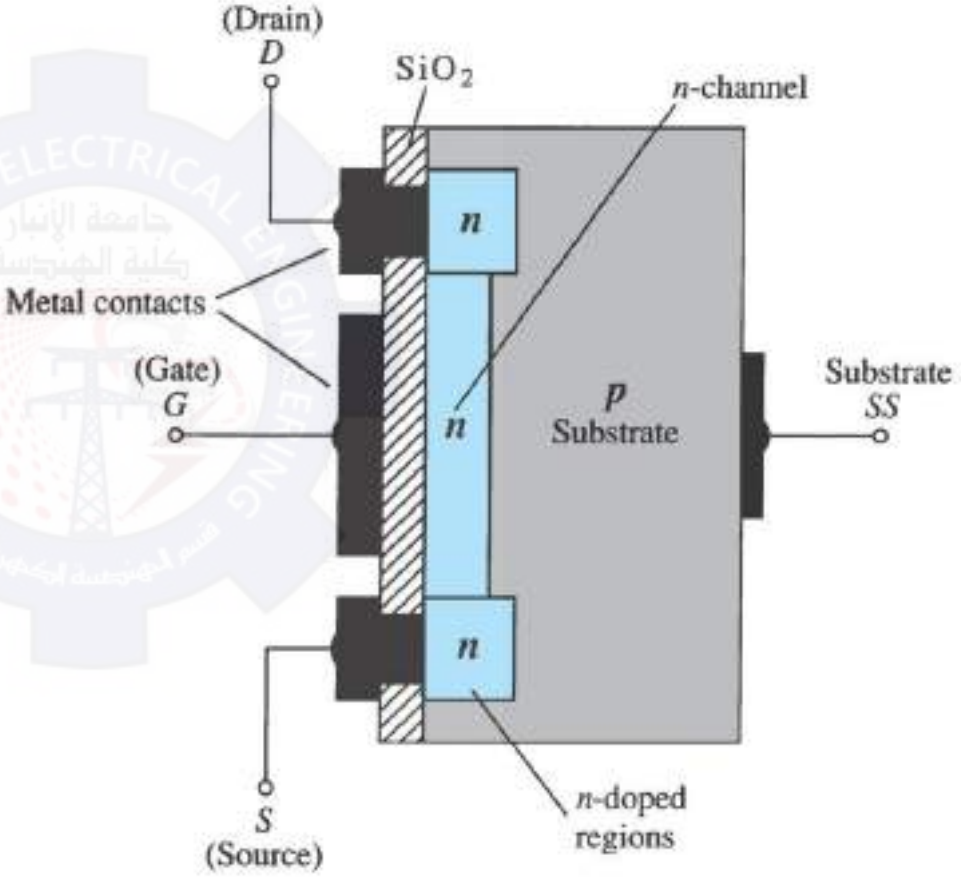
MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

- **Depletion-Type**
- **Enhancement-Type**

Depletion-Type MOSFET Construction

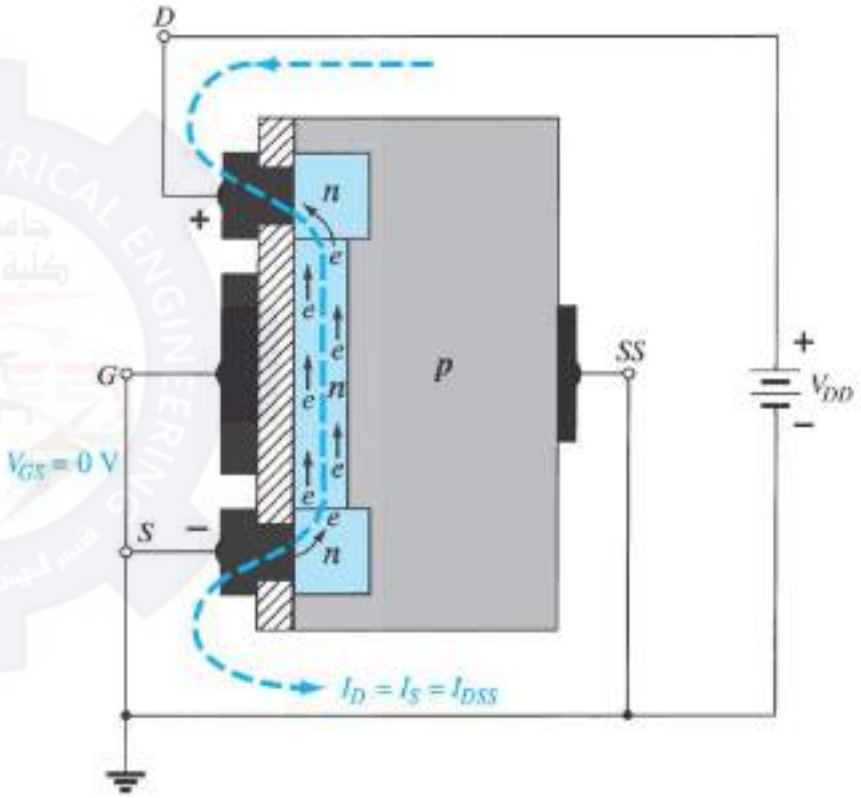
- The Drain (D) and Source (S) connect to the to *n*-doped regions.
- These *n*-doped regions are connected via an *n*-channel.
- This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).



n-Channel depletion-type MOSFET.

Depletion-Type MOSFET :Basic Operation and Characteristics

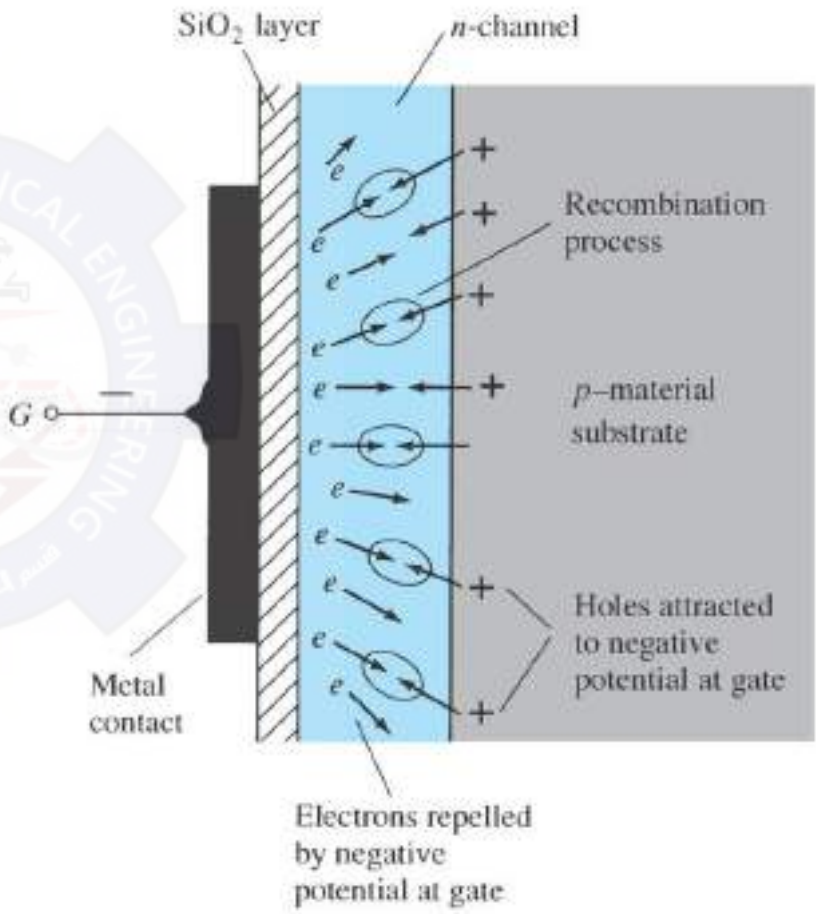
- V_{GS}=0 and V_{DS} is applied across the drain to source terminals.
- This results to attraction of free electrons of the n-channel to the drain, and hence current flows.



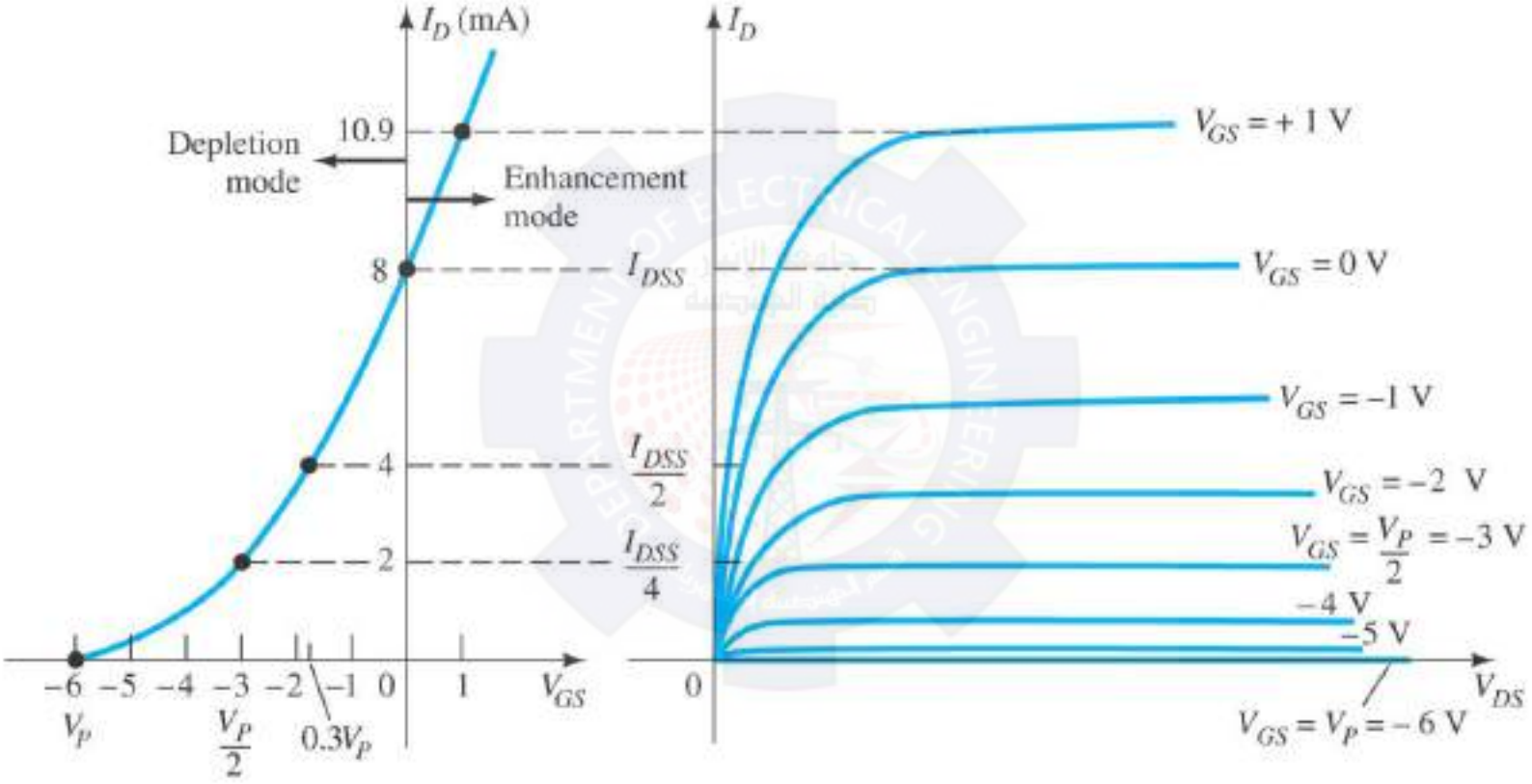
n-Channel depletion-type MOSFET with V_{GS} = 0 V and applied voltage V_{DD}.

Depletion-Type MOSFET :Basic Operation and Characteristics

- V_{GS} is set at a negative voltage such as -1 V.
- The negative potential at the gate pressures electrons toward the p-type substrate and attract holes from the p-type substrate.
- This will reduce the number of free electrons in the *n*-channel available for conduction.
- The more negative the V_{GS}, the resulting level of drain current I_D is reduced.
- When V_{GS} is reduced to V_P (Pinch-off voltage), then I_D=0 mA.



Depletion-Type MOSFET :Basic Operation and Characteristics

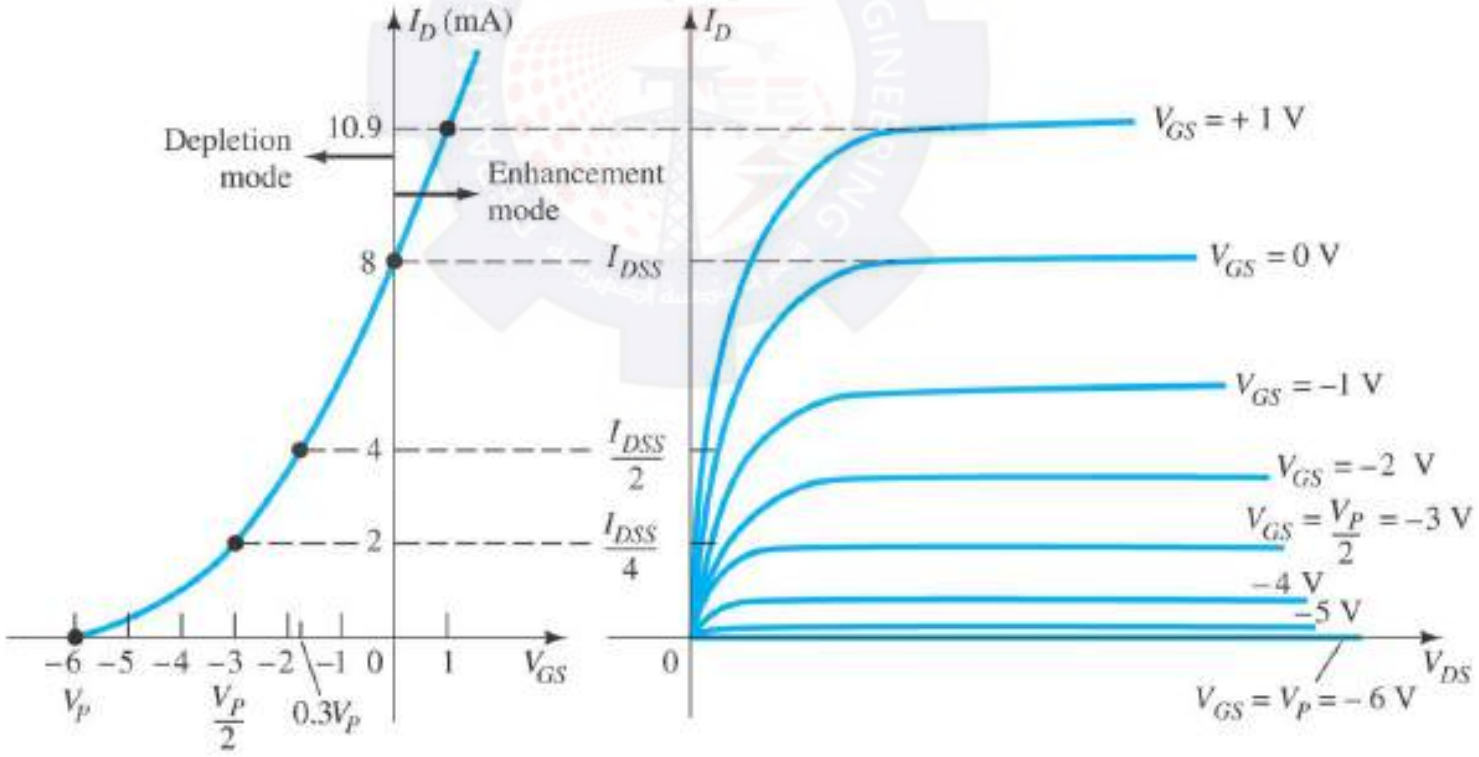


- When V_{GS} is reduced to V_P (Pinch-off) [i.e. V_p=-6V], then I_D=0 mA.
- For **positive** values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate and hence I_D increases.

Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

- **Depletion mode**
- **Enhancement mode**



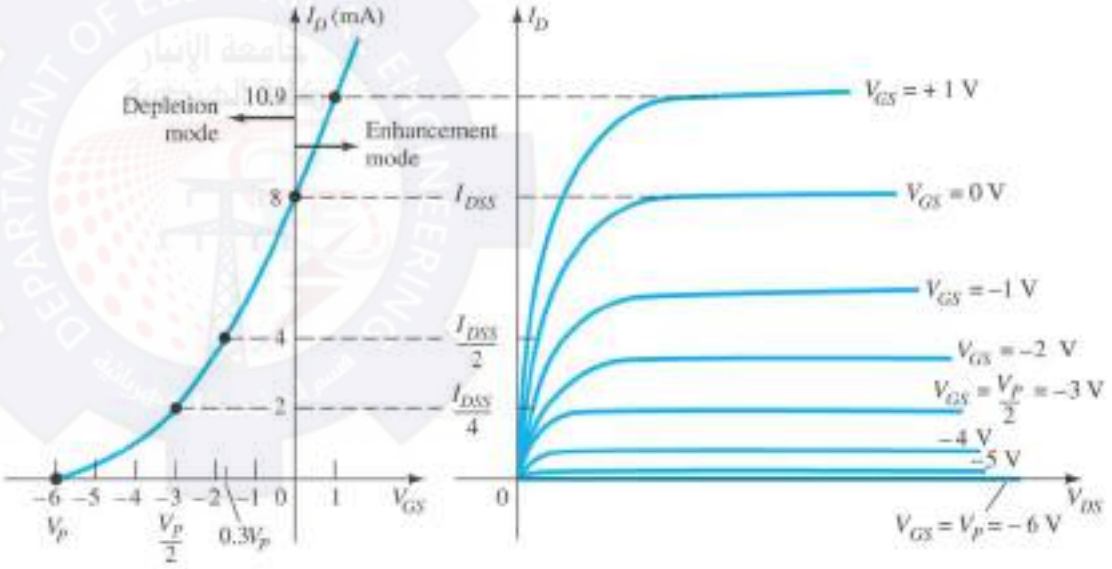
D-Type MOSFET in Depletion Mode

Depletion Mode

The characteristics are similar to a JFET.

- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

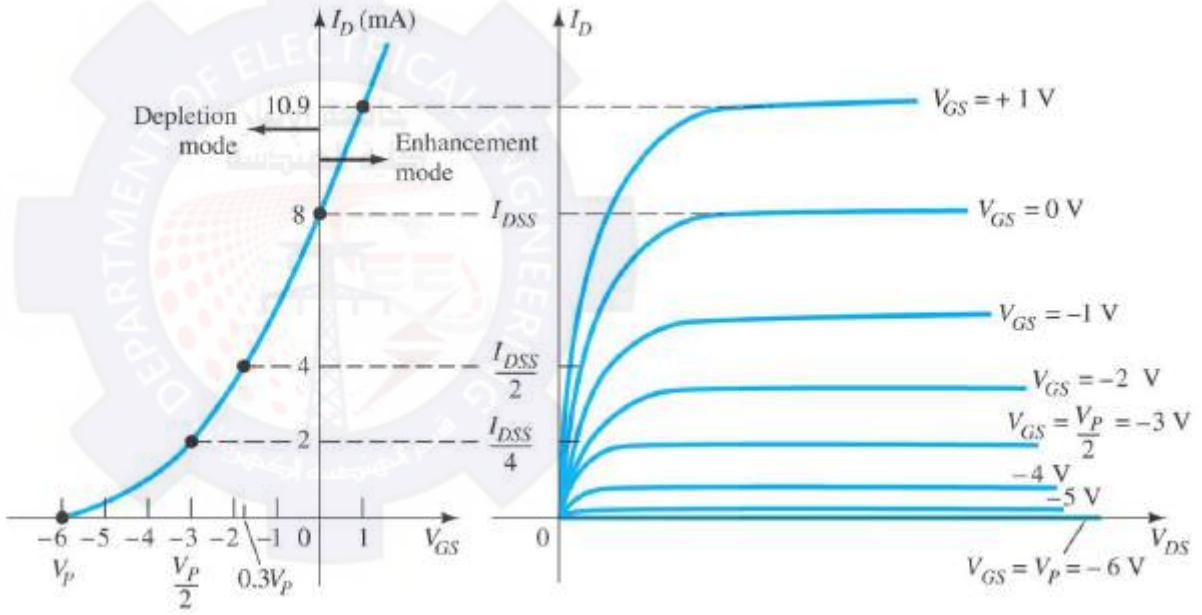


D-Type MOSFET in Enhancement Mode

Enhancement Mode

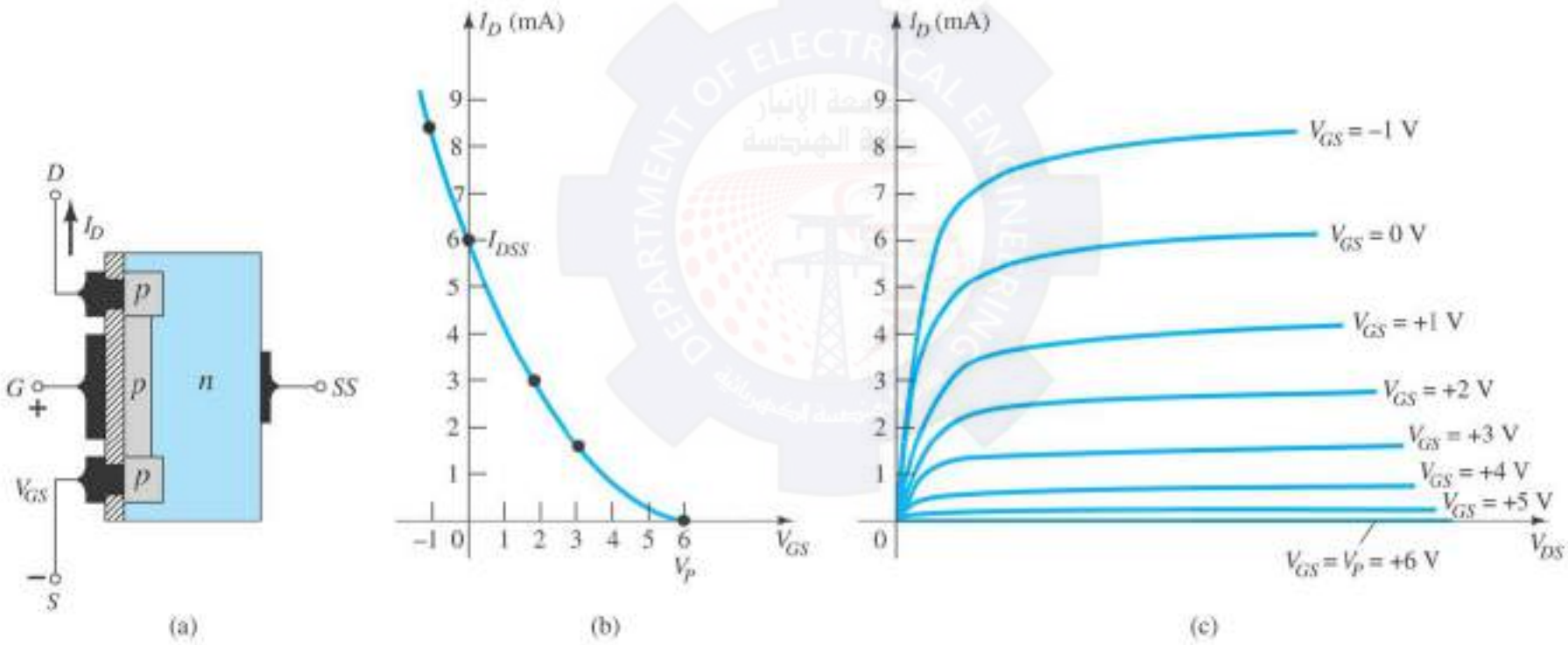
- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

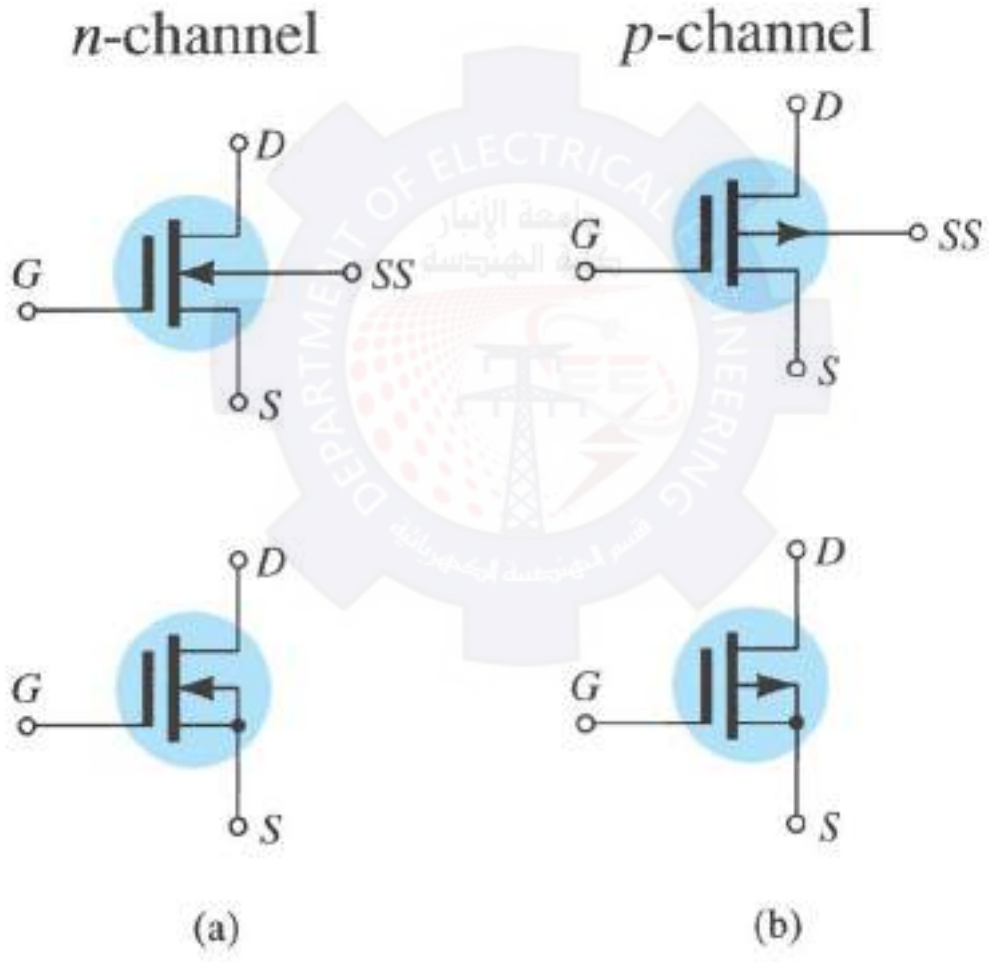


Note that V_{GS} is now a positive polarity

p-Channel D-Type MOSFET



D-Type MOSFET Symbols



(a) *n*-channel depletion-type MOSFETs ,(b) *p*-channel depletion-type MOSFETs

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Chapter 6 : Field Effect Transistors

Lec06_p4

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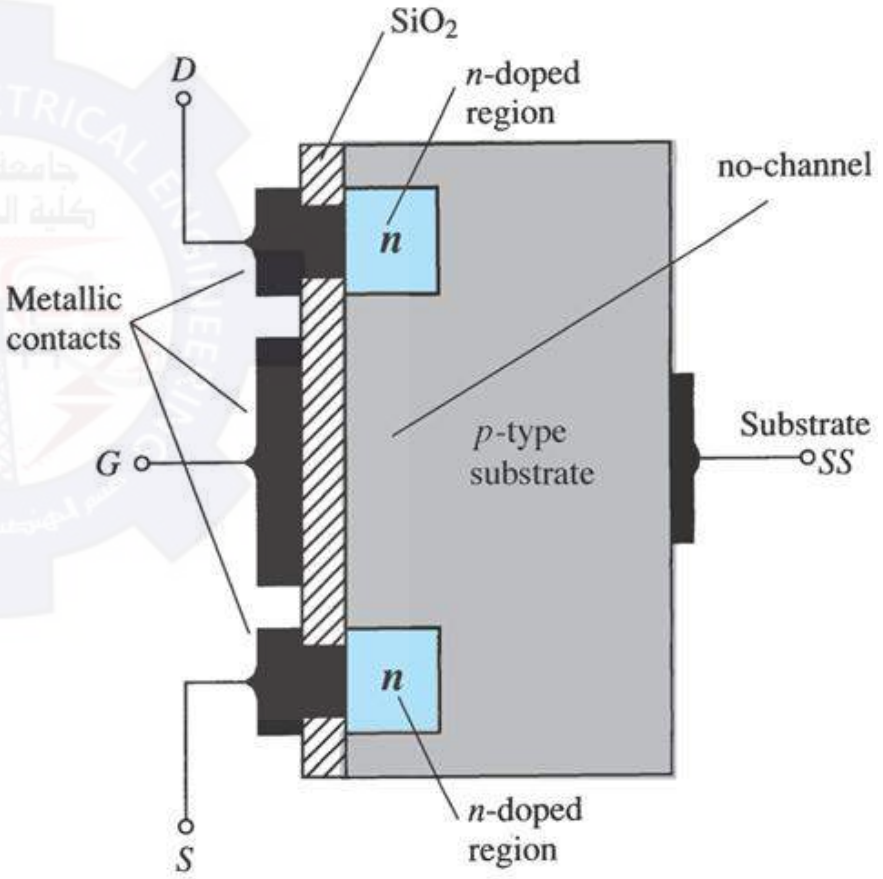
2019-2020

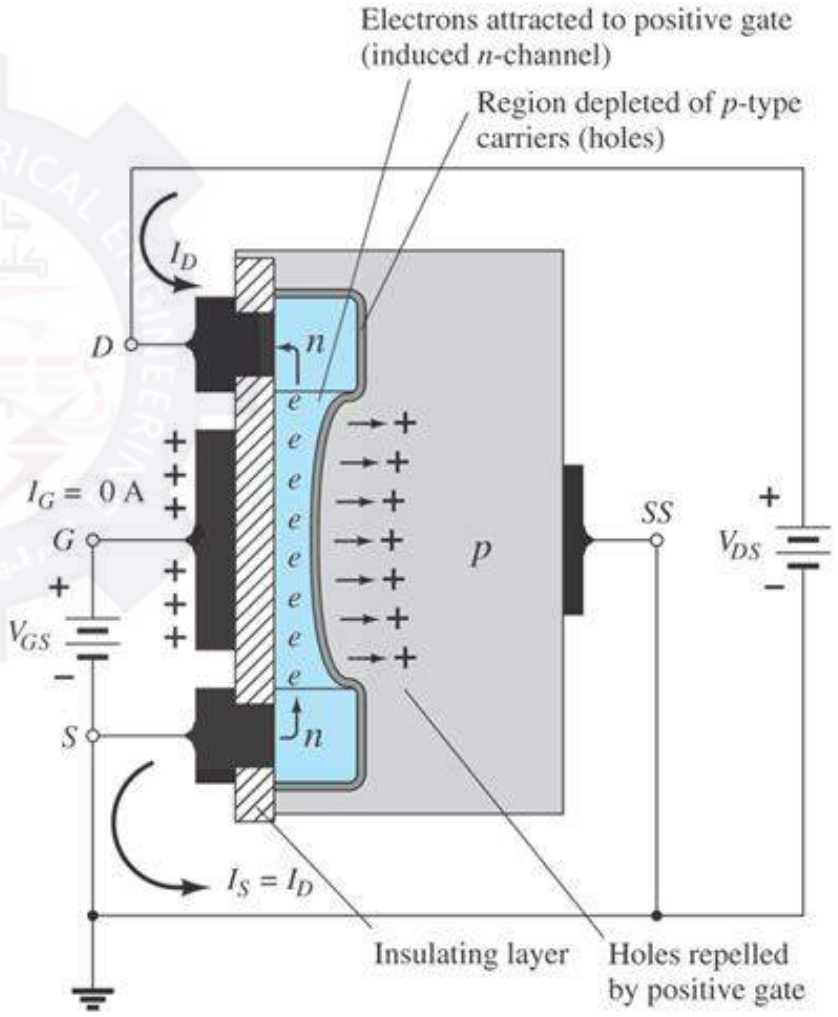
Enhancement-Type MOSFET Construction

- The Drain (D) and Source (S) connect to the to *n*-doped regions.
- The Gate (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- **There is no channel**
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the Substrate (SS)



Enhancement-Type MOSFET Construction

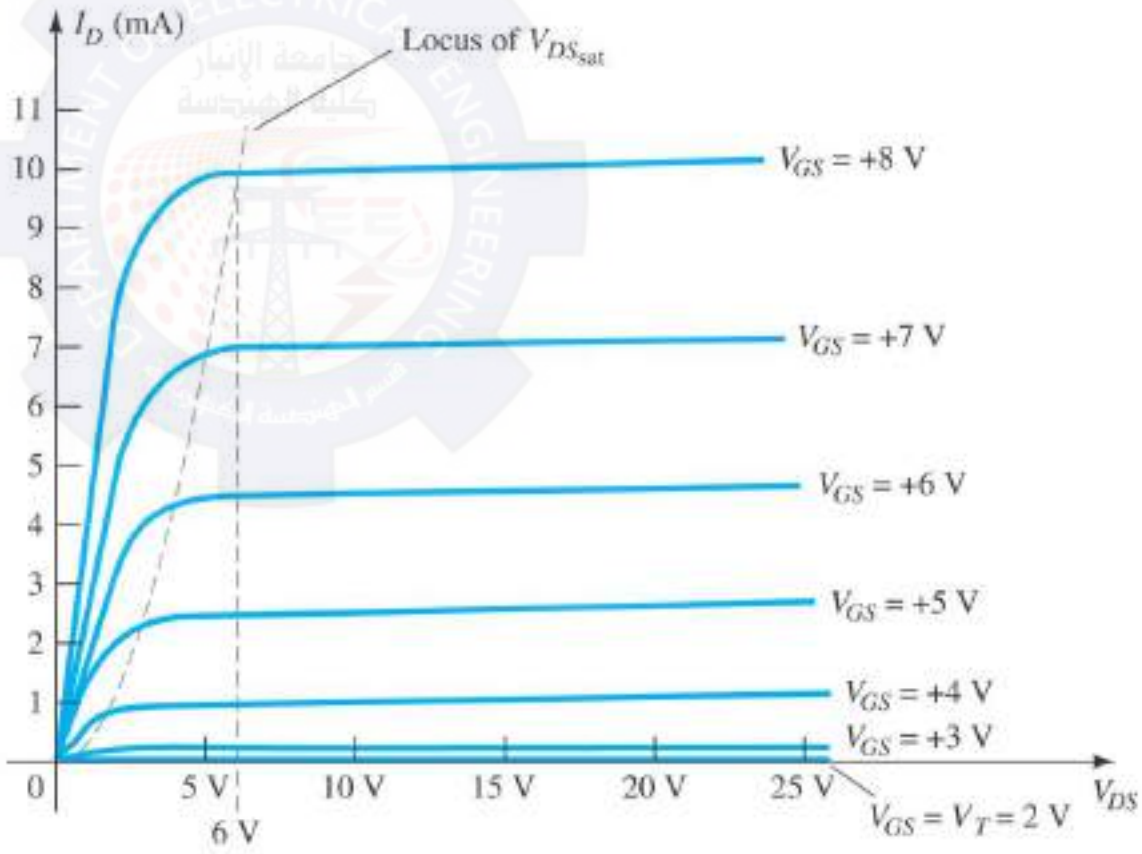
- For V_{GS}=0, I_D=0 (no channel).
- For V_{DS} some positive voltage, and V_{GS}=0, two reverse biased p-n junctions and no significant flow between drain and source.
- For V_{GS}>0 and V_{DS}>0, the positive voltage at gate pressure holes to enter deeper regions of the p-substrate, and the electrons in p-substrate will be attracted to the positive gate.
- The level of V_{GS} that results in the significant increase in drain current is called ***threshold voltage*** (V_T).
- For V_{GS}<V_T, I_D=0 mA.



Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

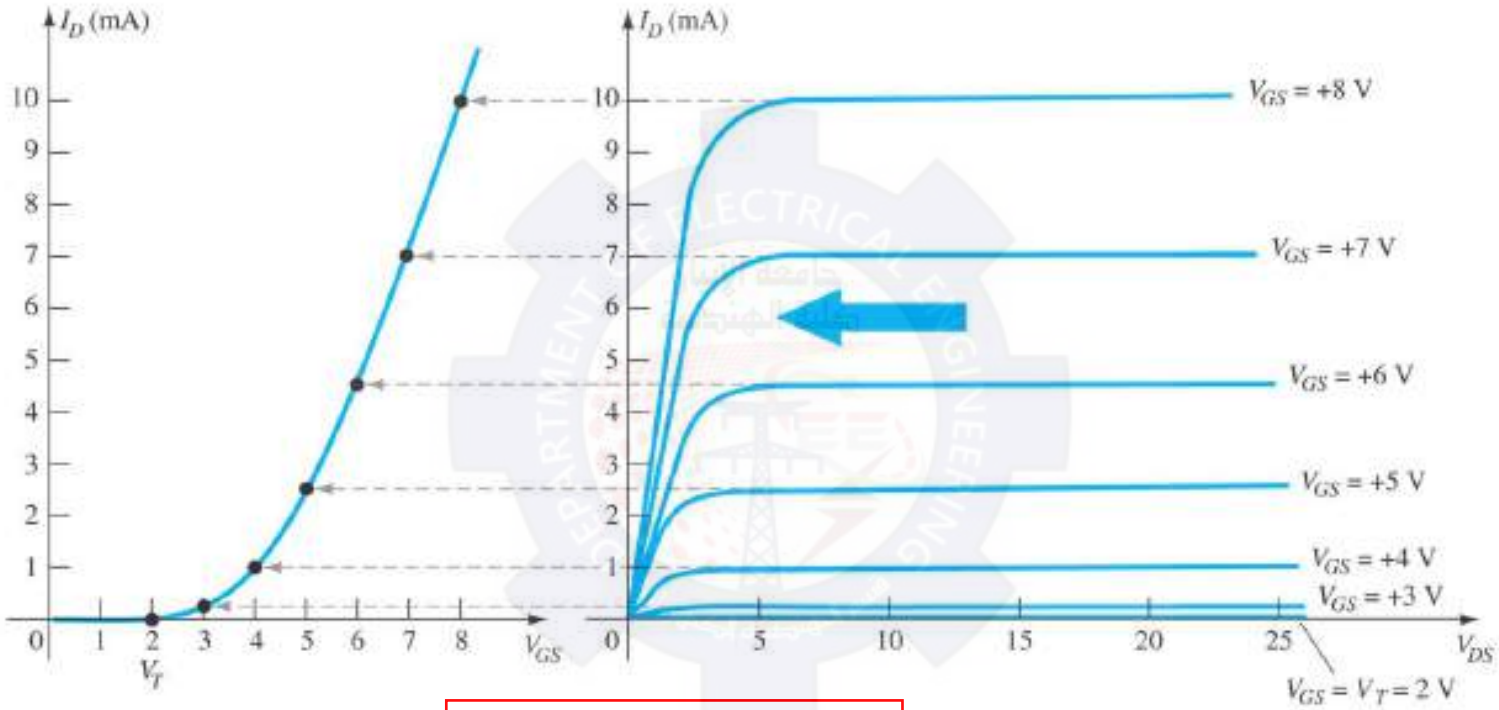
- **V_{GS} is always positive.**
- **As V_{GS} increases, I_D increases**
- **As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached**



V_{DSsat} can be calculated by:

$$V_{Dsat} = V_{GS} - V_T$$

E-Type MOSFET Transfer Curve



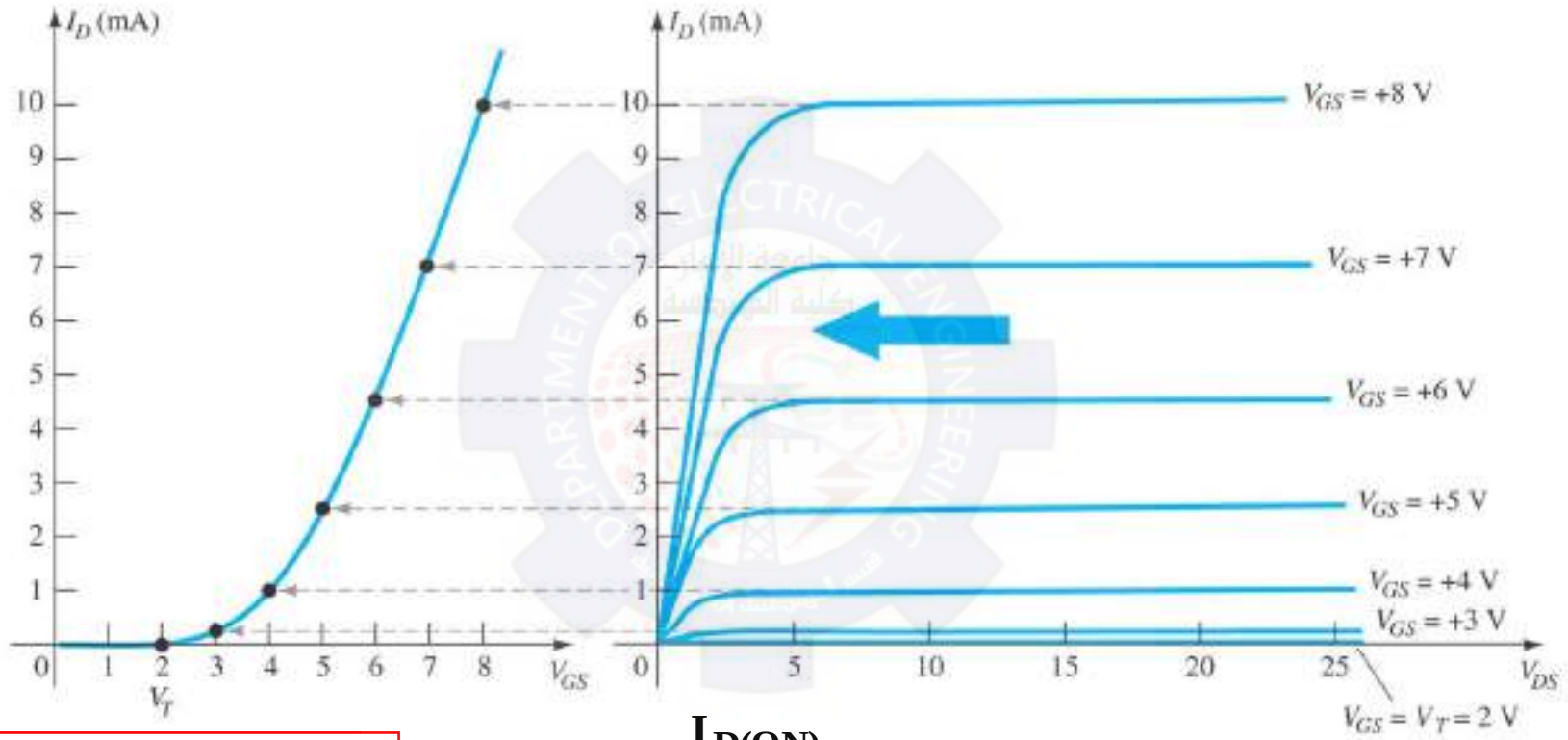
To determine I_D given V_{GS}: $\mathbf{I_D = k(V_{GS} - V_T)^2}$

Where: V_T = threshold voltage or voltage at which the MOSFET turns on

k, a constant, can be determined by using values at a specific point and the formula:

$$\mathbf{k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}}$$

E-Type MOSFET Transfer Curve

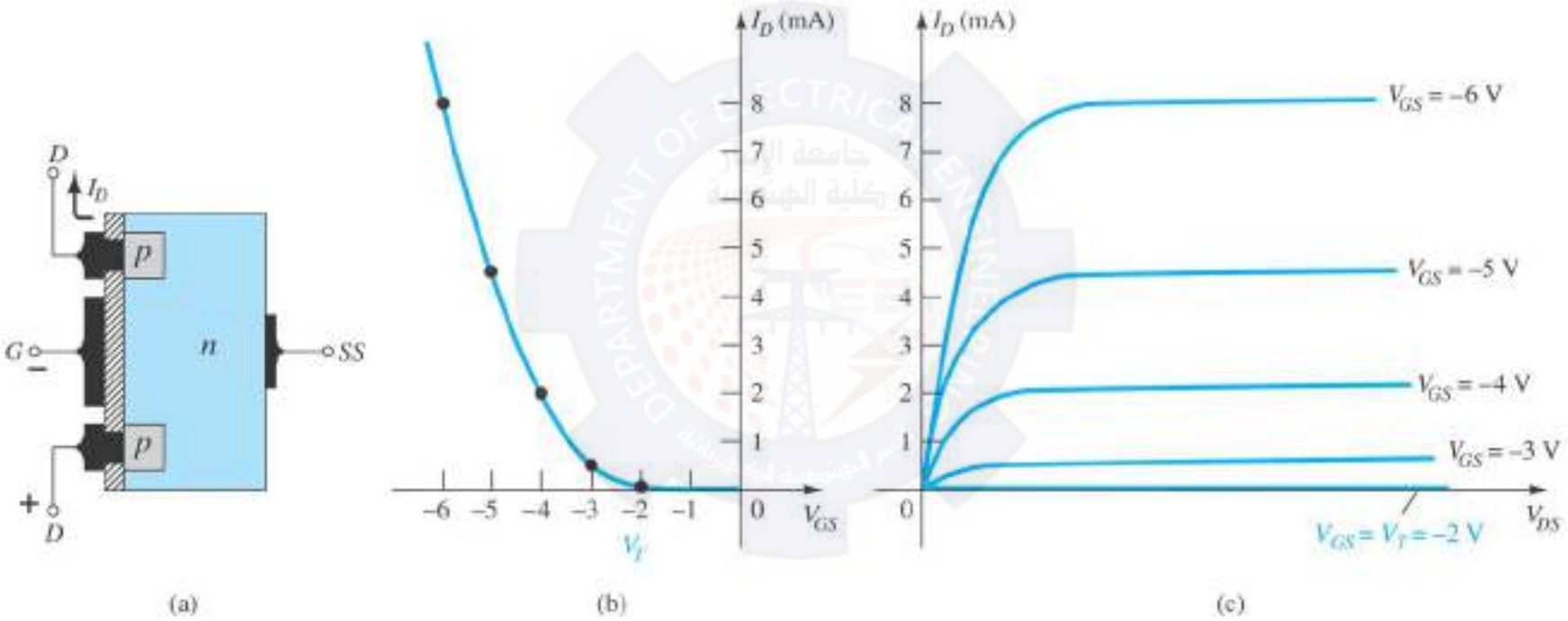


$$I_D = k(V_{GS} - V_T)^2 \qquad k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

Substituting $I_D(on)$ =10 mA when $V_{GS}(on)$=8V from the characteristics:

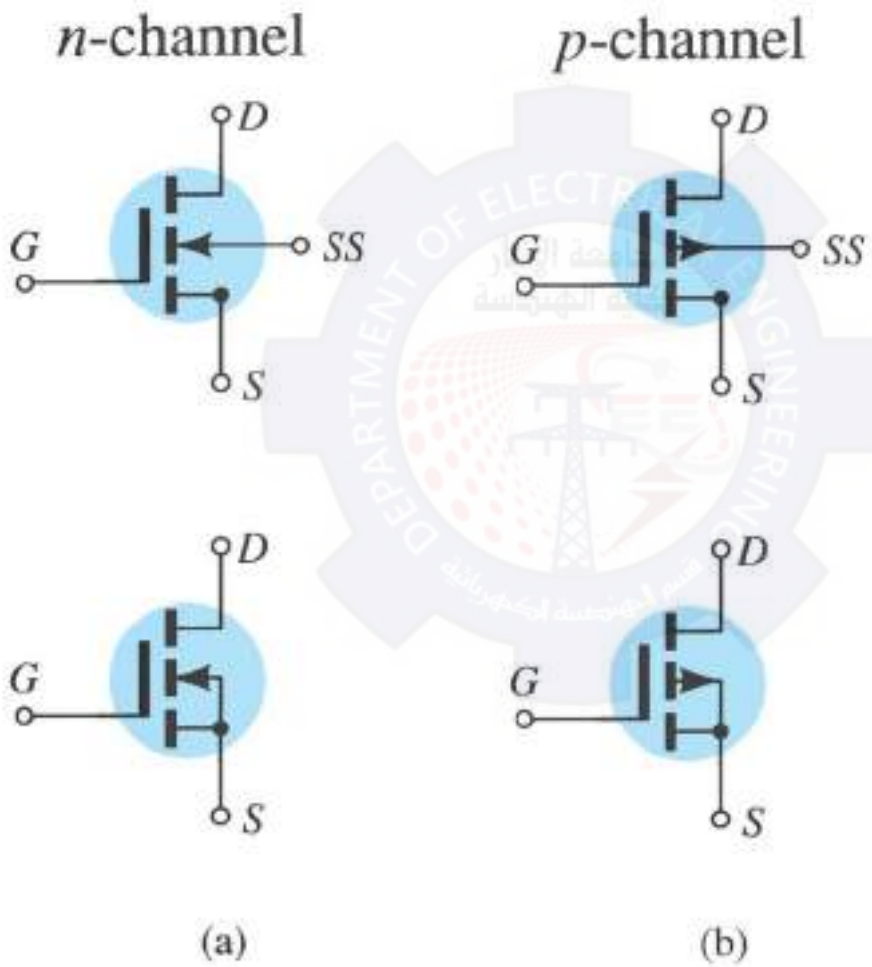
$$k = \frac{10\text{ mA}}{(8-2)^2} = 0.278\times10^{-3}\ \text{A/V}^2 \Rightarrow I_D = 0.278\times10^{-3}(V_{GS} - 2V)^2$$

p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

MOSFET Symbols



Symbols for (a) *n*-channel enhancement-type MOSFETs and (b) *p*-channel enhancement-type MOSFETs.

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Chapter 7 : FET Biasing

Lec07_p1

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2019-2020

Basic Current Relationships

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETS and D-Type MOSFETs:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For E-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

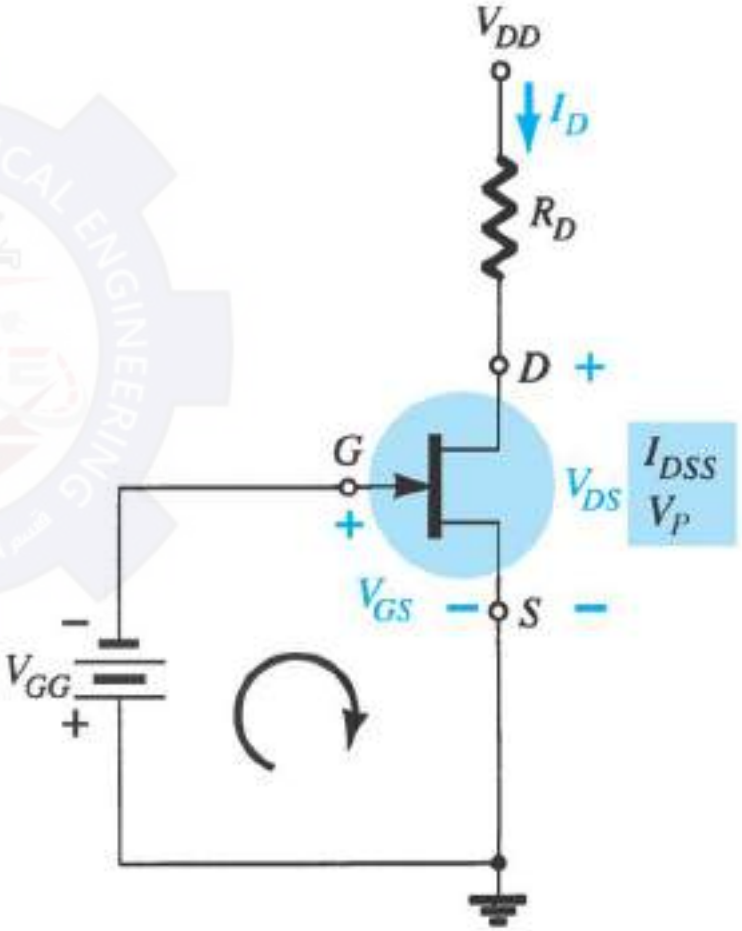
Fixed-Bias Configuration

$$I_G \cong 0A$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0, \quad V_D = V_{DS}, \quad V_{GS} = -V_{GG}$$

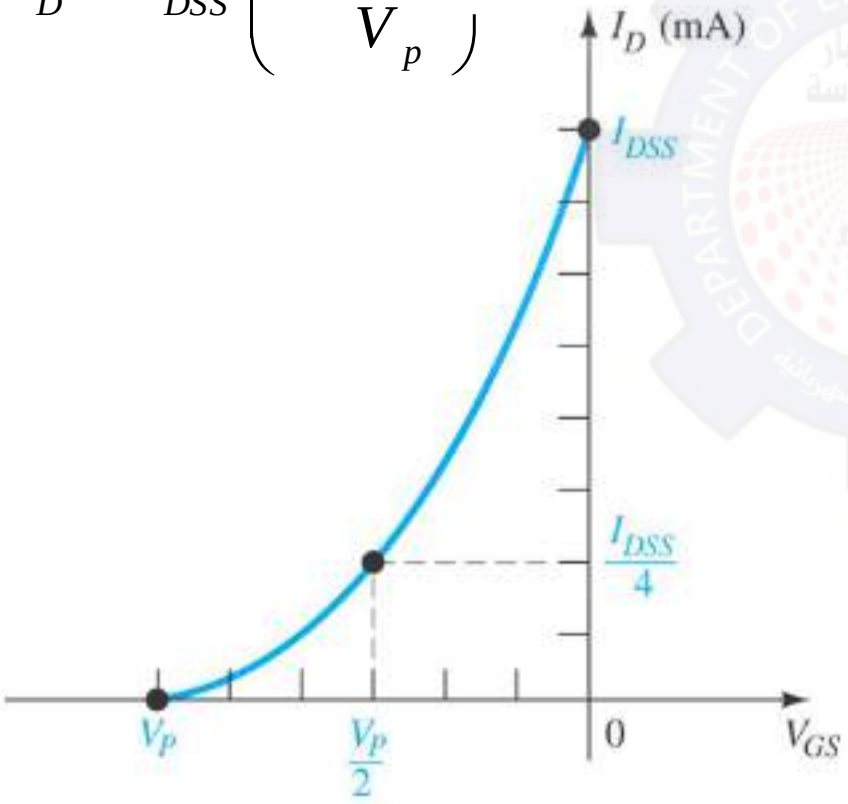
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$



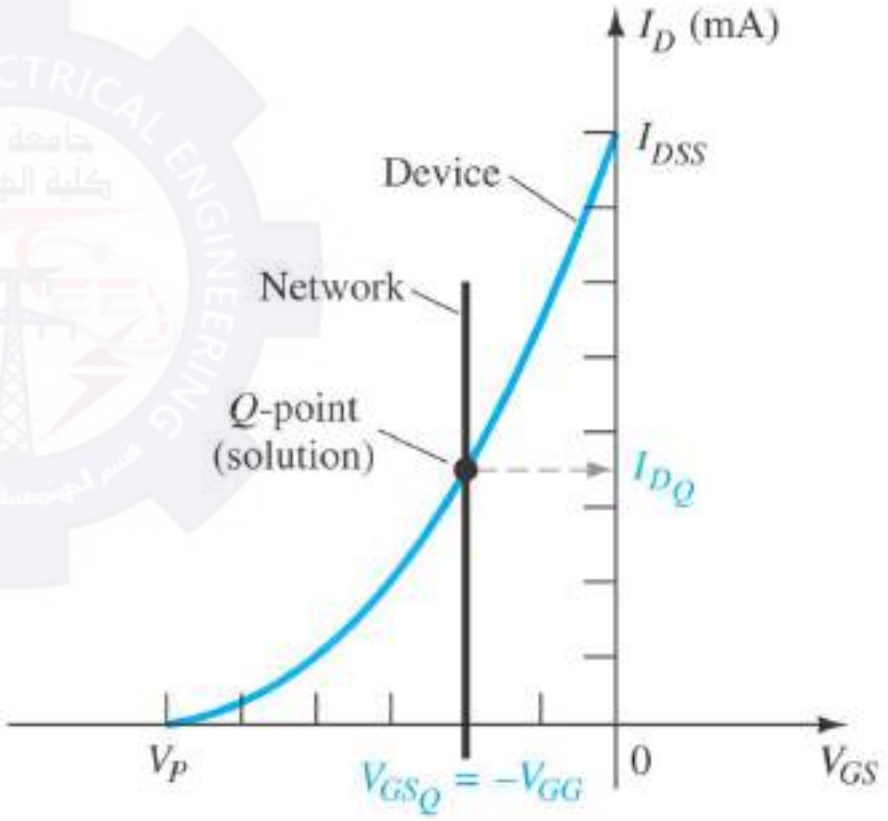
Network for dc analysis.

Fixed-Bias Configuration –Graphical Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$



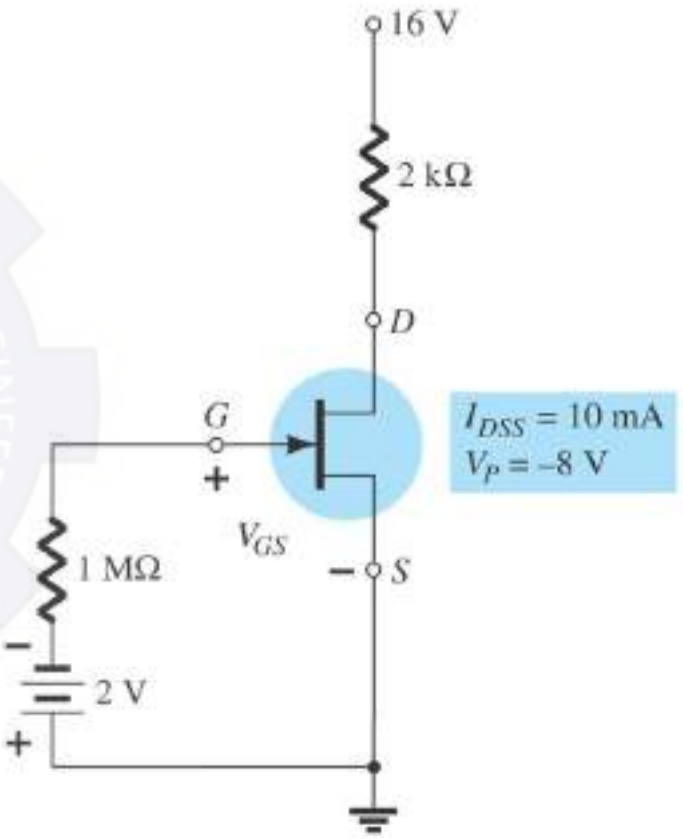
Plotting Shockley's equation.



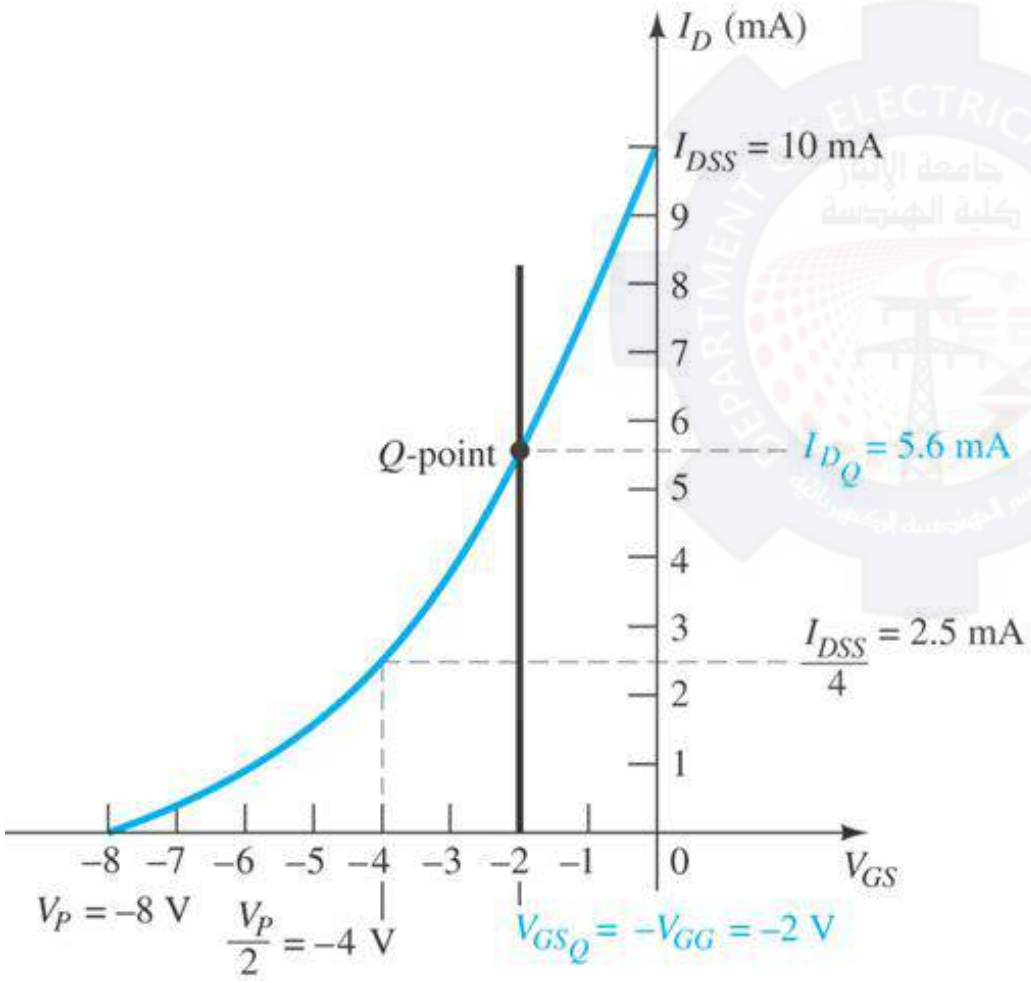
Finding the solution for the fixed-bias configuration.

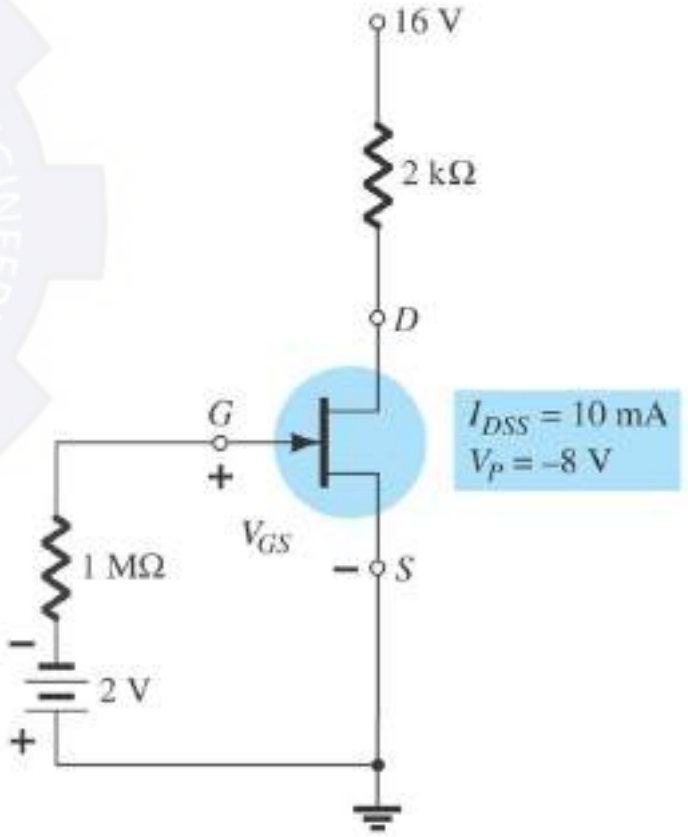
Example 7.1

Find V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S.

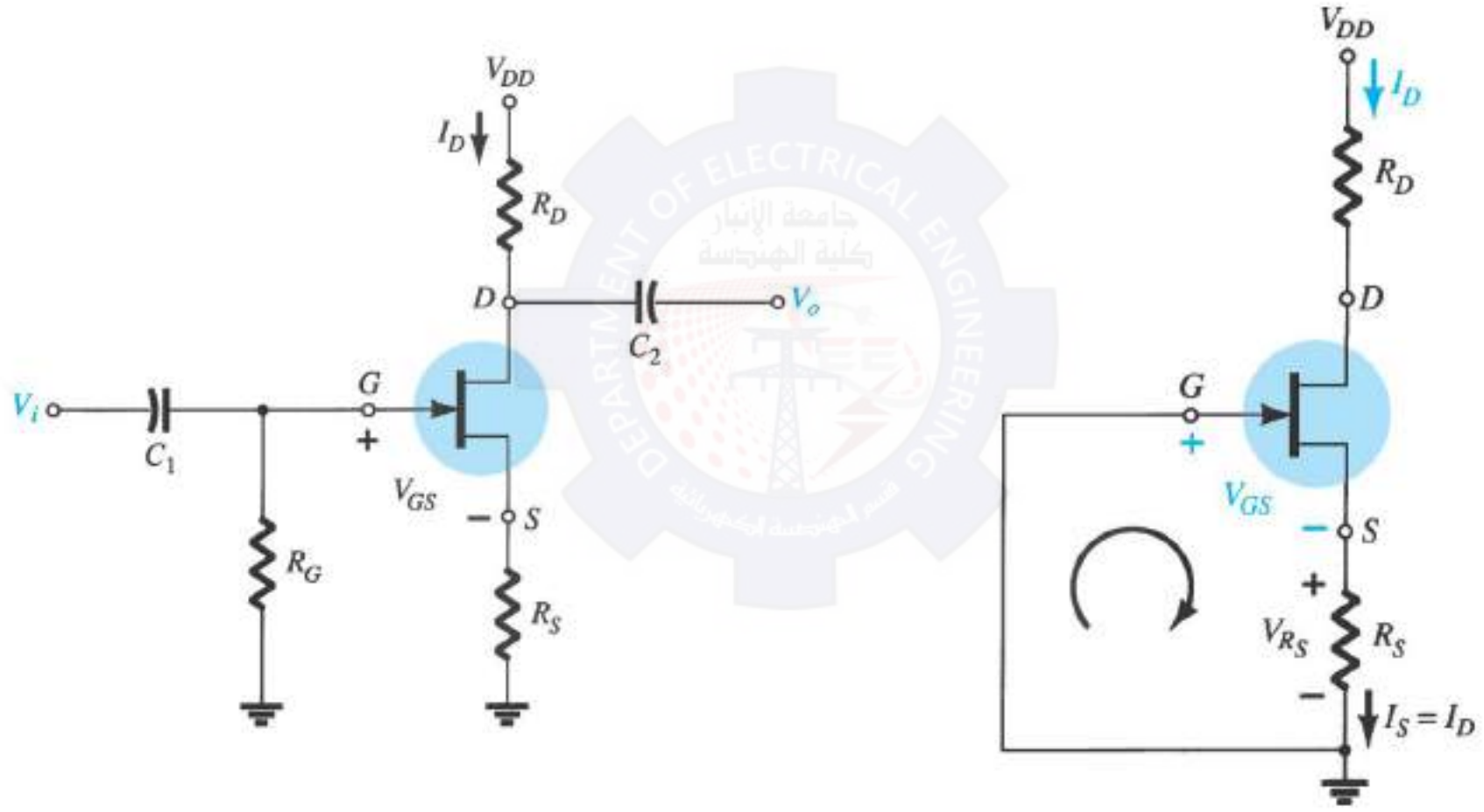


Example 7.1 - graphical solution





Self-Bias Configuration



DC analysis of the self-bias configuration.

Self-Bias Configuration

$$V_{GS} = -I_D R_S$$

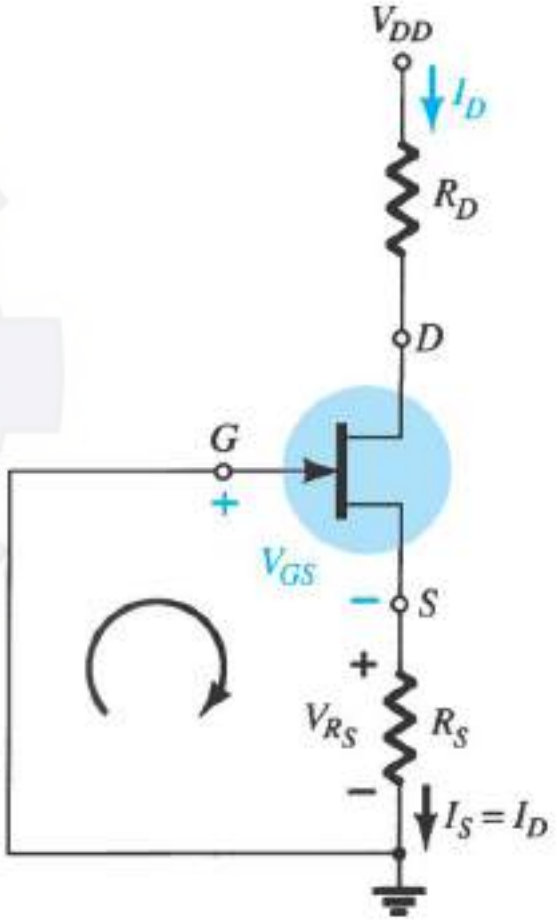
$$I_D = I_{DSS}\left(1 \quad \frac{V_{GS}}{V_p}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2$$

By squaring and rearranging, I_D has the form:

$$I_D^2 + k_1 I \quad + k_2 = 0 \quad [\text{Solve for } I_D]$$



DC analysis of the self-bias configuration.

Self-Bias Configuration – graphical solution

- Sketch the transfer curve.
- Draw the line:

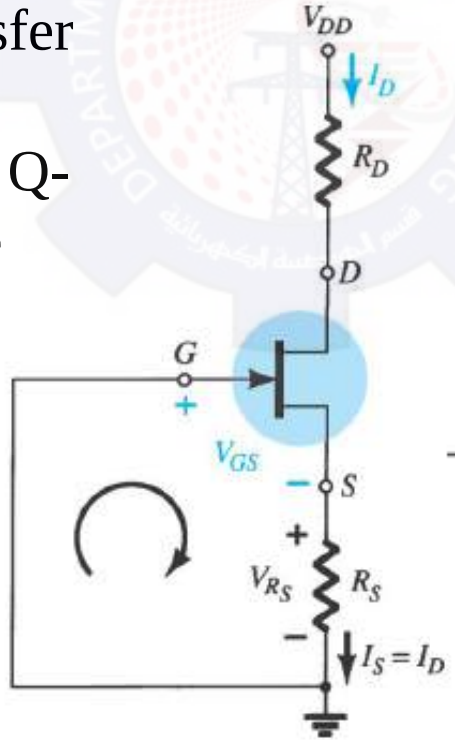
$$\mathbf{V_{GS} = -I_D R_S}$$

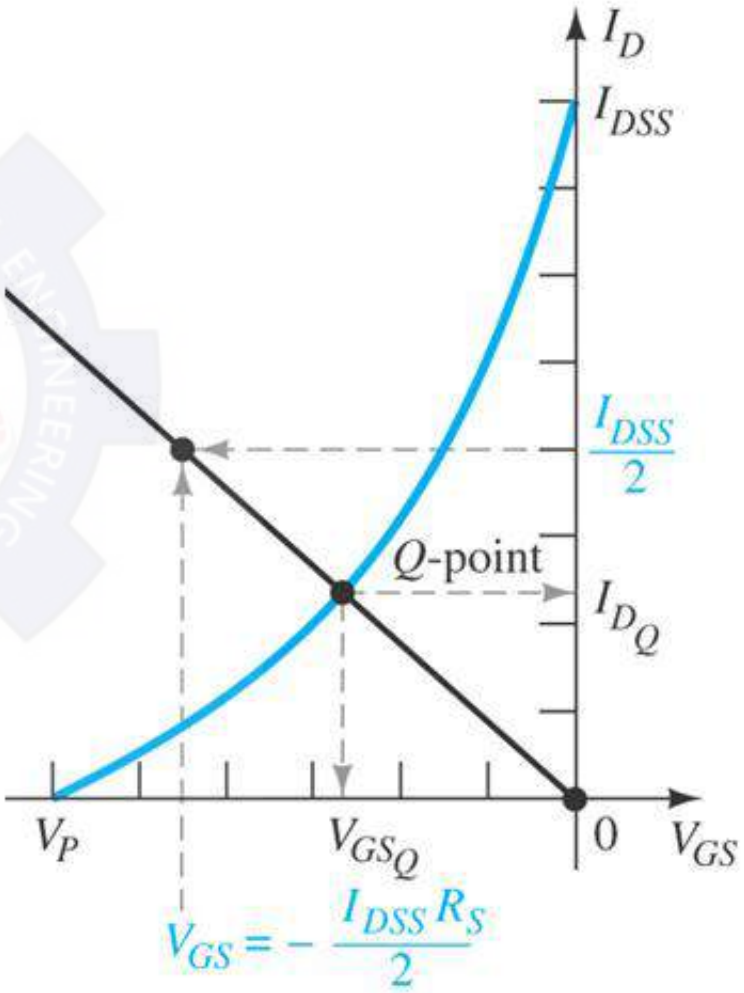
- The Q-point is located where the line intersects the transfer curve.
- Use the value of I_D at the Q-point (I_{DQ}) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D (R_S + R_D$$

$$V_S = I_D R_S$$

$$V_D \quad V_{DS} + V_S$$



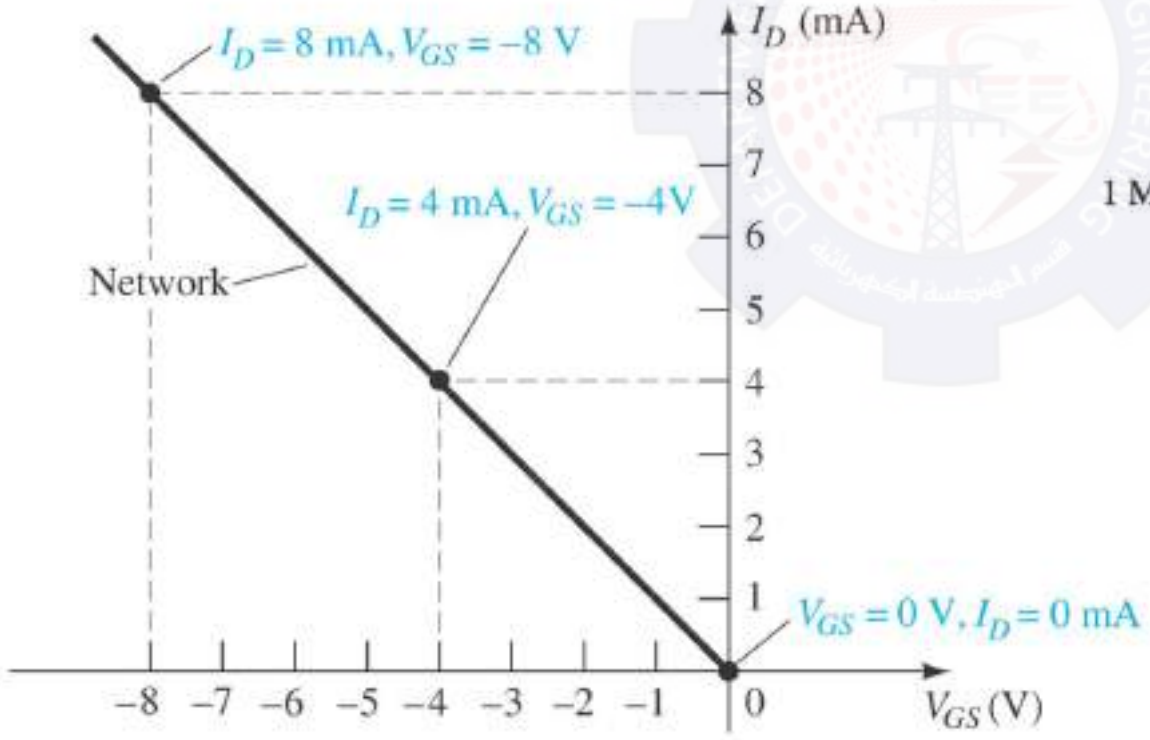


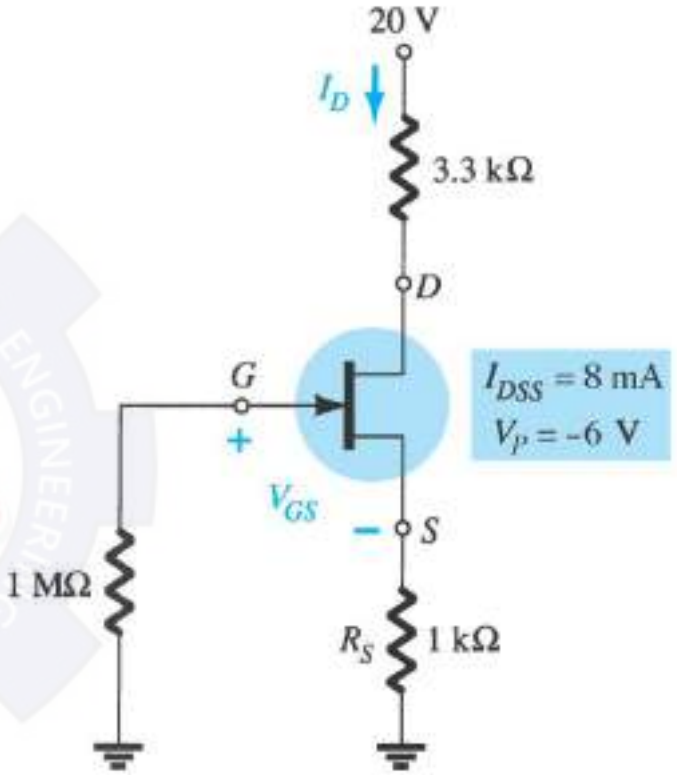
Example 7.2

Find V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S.

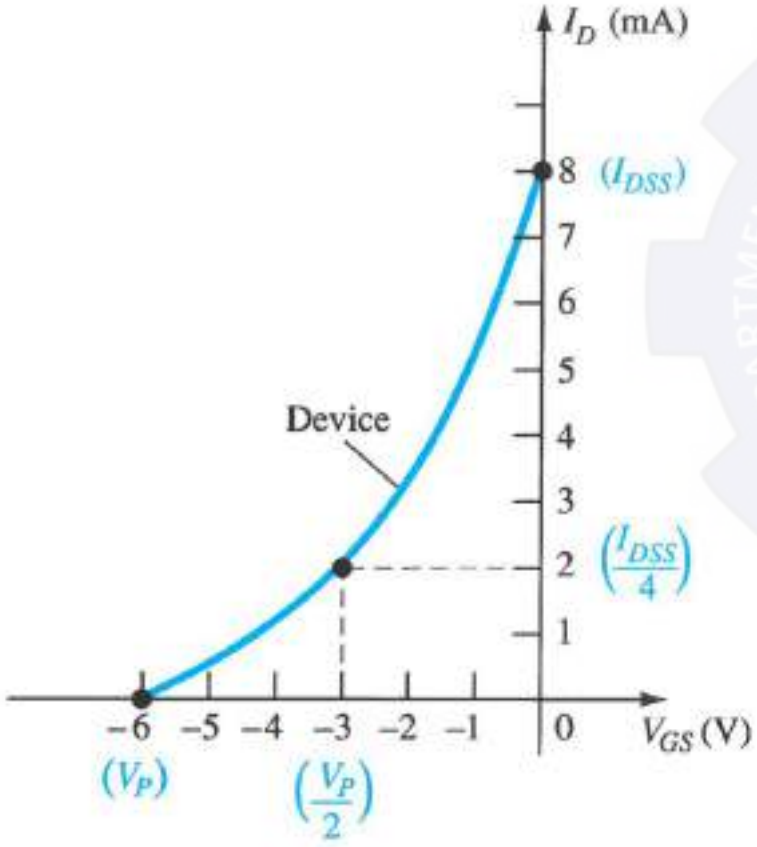
Solution

Draw the line: $\mathbf{V_{GS} = -I_D R_S}$

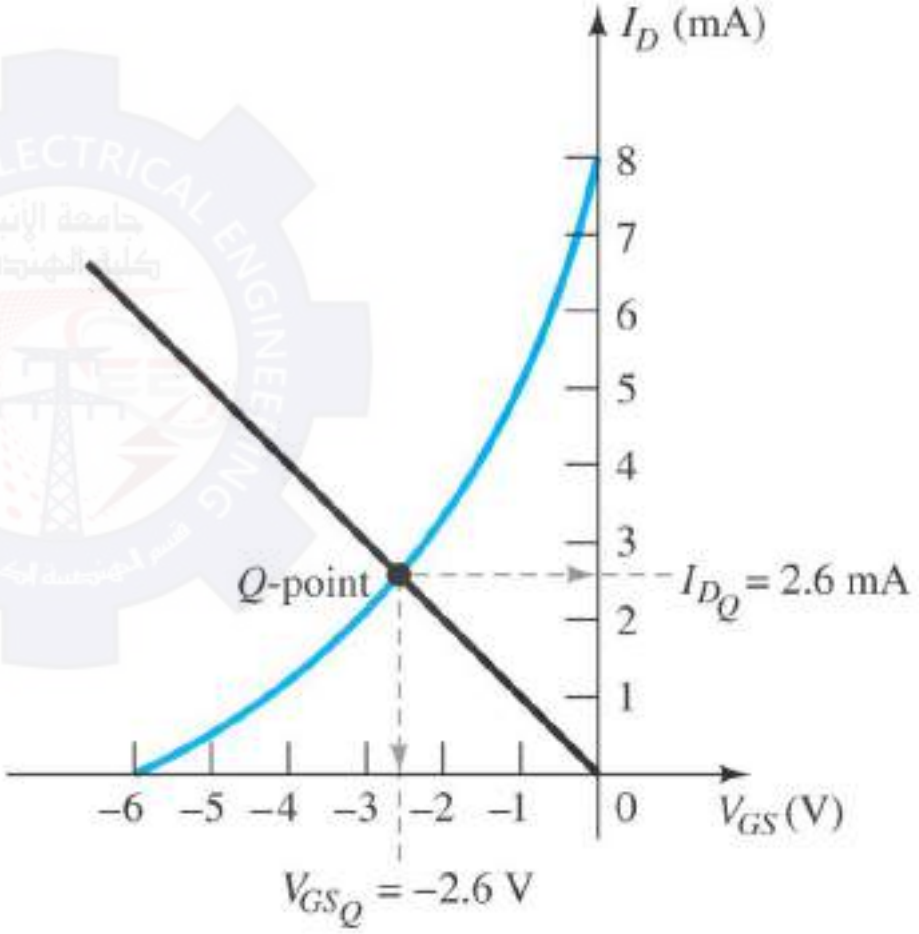




Example 7.2 - solution



Sketching the device characteristics for the JFET



Determining the *Q*-point for the network.

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Chapter 7 : FET Biasing

Lec07_p2

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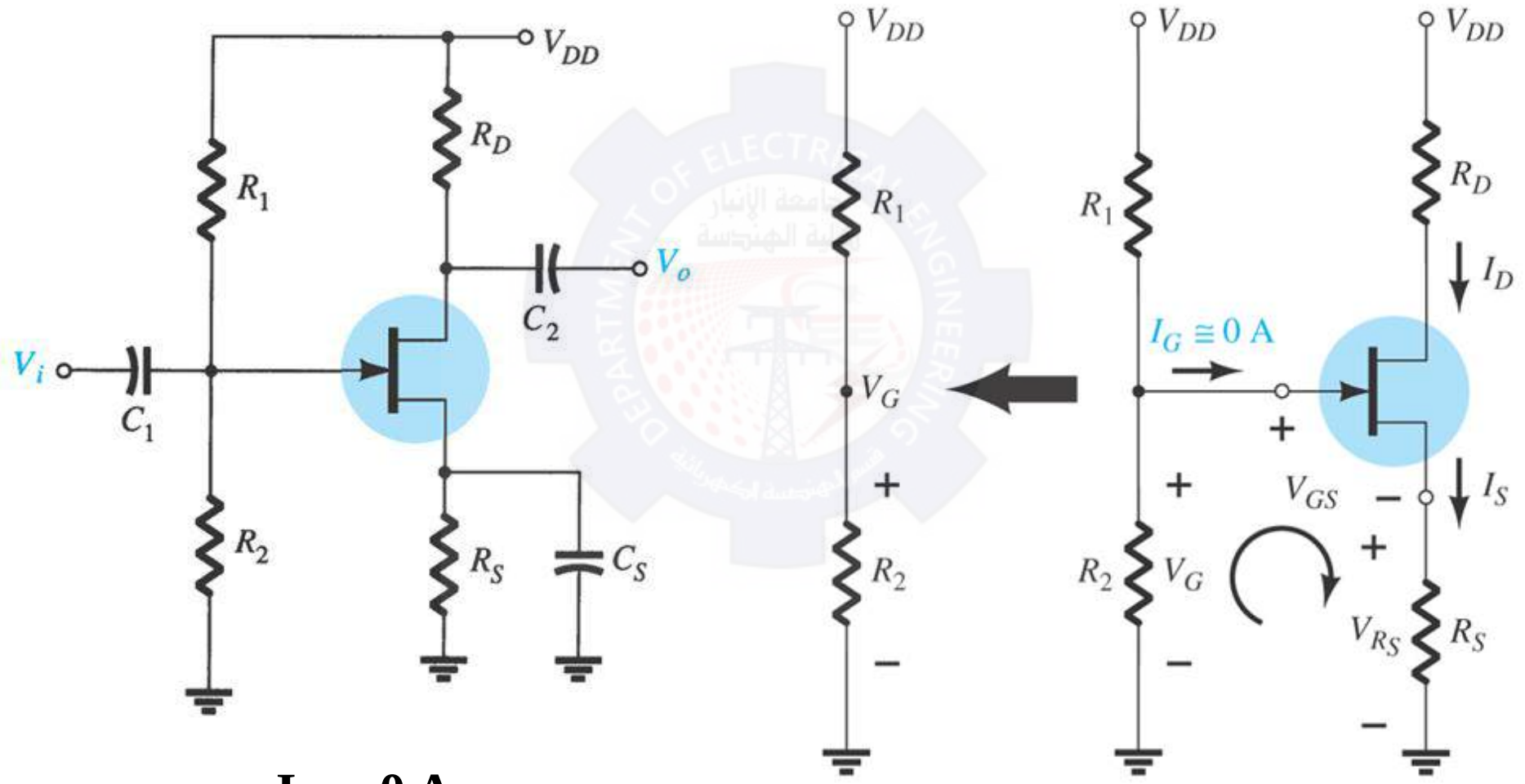
2019-2020

Voltage-Divider Bias



$I_G = 0$ A

$I_{R1}=I_{R2}$

Redrawn network for dc analysis.

Voltage-Divider Bias

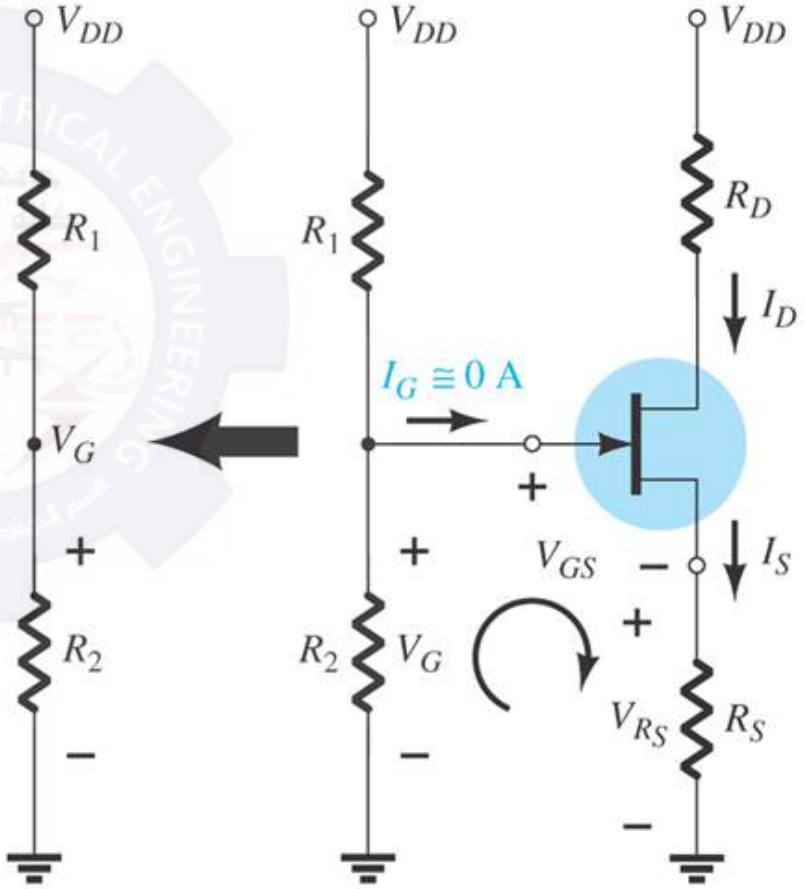
V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.



Voltage-Divider Bias

Step 1

$$V_{GS} = V_G - I_D R_S$$

Plot the line by plotting two points:

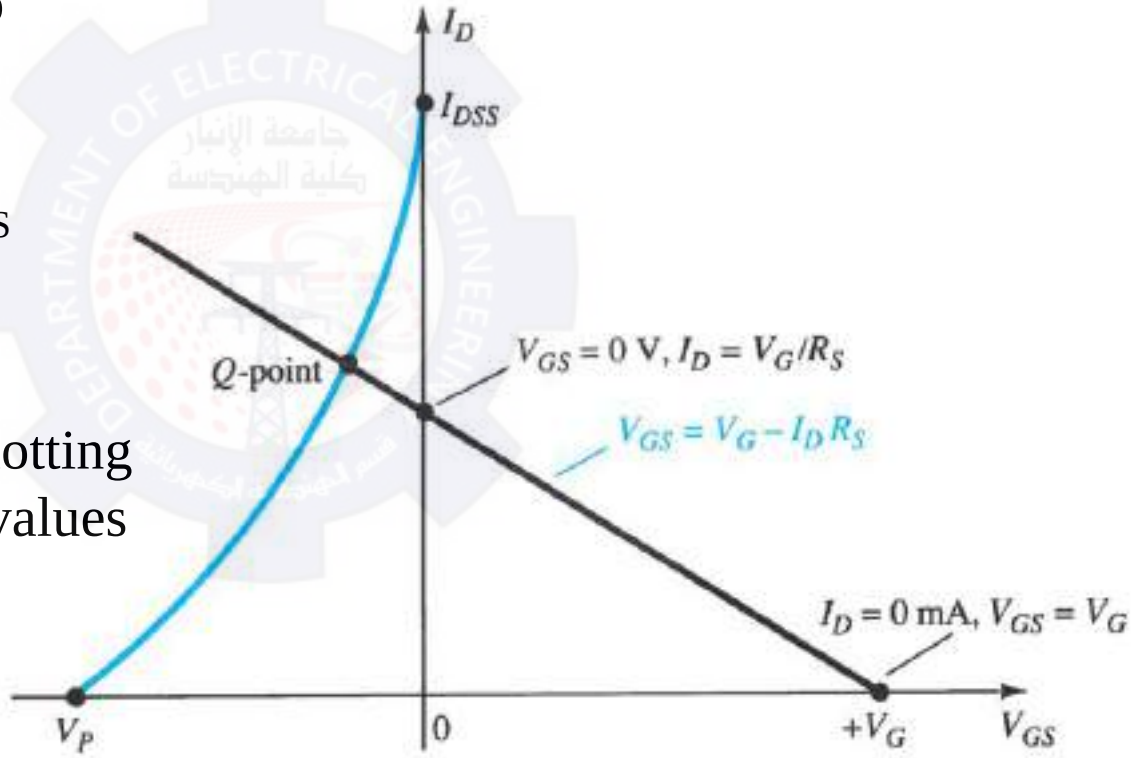
- $V_{GS} = V_G$, $I_D = 0$ A
- $V_{GS} = 0$ V, $I_D = V_G / R_S$

Step 2

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

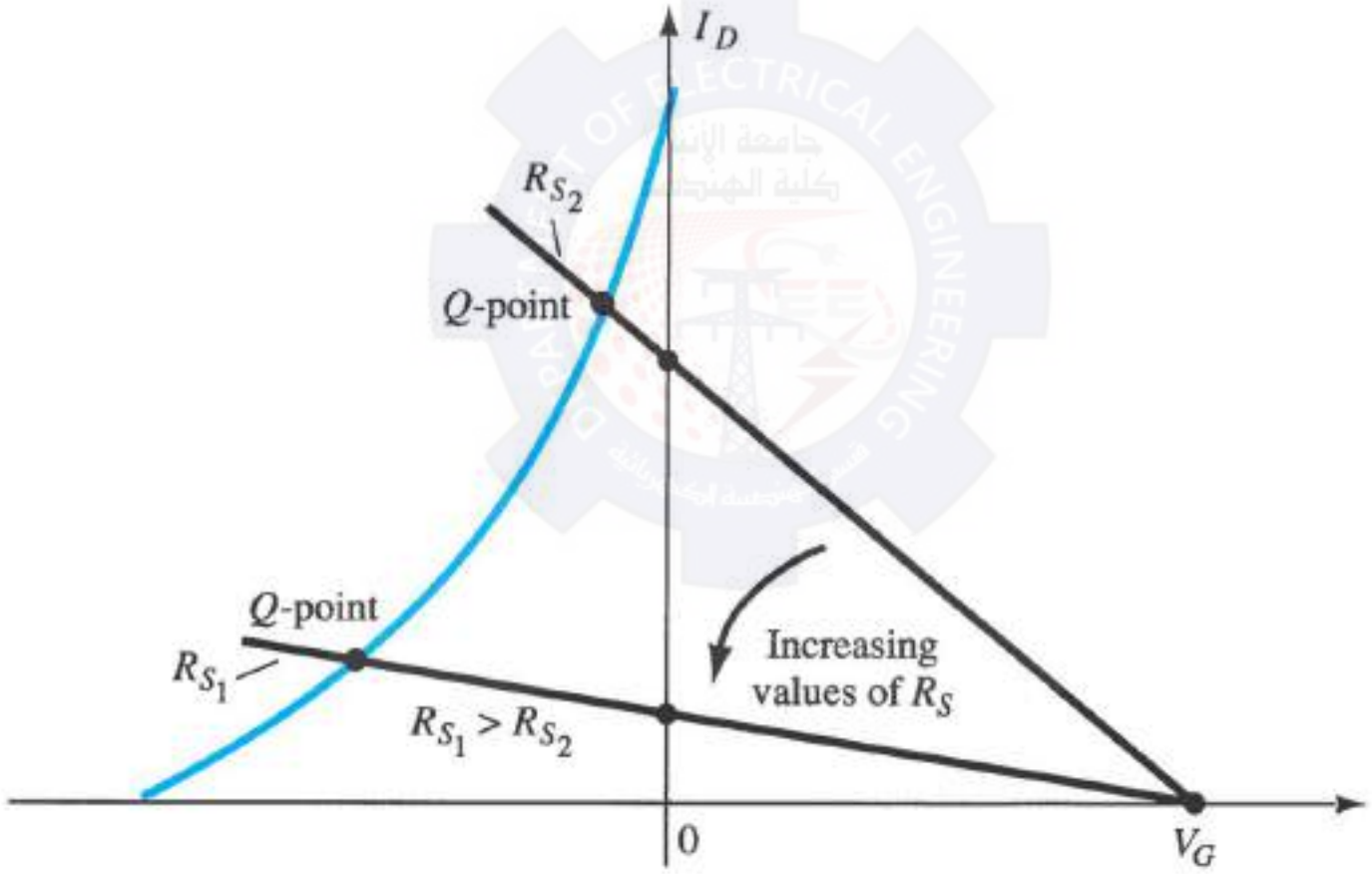
Step 3

The Q-point is located where the line intersects the transfer curve



Voltage-Divider Bias

$$V_{GS} = V_G - I_D R_S$$



Effect of R_S on the resulting Q-point.

Voltage-Divider Bias

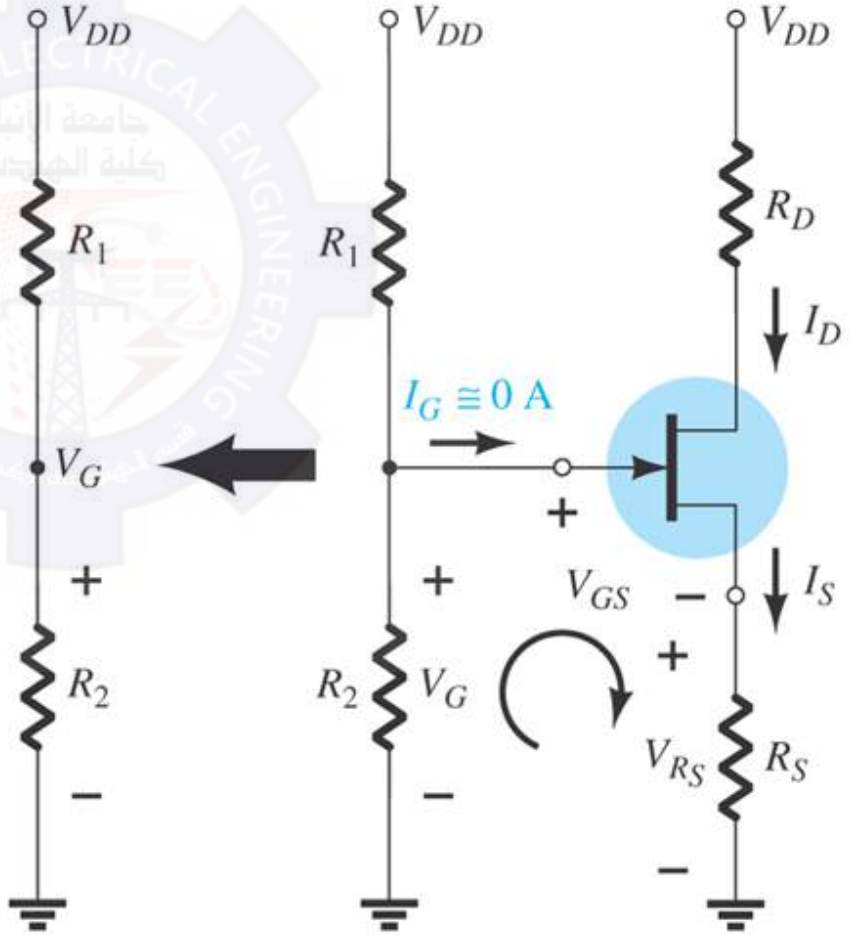
Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

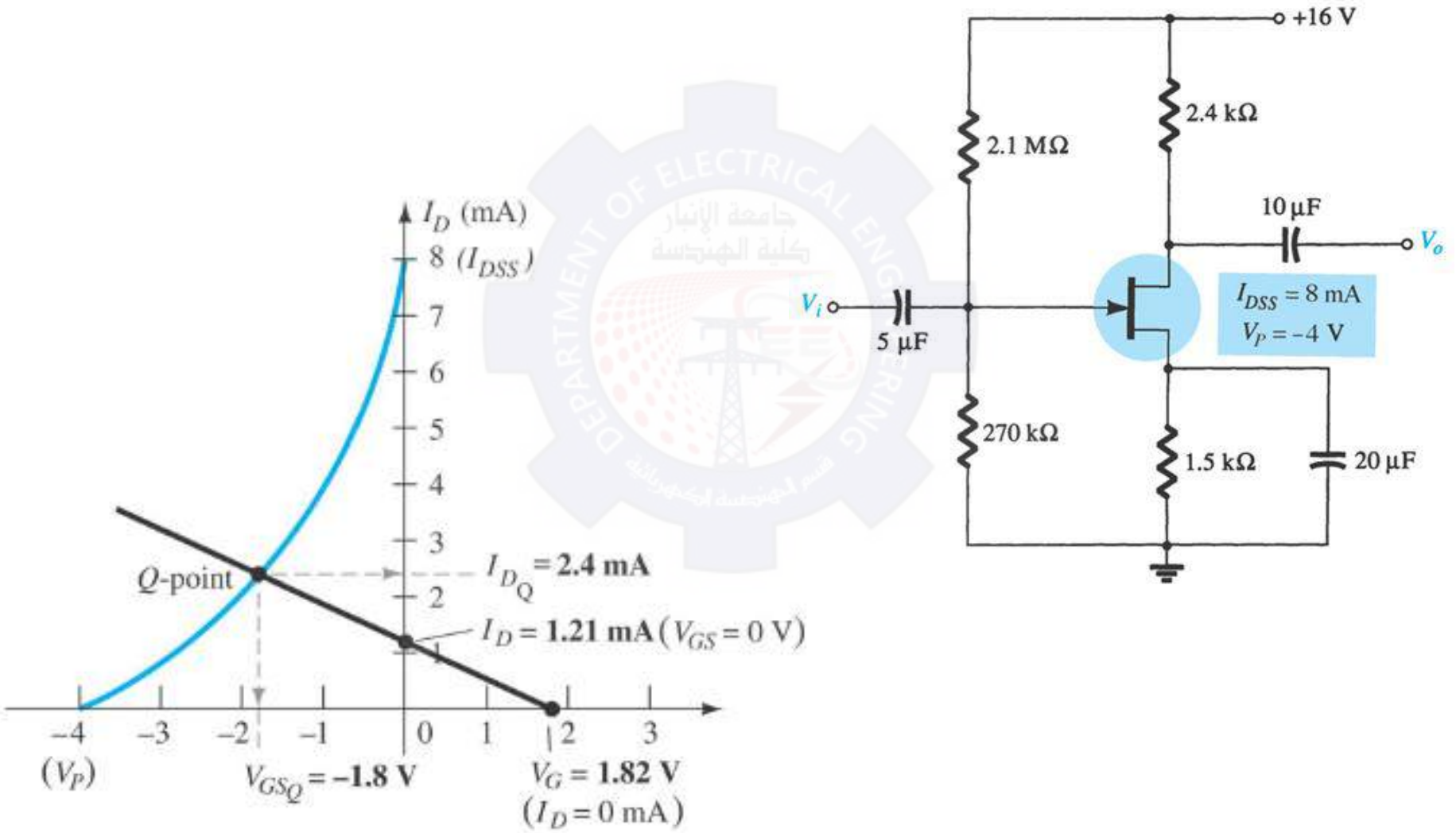
$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$



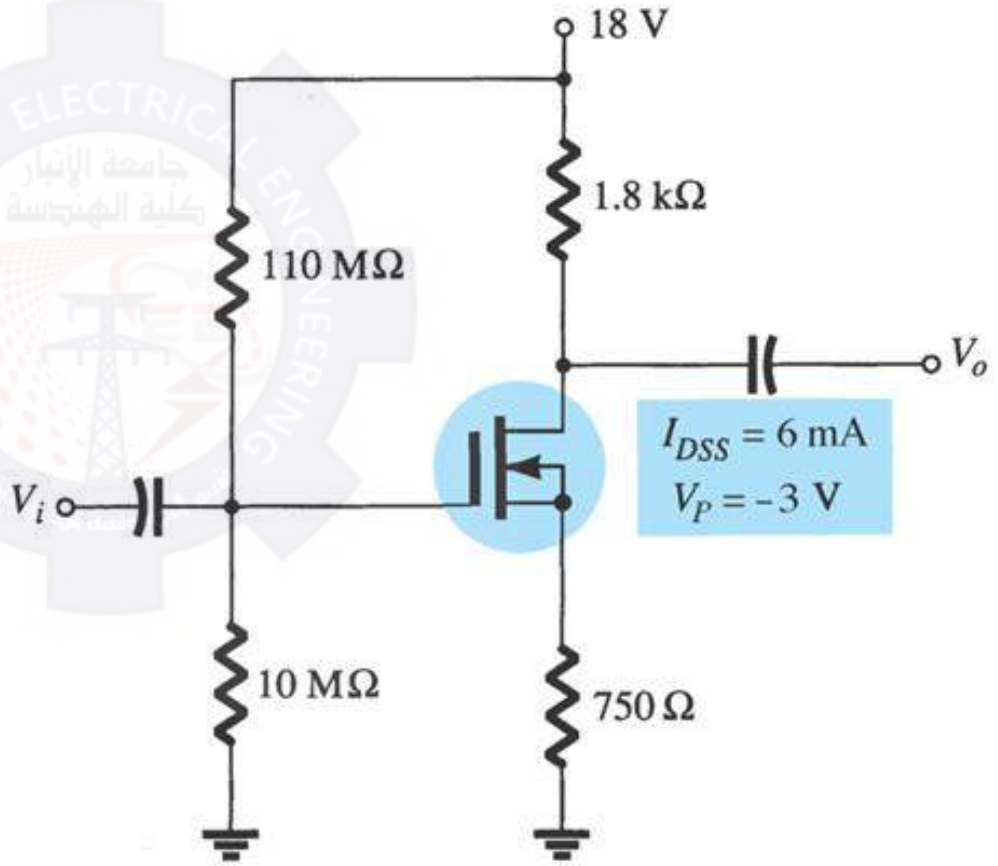
Example 7.5

Find V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S.



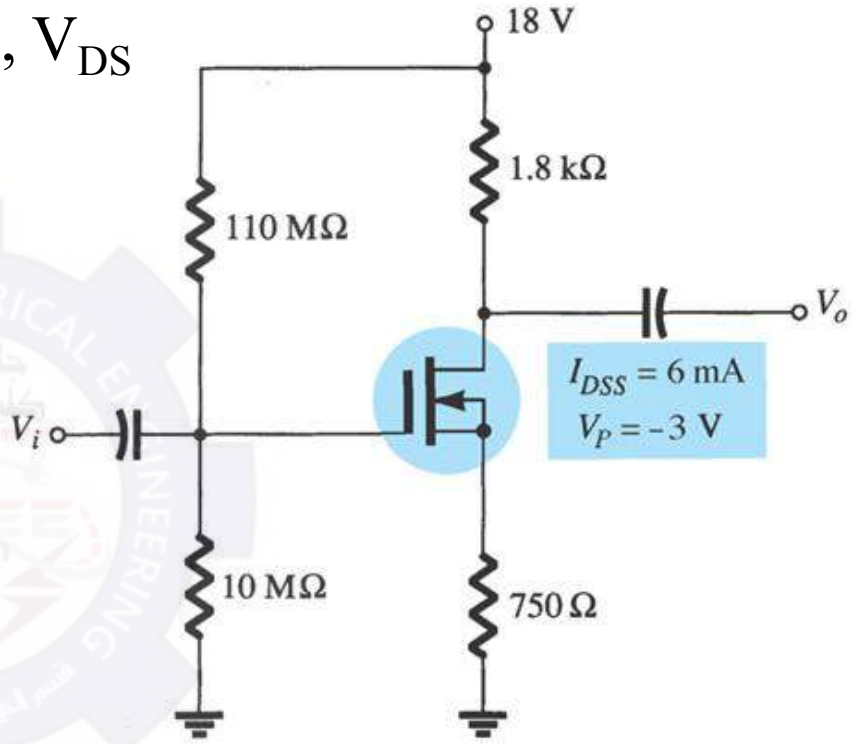
D-Type MOSFET Bias Circuits

Depletion-type MOSFET bias circuits are similar to those used to bias JFETs.
The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.



Example 7.7

Find V_{GSQ}, I_{DQ}, V_{DS}



Step 1

Plot the line for

- $V_{GS} = V_G$, $I_D = 0$ A
- $I_D = V_G/R_S$, $V_{GS} = 0$ V

Step 2

Plot the transfer curve using I_{DSS}, V_P and calculated values of I_D.

Step 3

The Q-point is located where the line intersects the transfer curve is. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

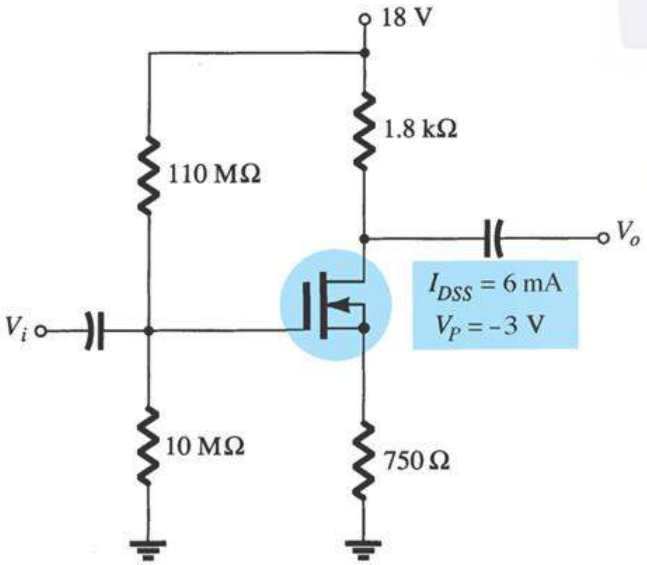
These are the same steps used to analyze JFET voltage-divider bias circuits.

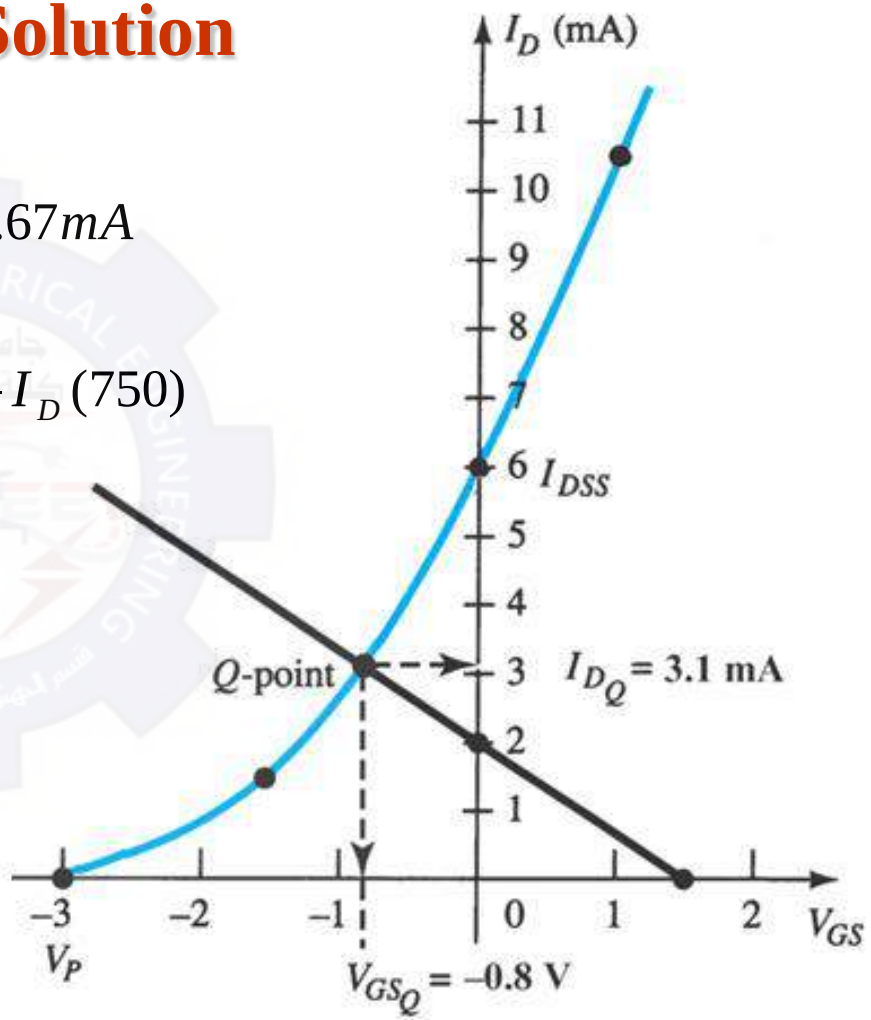
Example 7.7 - Solution

$$For\ V_{GS} = +1V$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 6\text{mA}\left(1 - \frac{+1}{-3}\right)^2 = 10.67mA$$

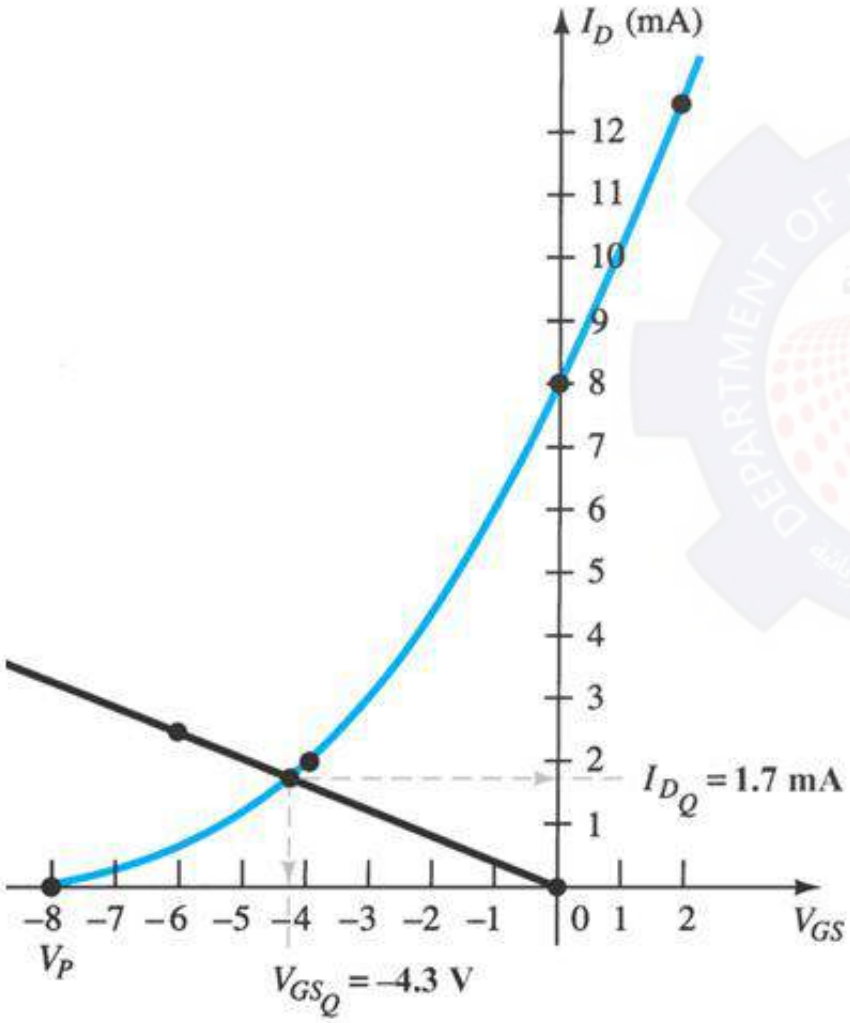
$$V_G = \frac{10M\,(18V)}{10M + 110M} = 1.5V \rightarrow V_{GS} = 1.5V - I_D(750)$$

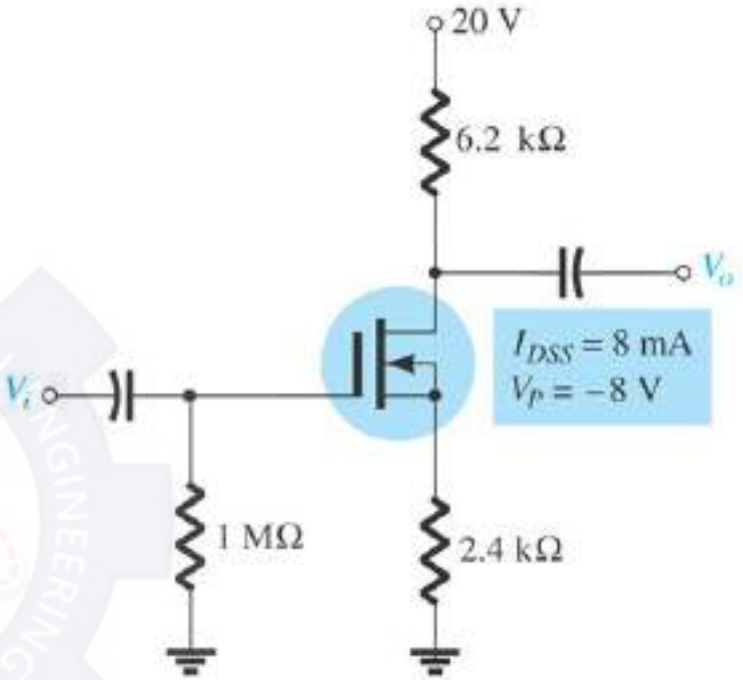




$$\mathbf{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \qquad \mathbf{V_{GS} = V_G - I_D R_S}$$

Example 7.9 Find V_{GSQ}, I_{DQ}, V_D





To plot line $V_{GS} = -I_D R_S$:

$I_D = -V_{GS} / R_S$

For $V_{GS} = -6$, $I_D = -(-6)/2.4k = 2.5mA$

To plot transfer curve for V_{GS}=+2V:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 8m\left(1 - \frac{+2}{-8}\right)^2 = 12.5mA$$

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Chapter 7 : FET Biasing
Lec07_p3

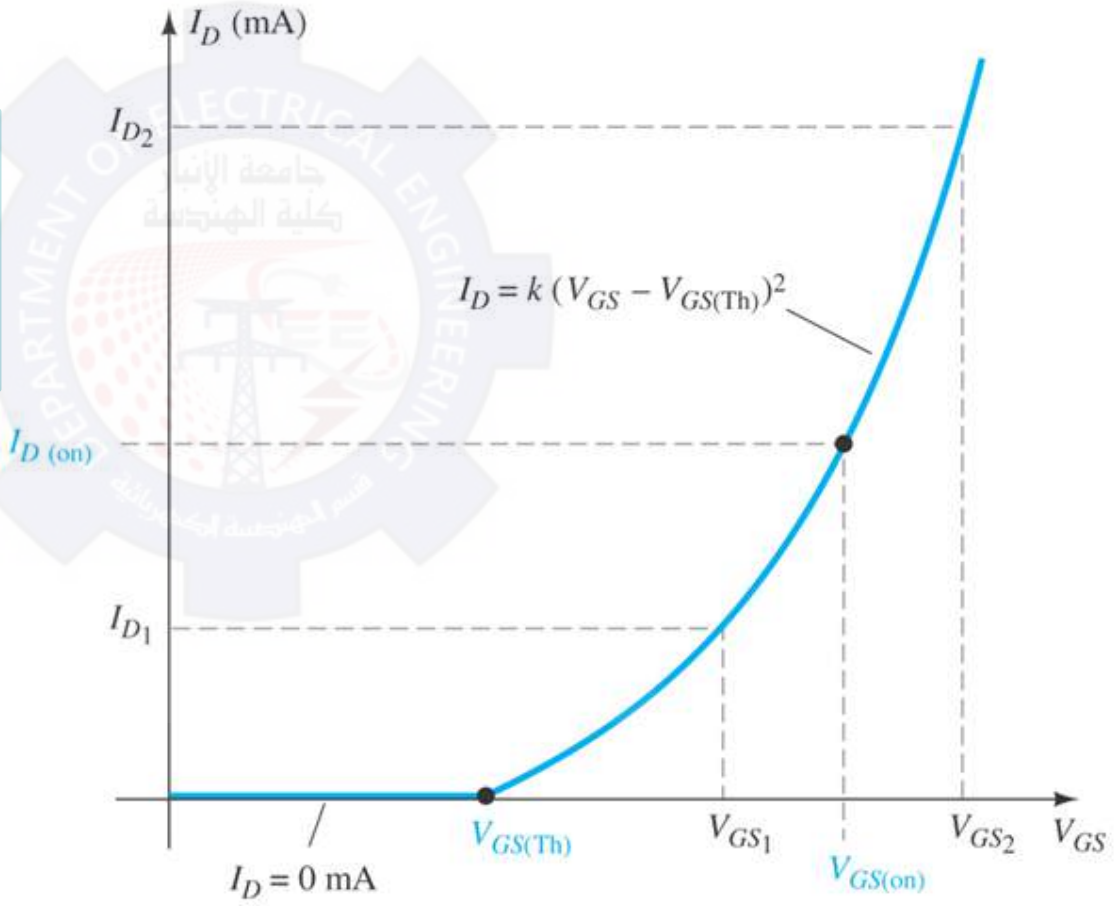
Munther N. Thiyab

2019-2020

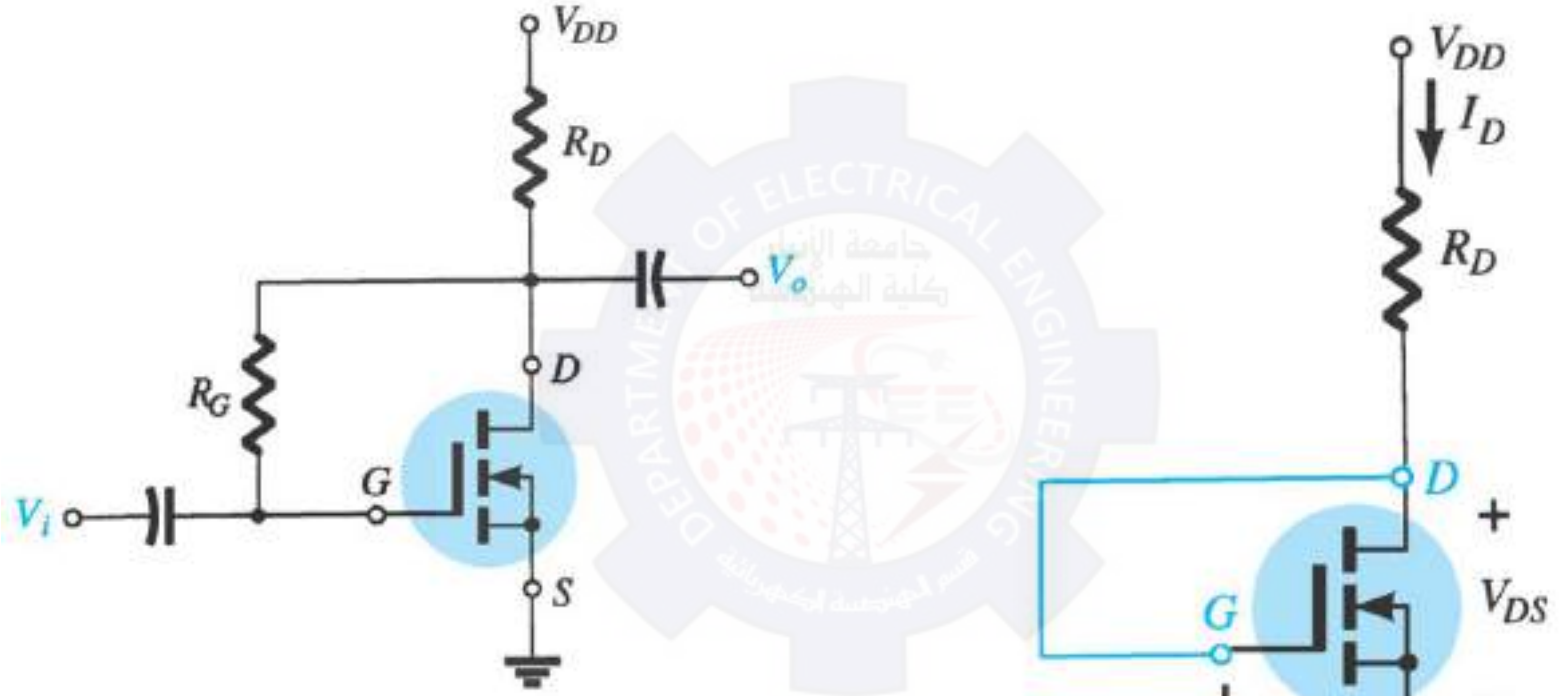
E-Type MOSFET Bias Circuits

The transfer characteristic for the e-type MOSFET is very different from that of a simple JFET or the d-type MOSFET.

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2$$



Feedback Bias Circuit



DC equivalent of the network

$I_G = 0\ A$

$V_{RG} = 0\ V$

$V_{DS} = V_{GS}$

$$\mathbf{V_{GS} = V_{DD} - I_D R_D}$$

Feedback Bias Q-Point

Step 1

Plot the line using

- $V_{GS} = V_{DD}$, $I_D = 0$ A
- $I_D = V_{DD} / R_D$, $V_{GS} = 0$ V

Step 2

Using values from the specification sheet, plot the transfer curve with

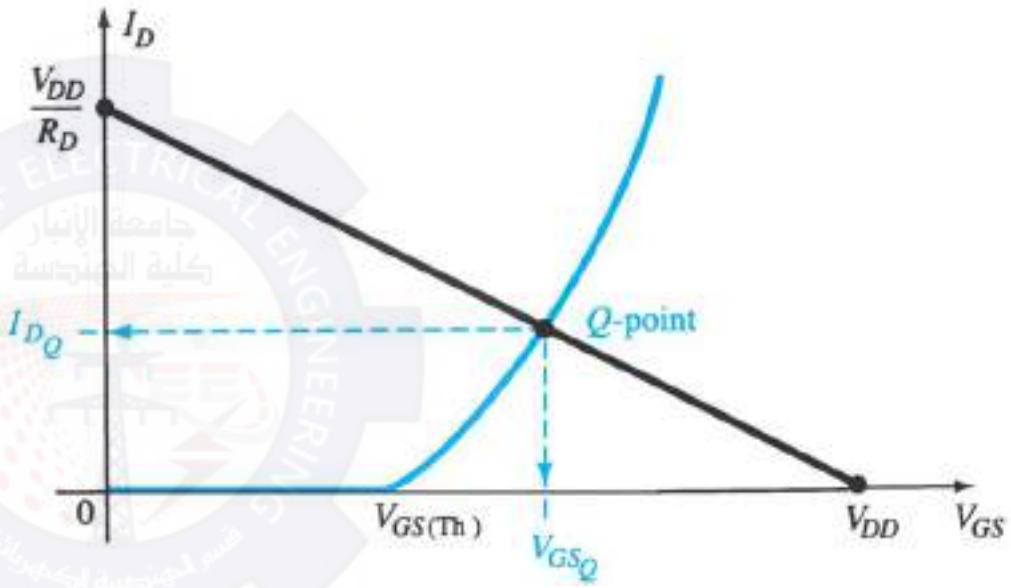
- V_{GSTh} , $I_D = 0$ A
- $V_{GS(on)}$, $I_{D(on)}$

Step 3

The Q-point is located where the line and the transfer curve intersect

Step 4

Using the value of I_D at the Q-point, solve for the other variables in the bias circuit.



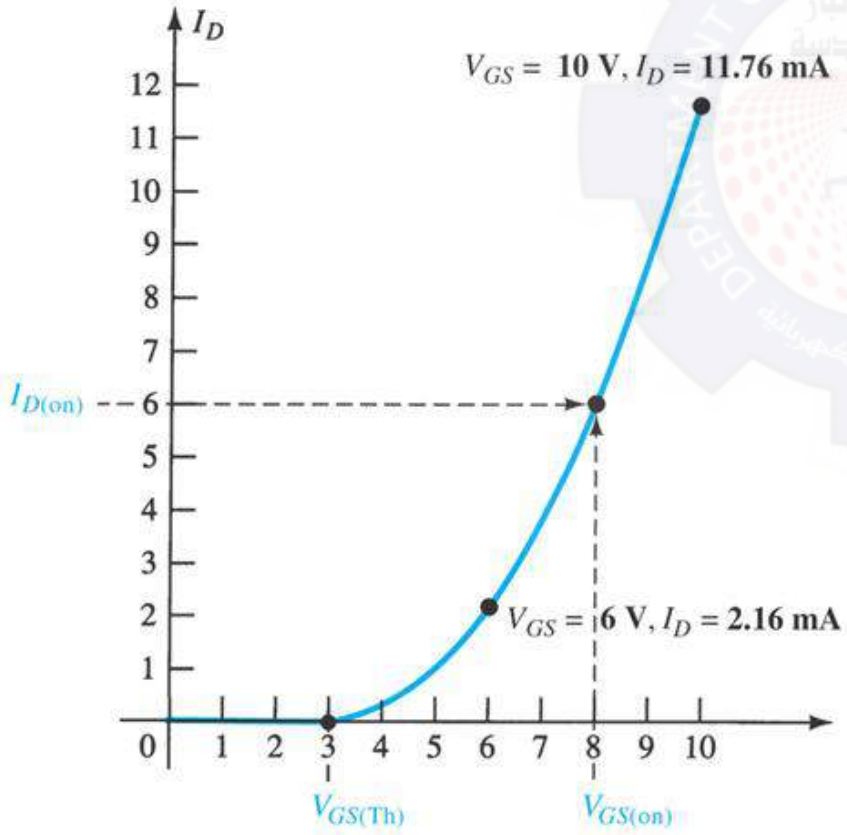
$$V_{GS} = V_{DD} - I_D R_D$$

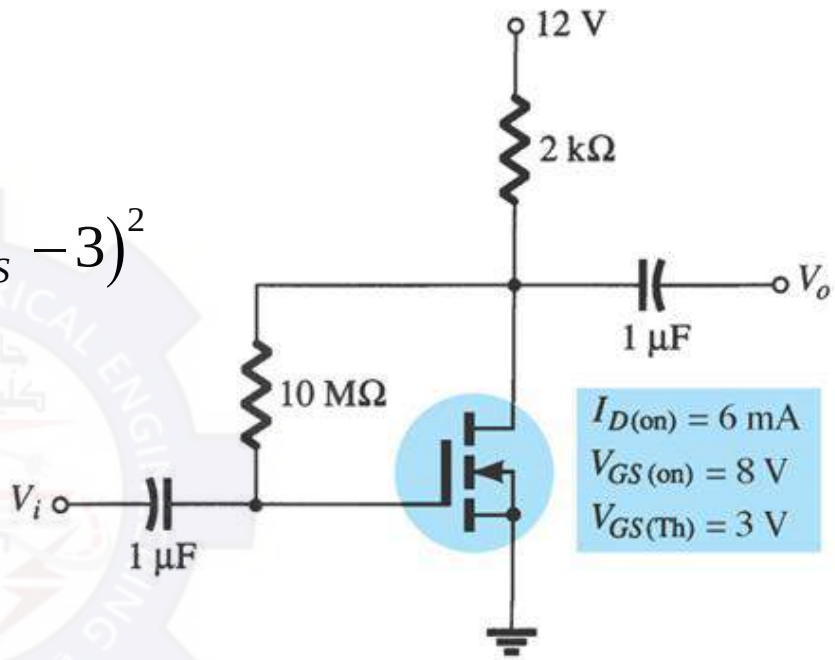
Example 7.11

Find V_{GSQ}, I_{DQ}

Plot Transfer Curve:

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2 = 0.24\times10^{-3}\left(V_{GS} - 3\right)^2$$





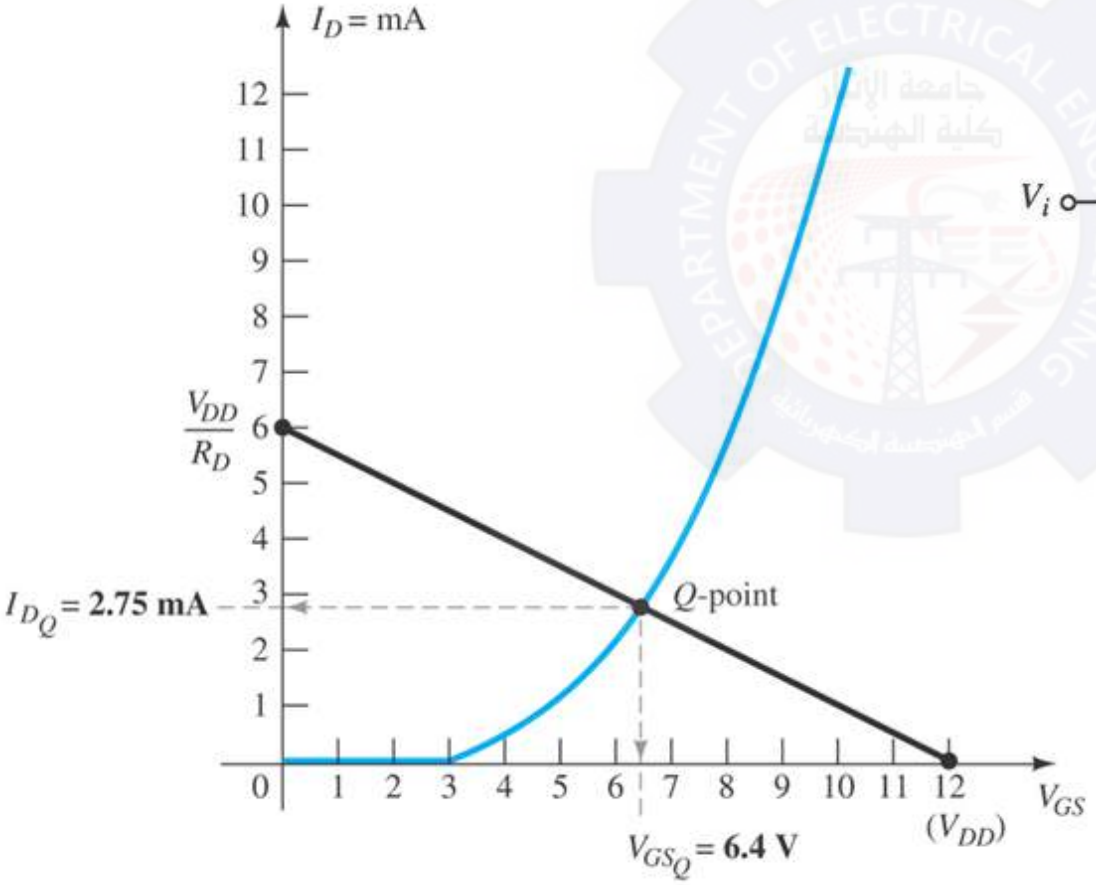
$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_{GS(Th)}\right)^2}$$

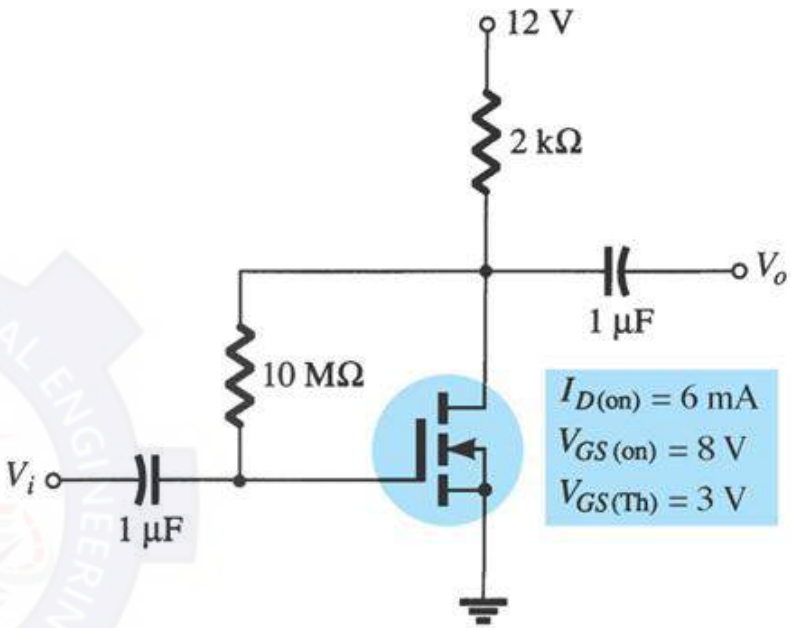
$$k = \frac{6mA}{\left(8 - \quad\right)^2} = 0.24\times10^{-3}$$

Example 7.11 - solution

Plot the line : $V_{GS} = V_{DD} - I_D R_D$

$V_{GS} = 12 - I_D(2k)$





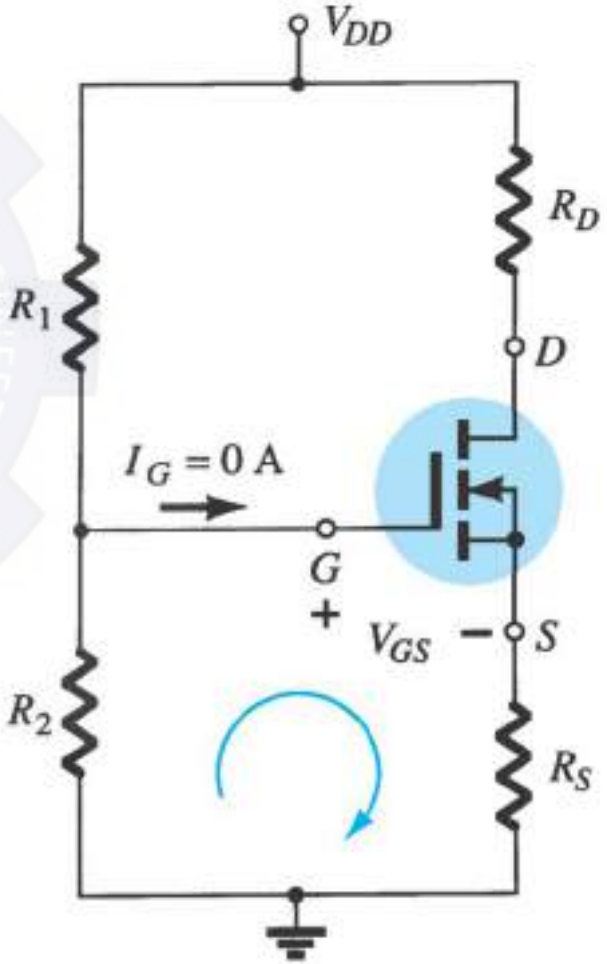
Voltage-Divider Biasing

Plot the line and the transfer curve to find the Q-point. Use these equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$



Example 7.12

Find V_{GSQ}, I_{DQ}

$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_{GS(Th)}\right)^2}$$

$$k = \frac{3mA}{(10-5)^2} = 0.12\times10^{-3}$$

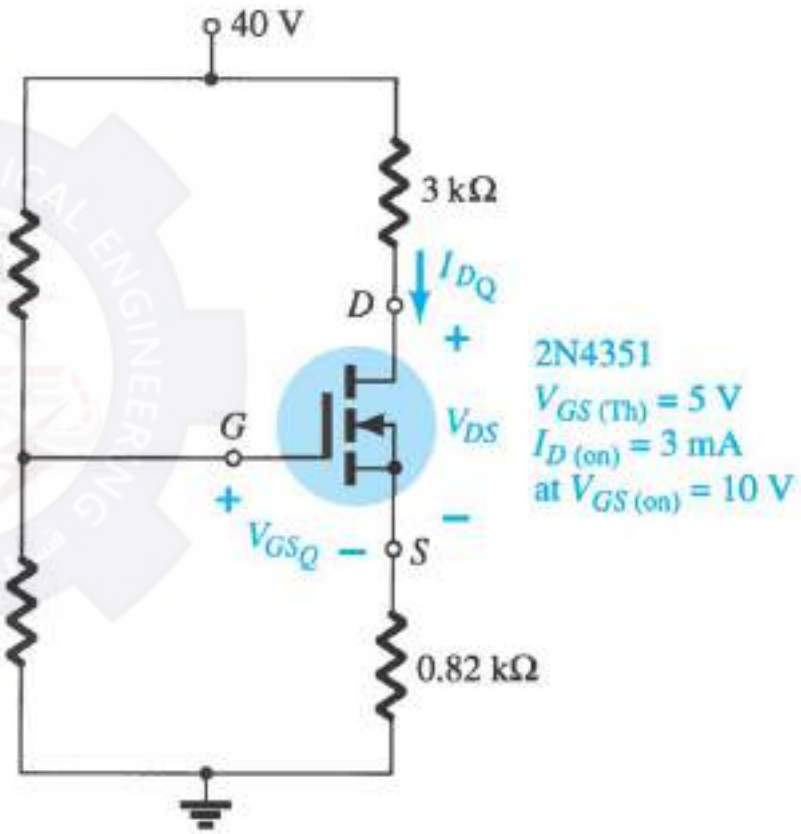
$$I_D = k\left(V_{GS} - V_{GS(Th}\right)^2$$

$$\boxed{I_D = 0.12\times10^{-3}\left(\ _{GS} - 5\right)^2}$$

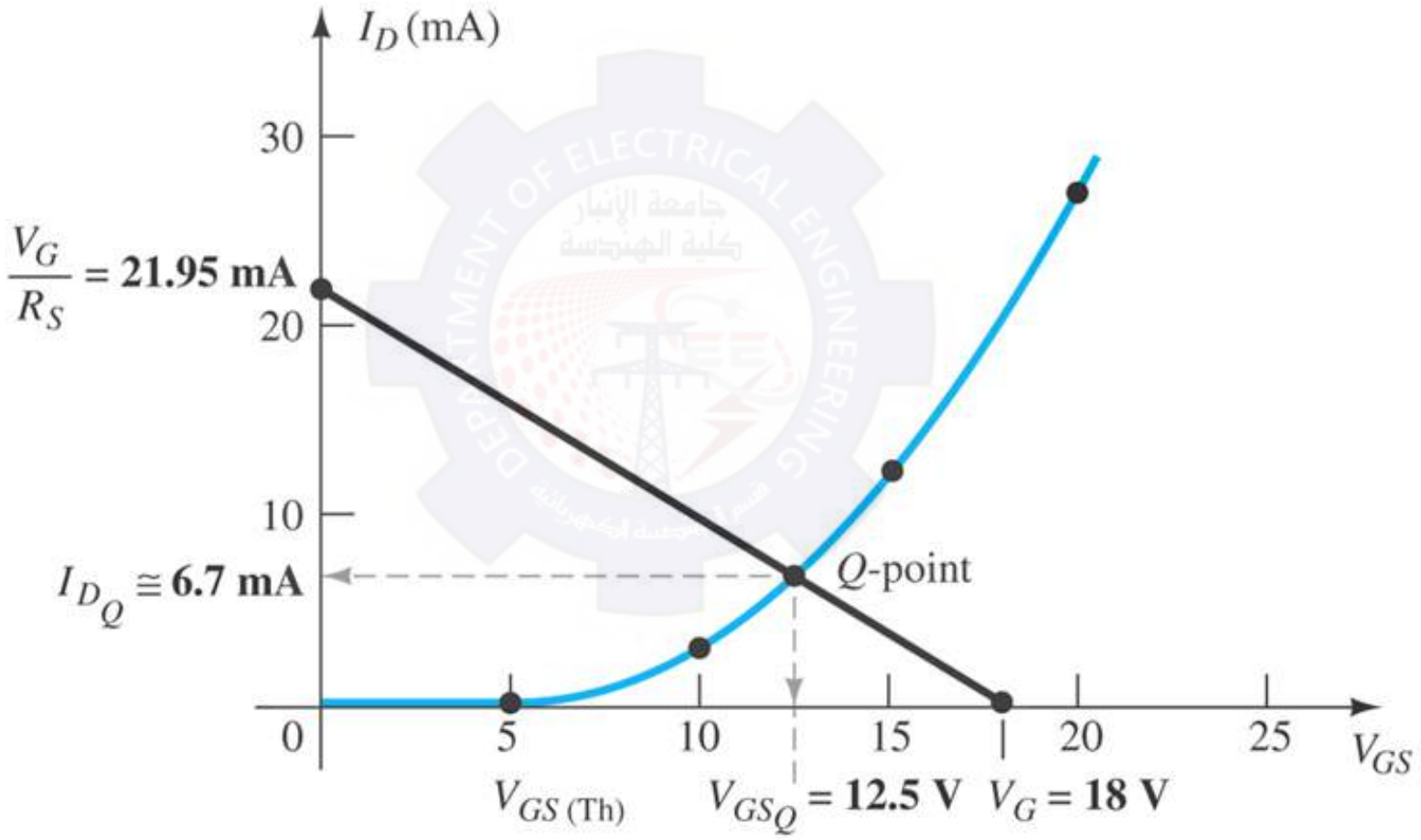
$$V_G \quad \frac{18M\ (40V\ )}{22M\ +18M} = 18V$$

$$V_{GS} = V_G \quad I_D R_S$$

$$\boxed{V_{GS} = 18V\ - I_D(0.82k\ )}$$



Example 7.12 - Solution



$$I_D = 0.12\times10^{-3}\left(V_{GS} - 5\right)^2$$

$$V_{GS} = 18V - I_D(0.82k)$$

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Chapter08: FET Amplifier

Lec08_p1

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2019-2020

Introduction

FETs provide:

- **Excellent voltage gain**
- **High input impedance**
- **Low-power consumption**
- **Good frequency range**

FET Small-Signal Model

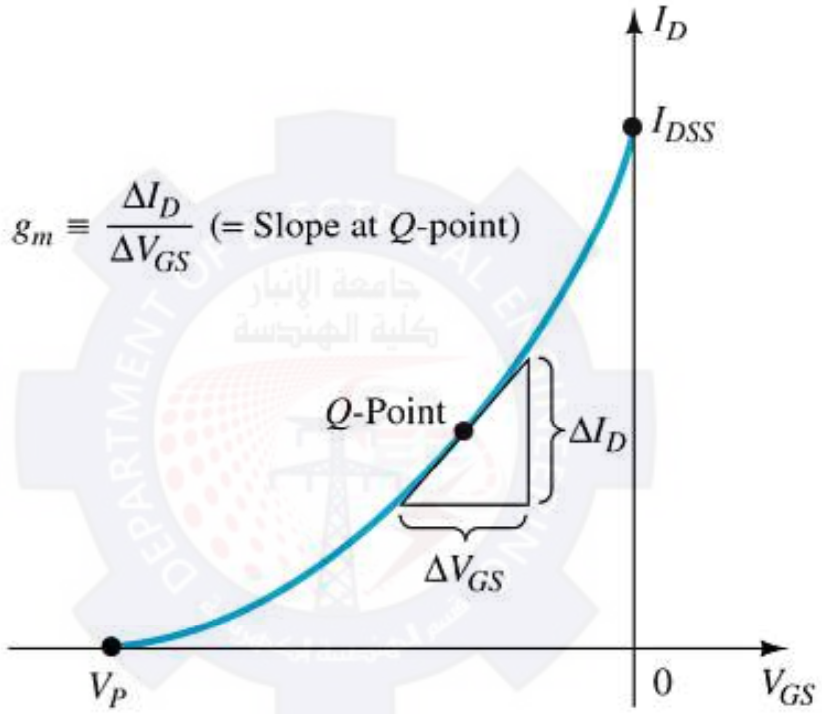
Transconductance

The relationship of a change in I_D to the corresponding change in V_{GS} is called transconductance

Transconductance is denoted g_m and given by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Graphical Determination of g_m



Mathematical Definitions of g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where $V_{GS} = 0V$ $\quad g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where $\quad 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

FET Impedance

Input impedance:

$$Z_i = \infty\Omega$$

Output Impedance:

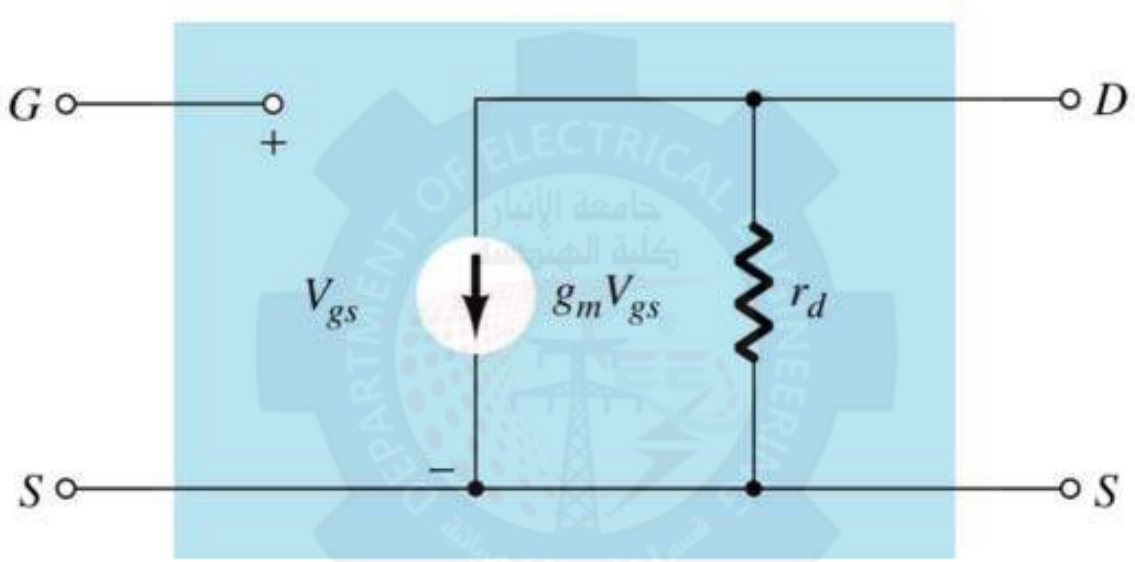
$$Z_o = r_d = \frac{1}{y_{os}}$$

where:

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{constant}}$$

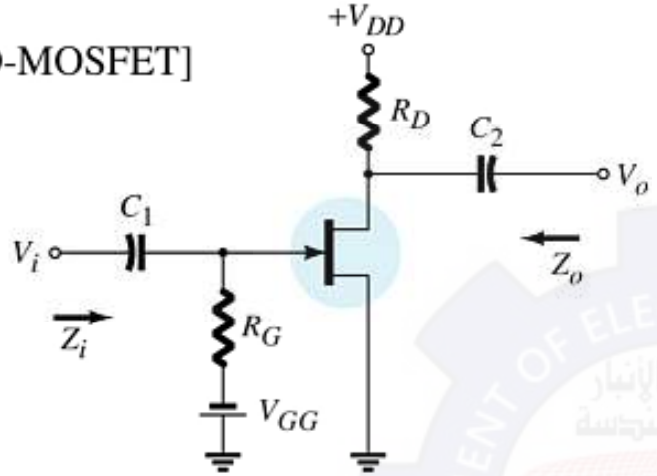
y_{os}= admittance parameter listed on FET specification sheets.

FET AC Equivalent Circuit

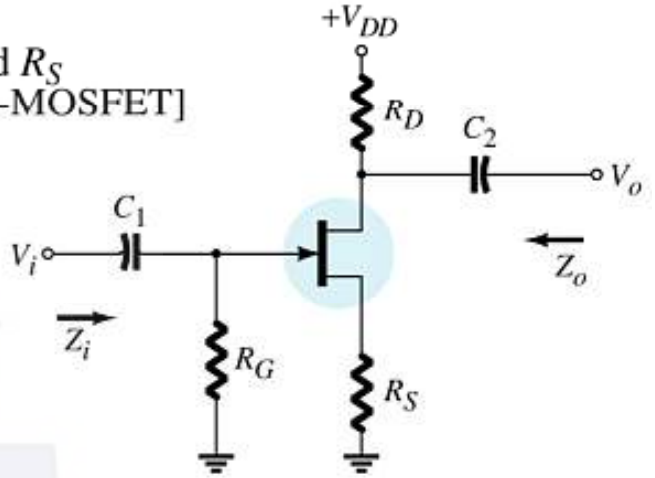


Summary Table

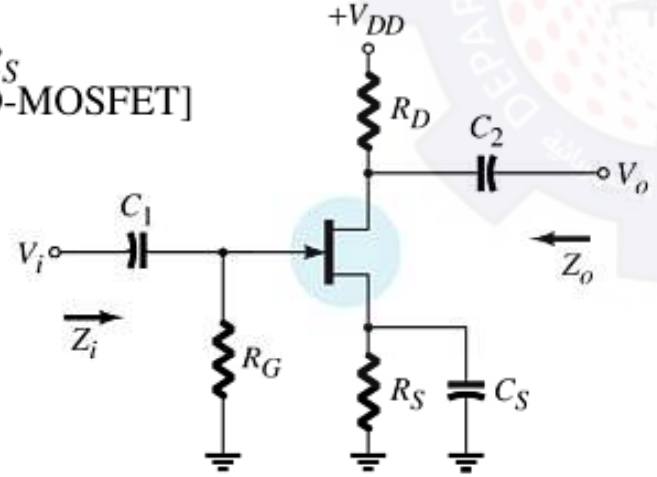
Fixed-bias
[JFET or D-MOSFET]



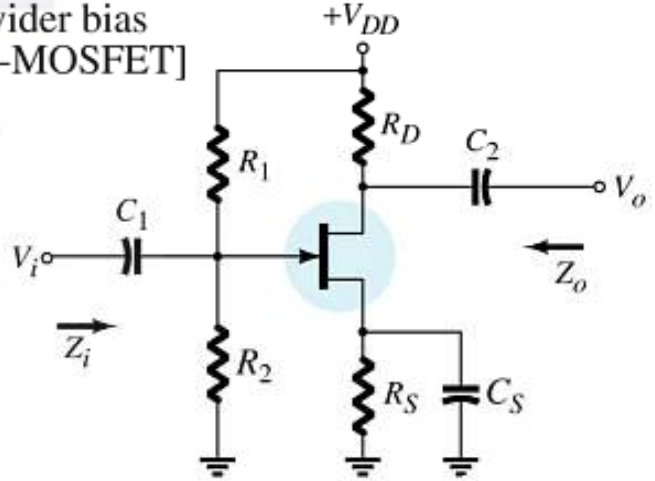
Self-bias
Unbypassed R_S
[JFET or D-MOSFET]



Self-bias
bypassed R_S
[JFET or D-MOSFET]



Voltage-divider bias
[JFET or D-MOSFET]



Troubleshooting

Check the DC bias voltages:

If not correct check power supply, resistors, FET. Also check to ensure that the coupling capacitor between amplifier stages is OK.

Check the AC voltages:

If not correct check FET, capacitors and the loading effect of the next stage

Practical Applications

Three-Channel Audio Mixer
Silent Switching
Phase Shift Networks
Motion Detection System

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Chapter08: FET Amplifier

Lec08_p2

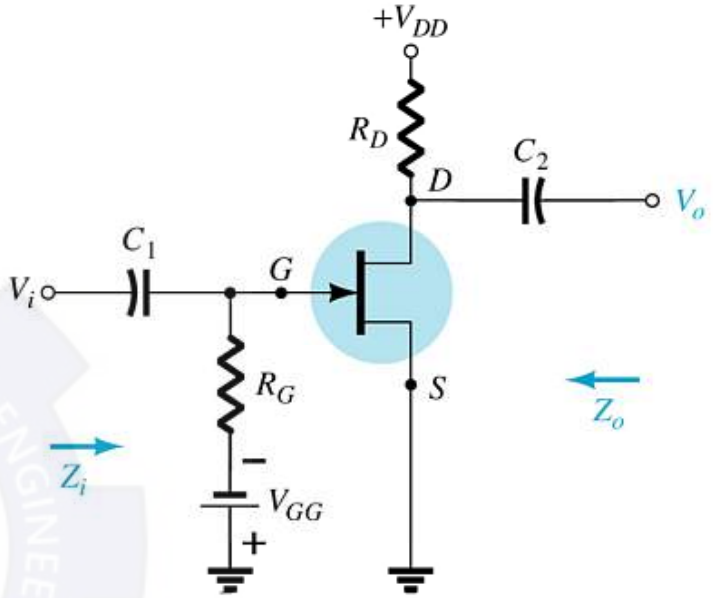
Munther N. Thiyab

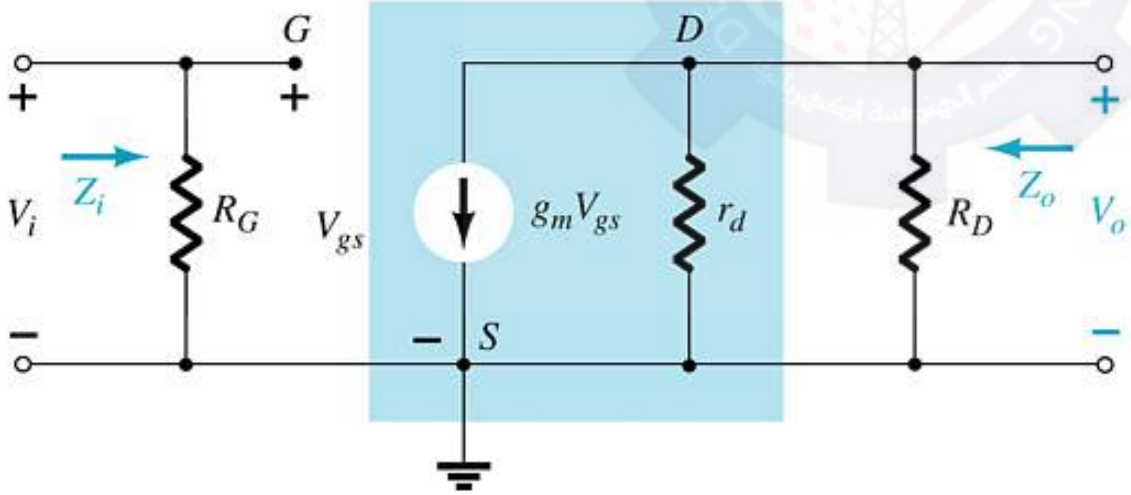
2019-2020

Common-Source (CS) Fixed-Bias Circuit

The input is on the gate and the output is on the drain

There is a 180° phase shift between input and output





Calculations

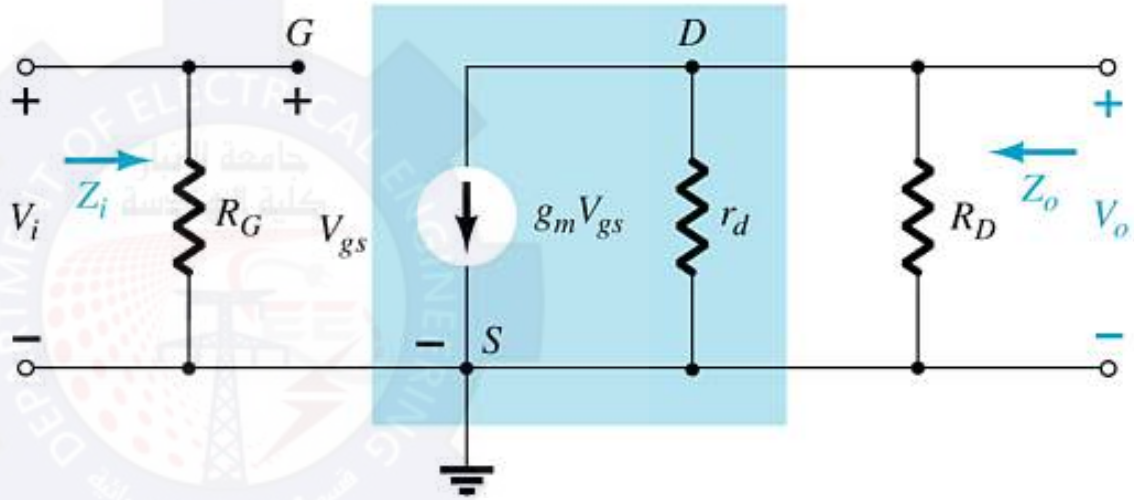
Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D \quad r_d \geq 10R_D$$



Voltage gain:

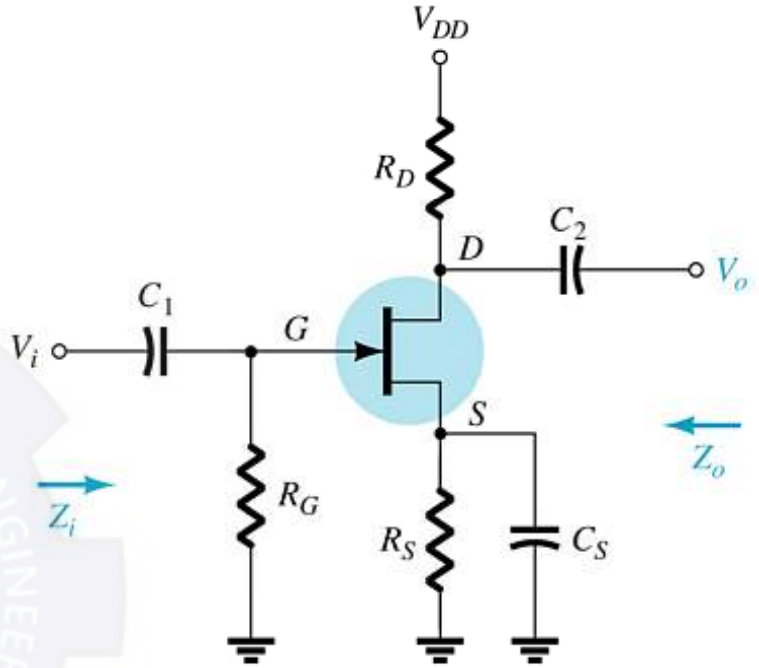
$$A_v = \frac{V_o}{V_i} = -g_m(r_d \parallel R_D)$$

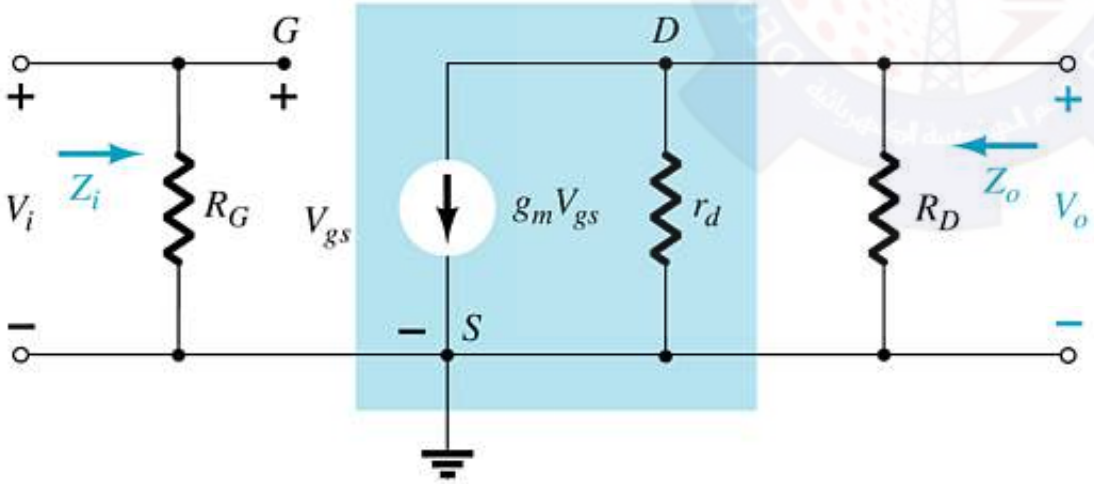
$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D$$

Common-Source (CS) Self-Bias Circuit

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain

There is a 180° phase shift between input and output





Calculations

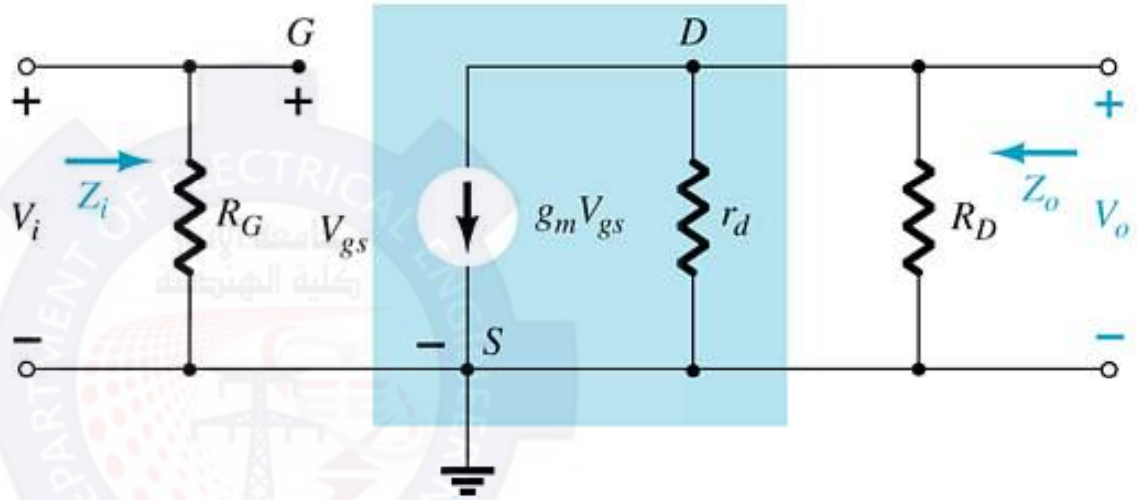
Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o = r_d \,||\, R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



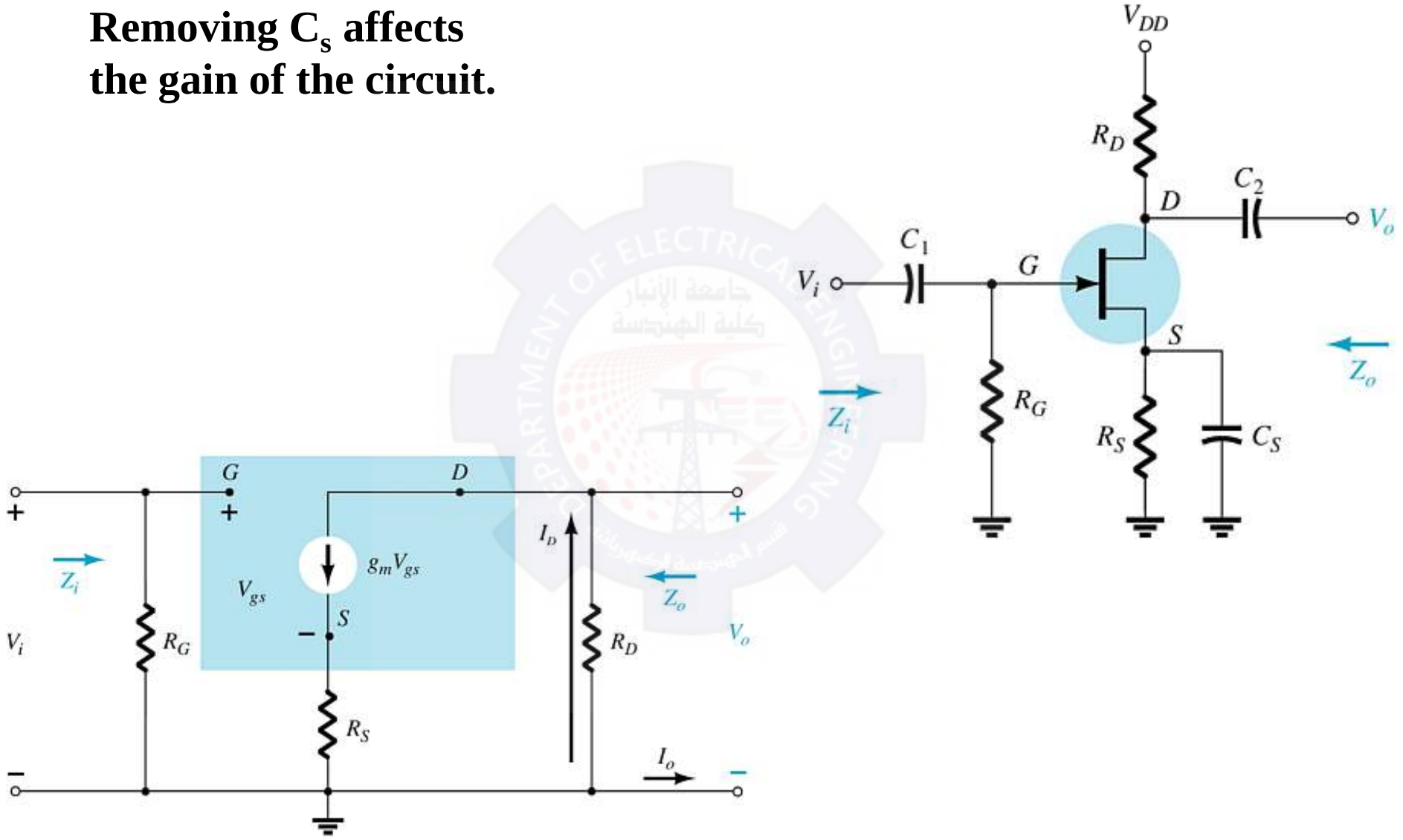
Voltage gain:

$$A_v = -g_m(r_d \,||\, R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Common-Source (CS) Self-Bias Circuit

Removing C_s affects the gain of the circuit.



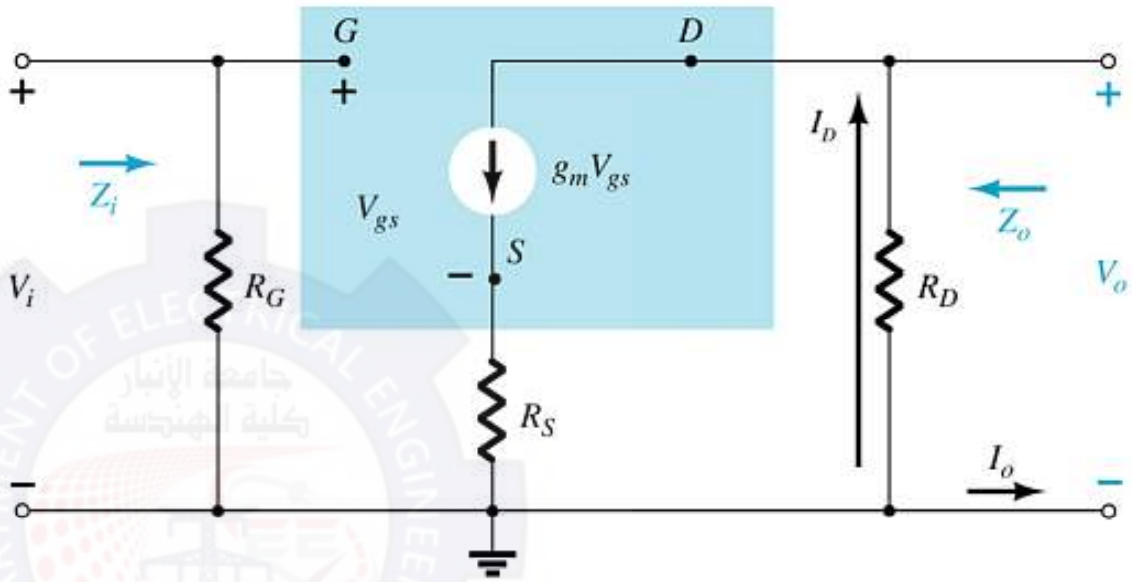
Calculations

Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



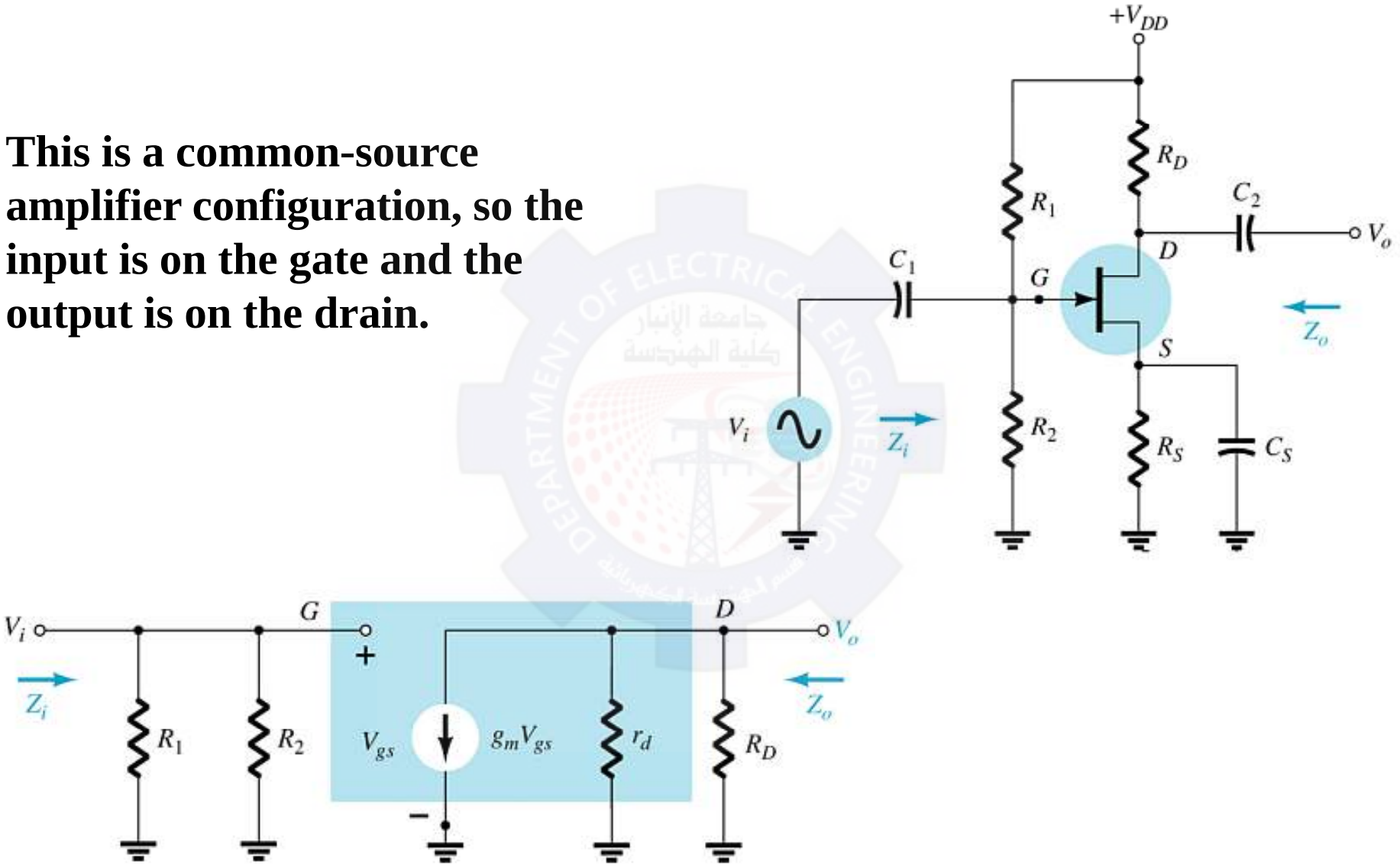
Voltage gain:

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \Big|_{r_d \geq 10(R_D + R_S)}$$

Common-Source (CS) Voltage-Divider Bias

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain.



Impedances

Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

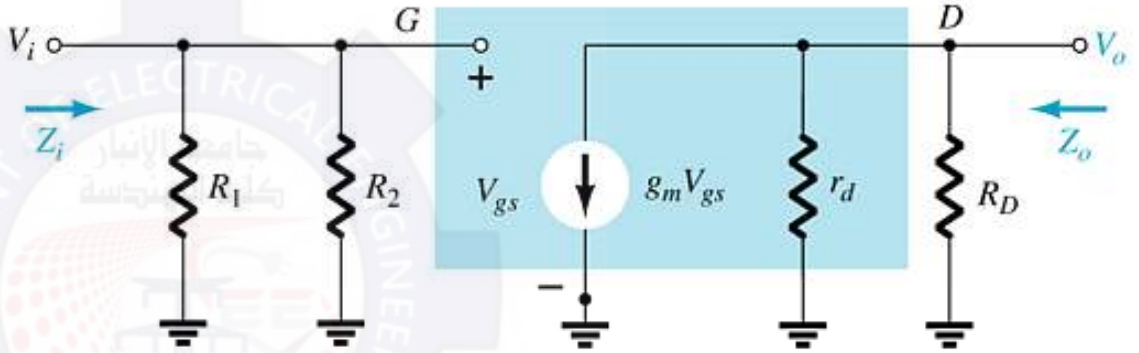
$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain:

$$A_v = -g_m(r_d \| R_D)$$

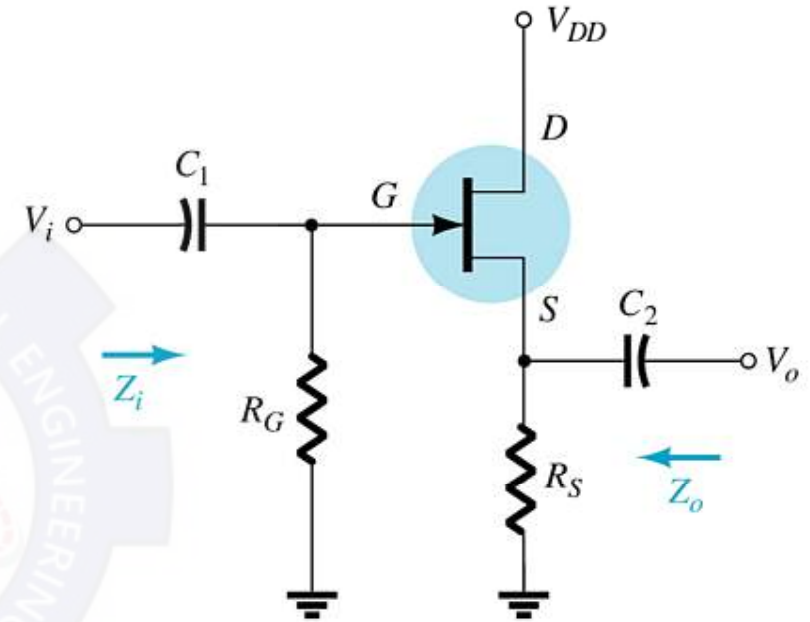
$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

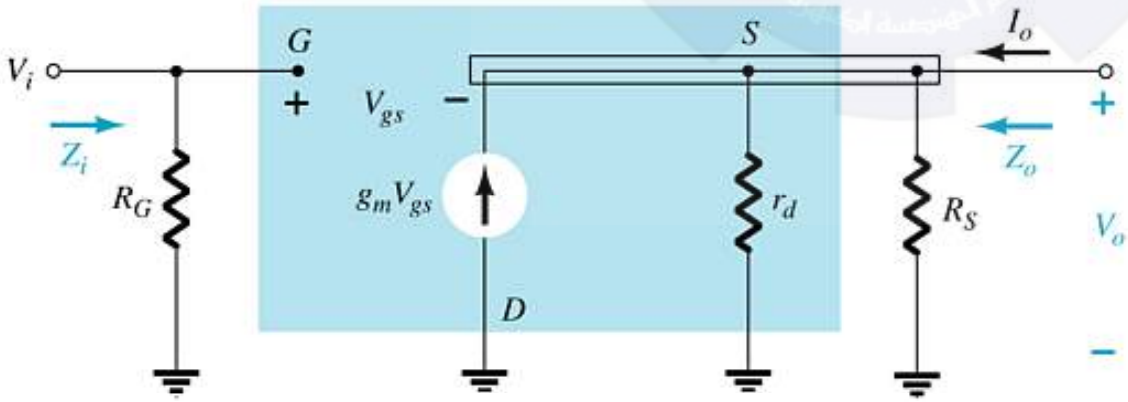


Source Follower (Common-Drain) Circuit

In a common-drain amplifier configuration, the input is on the gate, but the output is from the source.

There is no phase shift between input and output.

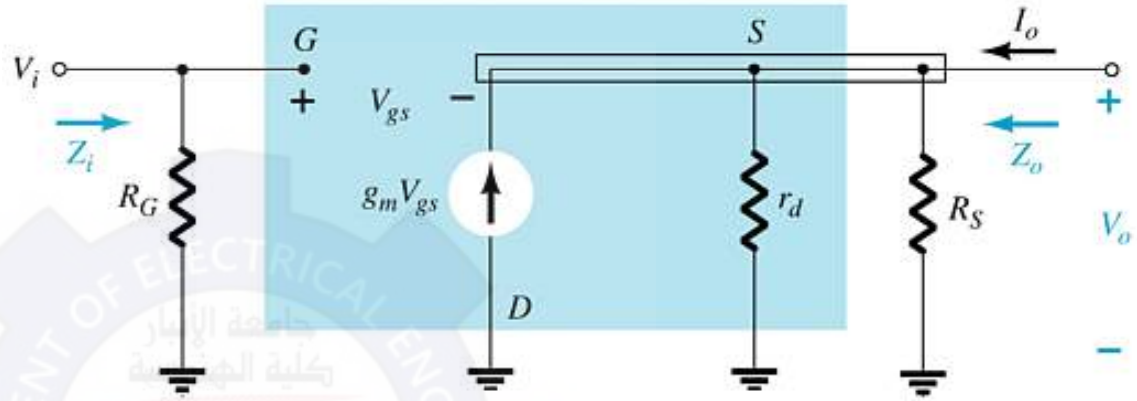




Impedances

Input impedance:

$$Z_i = R_G$$



Output impedance:

$$Z_o = r_d \,\|\, R_S \,\|\, \frac{1}{g_m}$$

$$Z_o \cong R_S \,\|\, \frac{1}{g_m} \Big|_{r_d \geq 10R_S}$$

Voltage gain:

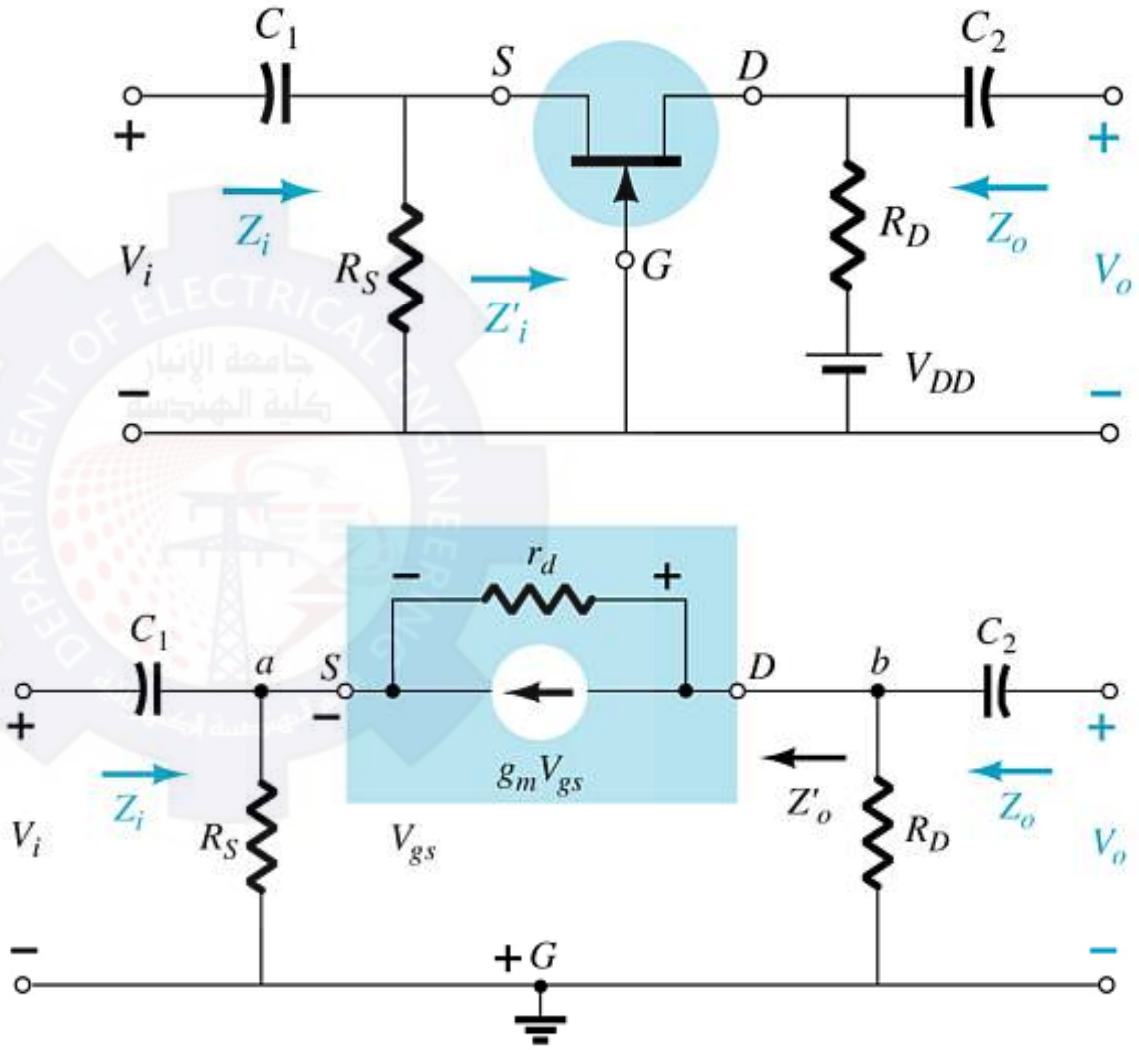
$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \,\|\, R_S)}{1 + g_m(r_d \,\|\, R_S)}$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \Big|_{r_d \geq 10}$$

Common-Gate (CG) Circuit

The input is on the source and the output is on the drain.

There is no phase shift between input and output.

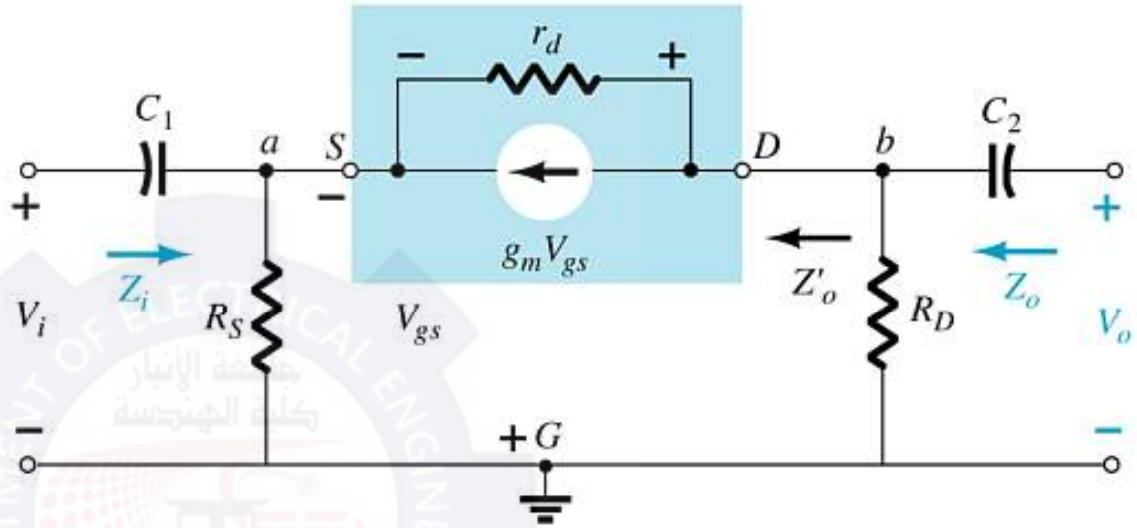


Calculations

Input impedance:

$$Z_i = R_S \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

$$Z_i \cong R_S \parallel \frac{1}{g_m}\Big|_{r_d \geq 10R_D}$$



Output impedance:

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D\Big|_{r_d \geq 10}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \qquad A_v = g_m R_D\Big|_{r_d \geq 10R_D}$$

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Chapter08: FET Amplifier

Lec08_p3

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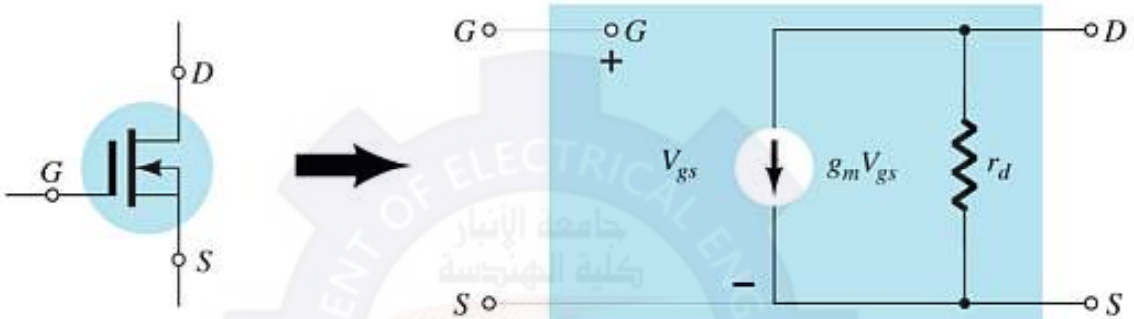
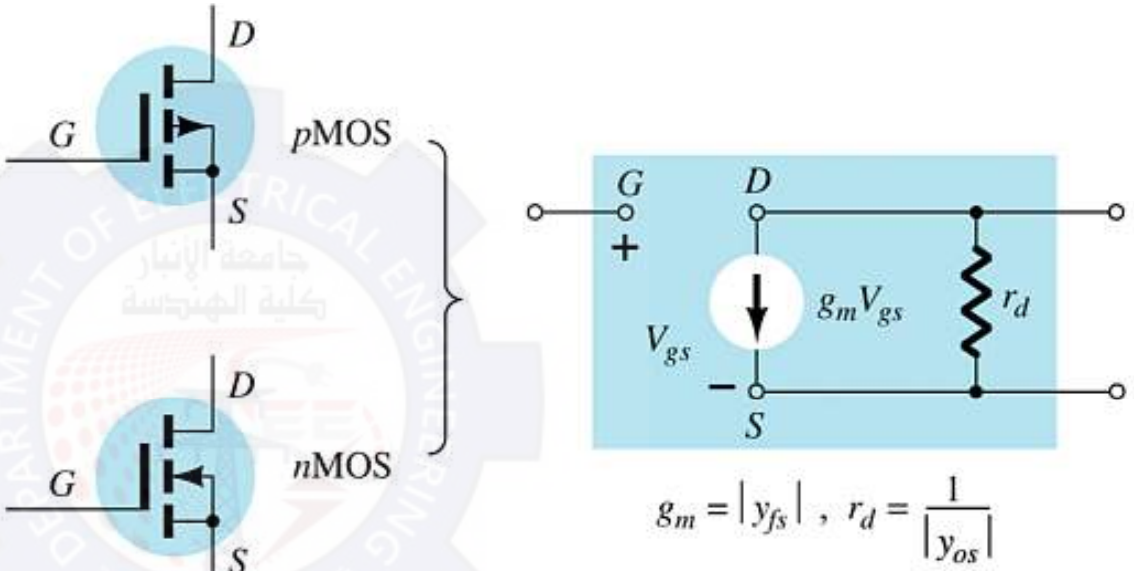
2019-2020

D-Type MOSFET AC Equivalent



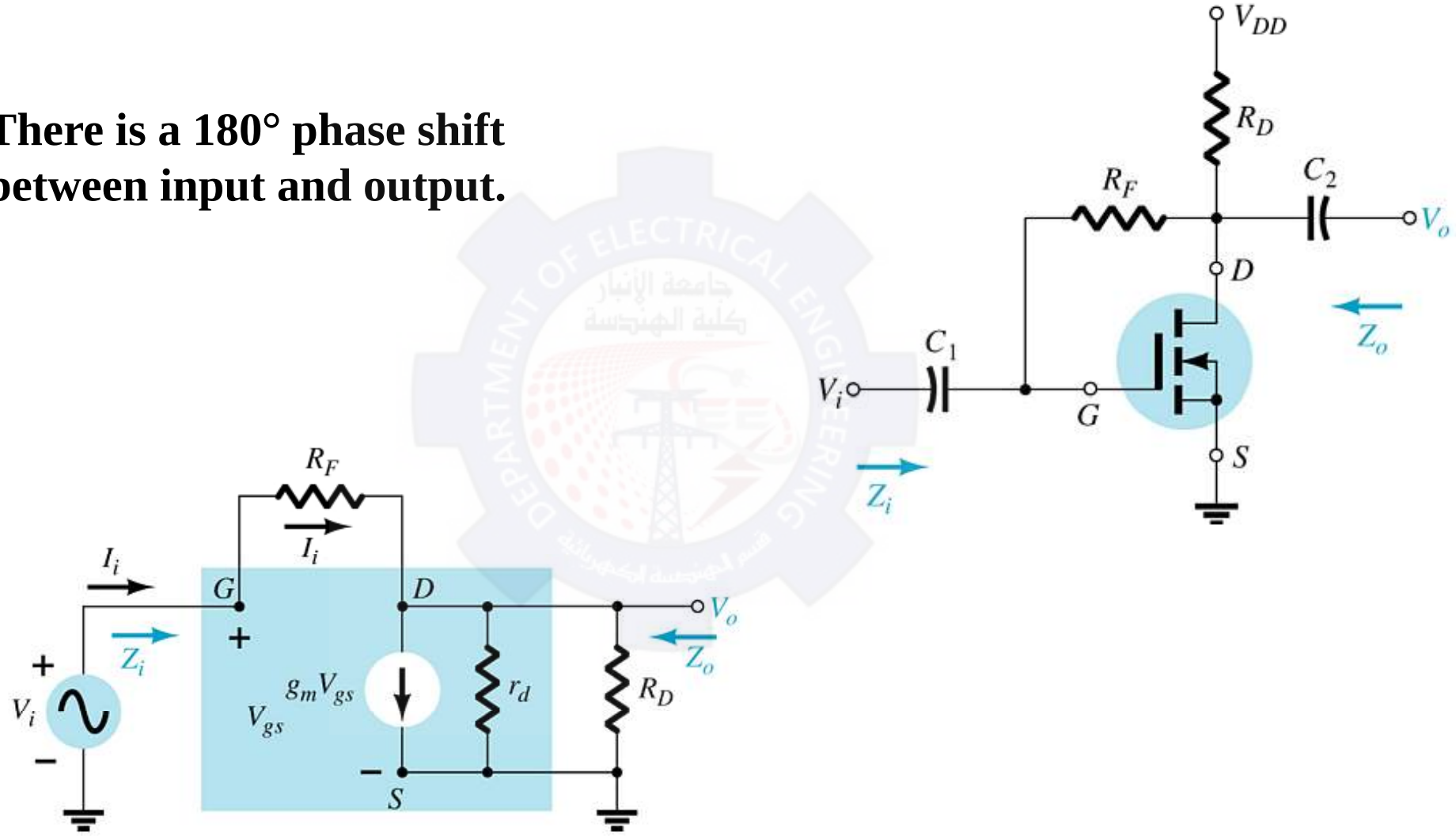
E-Type MOSFET AC Equivalent

g_m and r_d can be found in the specification sheet for the FET.



Common-Source Drain-Feedback

There is a 180° phase shift between input and output.



Calculations

Input impedance:

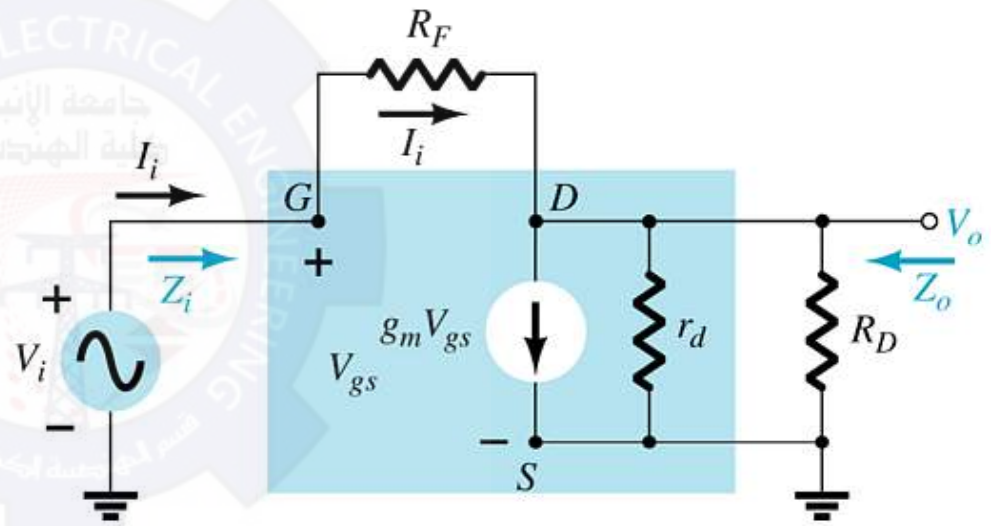
$$Z_i = \frac{R_F + r_d \,\|\, R_D}{1 + g_m (r_d \,\|\, R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \Big|_{R_F >> r_d \| R_D, r_d \geq 10 R_D}$$

Output impedance:

$$Z_o = R_F \,\|\, r_d \,\| R_D$$

$$Z_o \cong R_D \Big|_{R_F >> r_d \| R_D, r_d \geq 10 R_D}$$

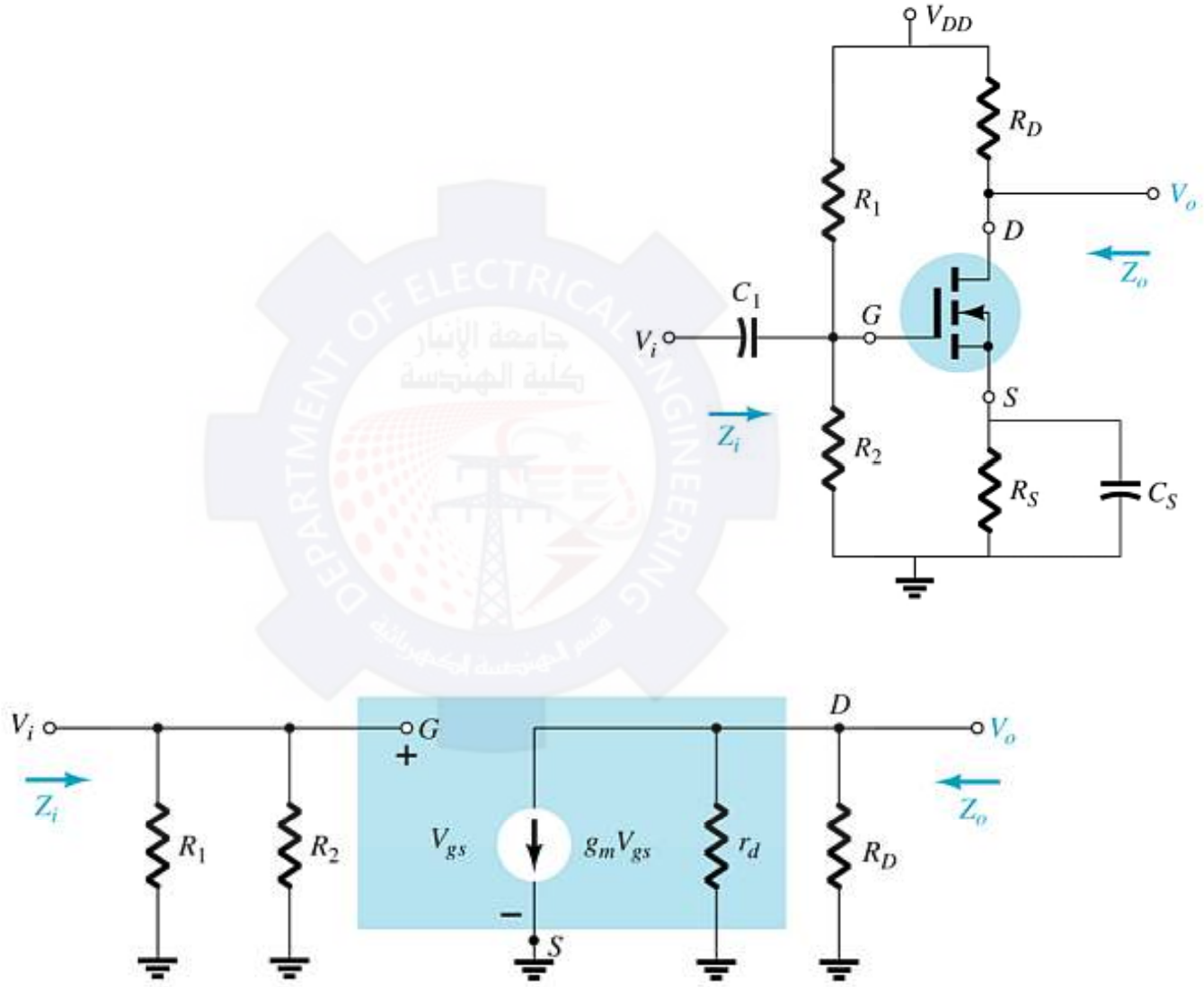


Voltage gain:

$$A_v = -g_m (R_F \,\|\, r_d \,\|\, R_D)$$

$$A_v \cong -g_m R_D \Big|_{R_F >> r_d \| R_D, r_d \geq 10 R_D}$$

Common-Source Voltage-Divider Bias



Calculations

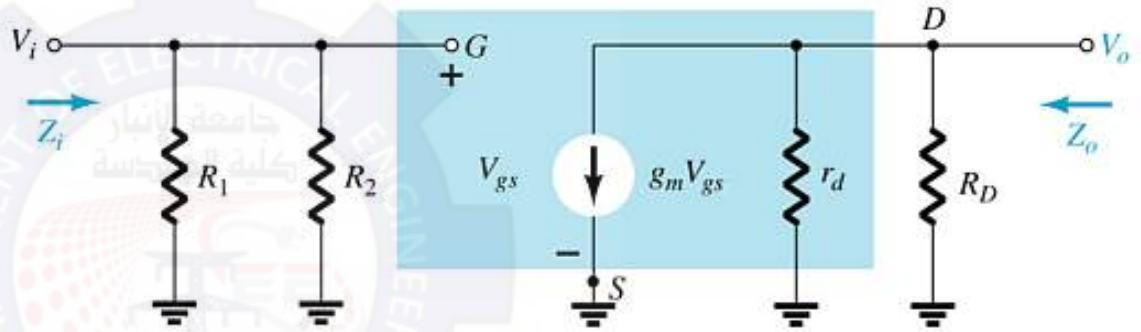
Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10}$$



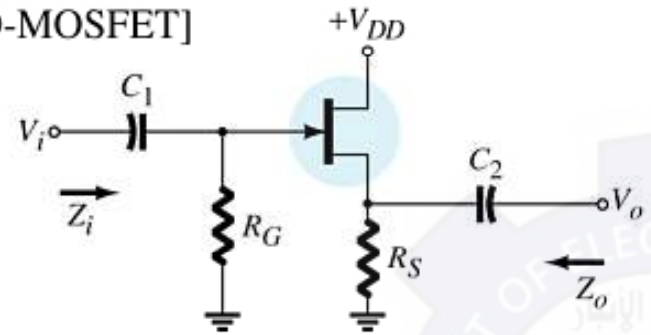
Voltage gain:

$$A_v = -g_m(r_d \| R_D)$$

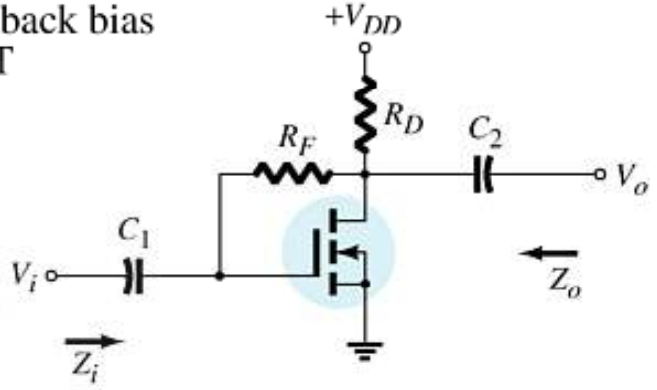
$$A_v \cong -g_m R_D \Big|_{r_d \geq 10R_D}$$

Summary Table

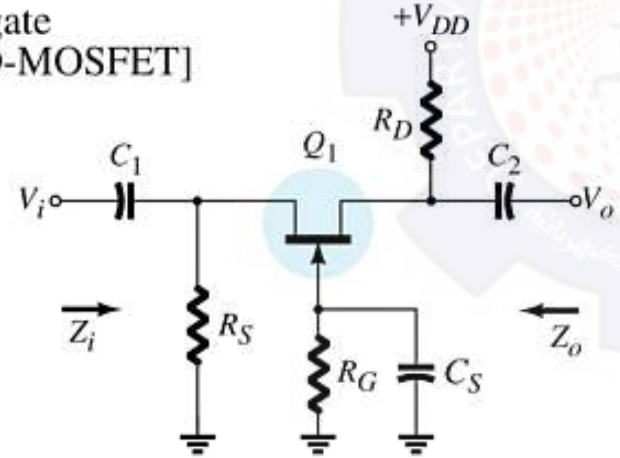
Source-follower
[JFET or D-MOSFET]



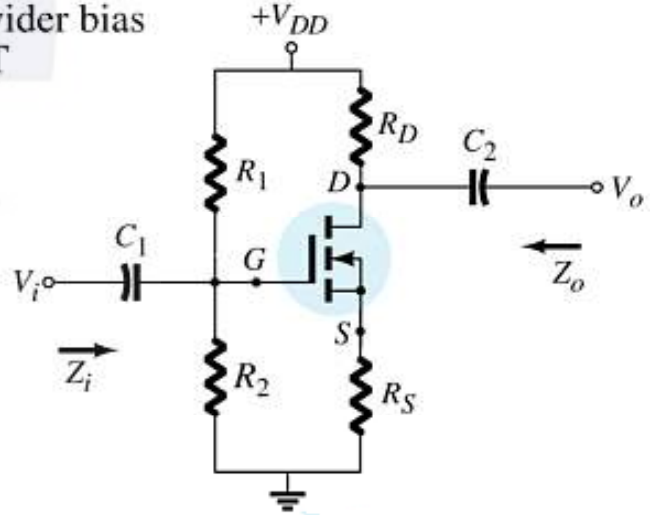
Drain-Feedback bias
E-MOSFET



Common-gate
[JFET or D-MOSFET]



Voltage-divider bias
E-MOSFET



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