Half-Subtractor and Full-Subtractor Circuit

OBJECTIVE

Understanding the theory of complements and construction of subtractor circuits.

summary

Half-subtractor and full-subtractor circuits can be built by referring to the truth tables and the Boolean expressions, or Karnaugh's map of logic gates. In this experiment we will use the theory of complement to assemble full and half subtractor circuits.

Binary subtraction are usually performed by 2's complement. Two steps are required to obtain 2's complement. First, the subtrachend is inverted to its 1's complement, i.e. an "1" to a "0" and a "0" to an "1". Secondly, an "1" is added to the least significant digit of the subtrahend in 1's complement.

In general subtraction the subtrahend is directly subtracted from the minuend but in 2's complement, the two numbers are added. Hence an adder also can be used as a subtractor.

EXAMPLE :

What is the equivalent in 2's complent for the decimal subtraction of 11 - 10?

MINUEND : 11 (DECIMAL) = 1011 (BINARY)

SUBTRAHEND : 10 (DECIMAL) = 1010 (BINARY)
= 0101 (1'S COMPLEMENT)
= 0110 (2'S COMPLEMENT)

DECIMAL	BINARY	1'S COMPLEMENT	2'S COMPLEMENT
11	1011	1011	1011
– 10	– 1010	– 1011	– 0110
1	1	0	10001

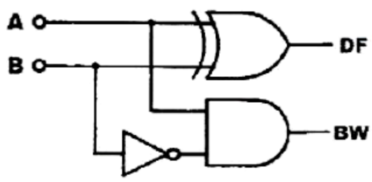
A carry of "1" is generated in the 2's complement subtraction.

A half-subtractor execute its task of subtraction 1-bit at a time regardless of whether the minuend is greater or less than the subtrahend. The true table and logic diagram of a half-sub tractor is shown in Fig. 2-48. "Borrow" from previous subtraction are not taken into consideration.

Subtrahend, Minuend, Difference, Borrow

A	B	DF	BW
0	1	0	0
0	0	1	1
1	1	1	0
1	0	0	0

(a) Truth table



(b) Schematics

Fig. 2-48 Half- subtractor

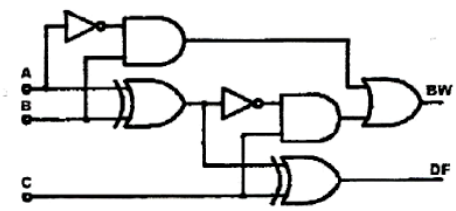
Compare the logic diagrams of half-subtractor with half-adder and we can see that the only difference is the inverter at the input of the half-subtractor. This inverter gate represent the borrow.

The full-subtractor has to consider borrow(s) from previous stages. Its truth table and logic diagram are shown in Figure 2-49. When C = "0" it is equivalent to a half-subtractor.

Previous borrow, Minuend, Subtrahend, Difference, Borrow

C	A	B	DF	BW
0	0	1	0	0
0	0	0	1	1
0	1	1	1	0
0	1	0	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

(a) Truth table



(b) Schematics

Fig. 2-49 Full-subtractor

From a 4-bit adder circuit we can assemble subtractor circuits of 4-bit or longer. Fig. 2-50 shows a dual-purpose adder/ subtractor circuit. When Bn-1="0" additions are performed and all XOR gates act as buffers. When Bn-1="1" subtractions will be performed and all XOR gates act as NOT gates. Y inputs uses 1's complement and adds an "1" from Cin. The outputs are Cn (carry) and Bn (borrow), Cn and Bn are dependent on Bn-1.

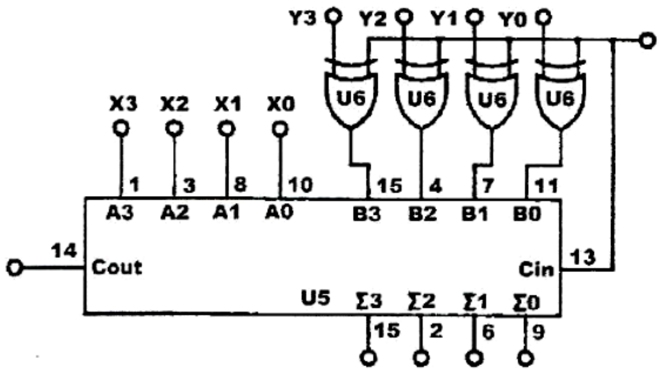


Fig. 2-50

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab, Module KL-33004

PROCEDURES

(a) Subtractor Circuit Constructed with Basic Logic Gates

1. Insert connection clips sccording to Fig. 2-51.

2. Connect inputs A~C to Data Switches SW0~SW2;outputs F2 to Logic Indicator L1; F1 to L2; F3 to L3; F5 to L4. When C=0 the circuit is a half-subtractor. F1 is the borrow output; F2 is the difference and F5=F2; F4=0; F3=F1. When C=1 the circuit is a full-subtractor. F3 is the borrow output and F5 is the difference output.

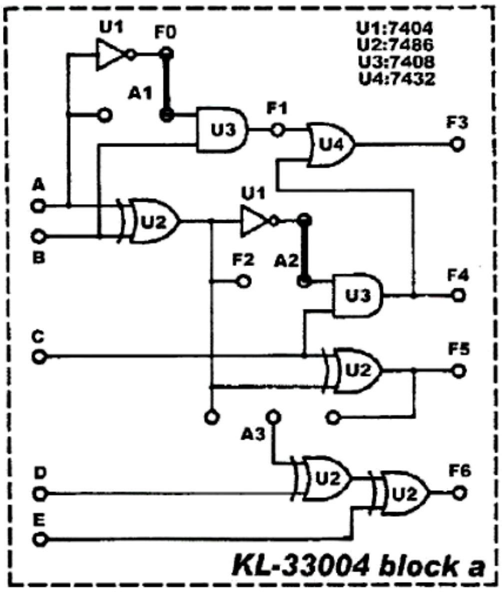


Fig. 2-51 Half-adder/Full-adder

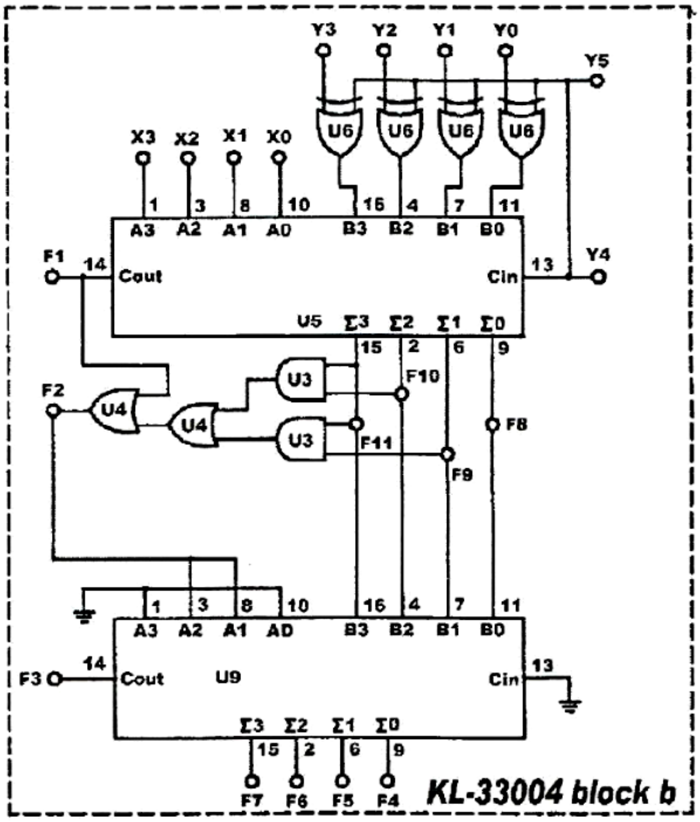
3. Follow the input sequences in Table 2-21 and record output states.

	Input			Borrow	Difference		Sum
	C	A	B	F1	F2	F3	F5
Half-subtractor Half-adder	0	0	1				
	0	0	0				
	0	1	1				
	0	1	0				
Full-subtractor Full-adder	1	0	0				
	1	0	1				
	1	1	0				
	1	1	1				

Table 2-21

(b) Full-Adder and Inverter Circuit

1. The circuit of Module KL-33004 block b (Fig. 2-52) is equivalent to the adder/ subtractor circuit of Fig. 2-53.



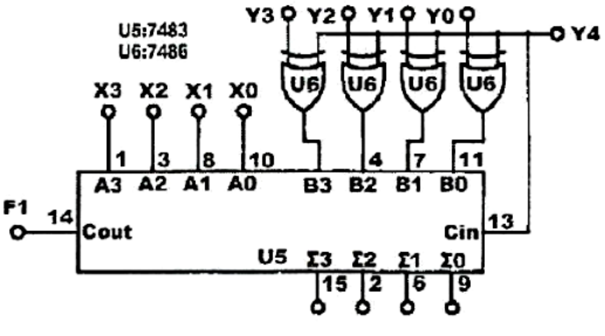


Fig. 2-53 Adder/subtractor

2. Connect inputs X3~X0 to DIP Switch 1.3~1.0; Y3~Y0 to DIP 2.3~DIP2.0; Y5 to SW0.
   Connect outputs F1 to L1; F11~F8 to L5~L2. To execute the subtract operation, connect Y5 to "1" (or Cin of U5=1). Follow the input sequences below and record the output states in Table 2-22.

INPUT								OUTPUT				
X3	X2	X1	X0	Y3	Y2	Y1	Y0	F1	F11	F10	F9	F8
0	1	0	0	0	1	0	0					
0	1	0	0	0	0	1	1					
1	0	0	0	0	0	1	1					
1	0	0	0	0	0	0	1					
1	0	0	1	1	0	0	0					
1	0	0	1	0	1	1	1					
1	0	1	0	0	1	1	0					
1	0	1	0	0	1	0	1					
1	0	1	1	1	0	1	0					
1	1	1	1	1	0	1	0					

Table 2-22

DISCUSSION:

1- Design a full-subtractor circuit?

2- Design a subtractor to subtract two numbers of 4-bit?

3- Explain in details the full subtractor circuits which are used to achieve subtraction the binary numbers by taking the previous borrow ? Then design 4-bits parallel subtractor using block-diagram?

4- Design combinational logic circuit to find the second complement for a binary number of 3-bits?