

Experiment no.: 6

Lab. Supervisor: Arrak –M-Idan

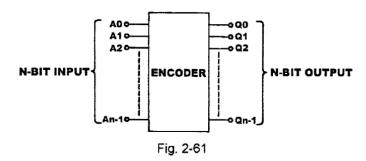
Encoder Circuit

OBJECTIVE

Understanding the operating principles of encoder circuits.

Summary

An encoder is a combinational logic gate that accept one or multiple inputs and generates a specific output code. Only one input is triggered at a time. An encoder with n-bit inputs and n-bit outputs is shown in Fig. 2-61. When one of the inputs is triggered there will be a n-bit output code at the outputs.



Octal to Binary Encoder

An octal to binary encoder is shown in Fig. 2-62. There are 8 octal inputs A1 \sim A7 (0 \sim 7); and three binary outputs Q0, Q1, Q2 (000 \sim 111). If input A0="0" the corresponding output Q2Q1Q0 is equal to "000".

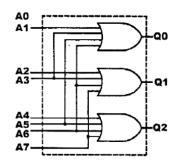


Fig. 2-62 Octal -Binary encoder



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Actually, A0 is not connected to the gate input. If A1="1" then Q2Q1Q0=001. When A2="1" the output Q2Q1Q0=010. There can't be more than one "1" among the inputs. For example, if A2="1" and A3="1" simultaneously, Q2Q1Q0=011. If A3, A4 both are "1" at the same time, Q2Q1Q0=111. Both outputs are incorrect.

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Modules KL-33005, KL-33006

PROCEDURES

- (a) Constructing a 4-to-2 Encoder with Basic Gates
 - 1. Insert connection clips according to Fig. 2-64.

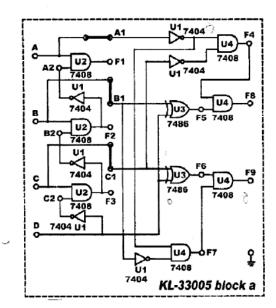


Fig. 2-64



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- 2. Connect Vcc to +5V.
- 3. Connect inputs A~D to Data Switches SW0~SW3 respectively; outputs F8 and F9 to Logic Indicator L0 and L1.
- 4. Follow the input sequences for D, C, B, A in Table 2-28 and record the output states.

D	С	В	Α	F8	F9			
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
DO000000111111111	00000111100001111	0011001100110011	010101010101					
Table 2-28								

5. Remove the connection clip between A and A1; insert it between A1 and F1 as shown in Fig. 2-65. All other connections remain the same. Follow the input sequences in Table 2-29 and record output states.

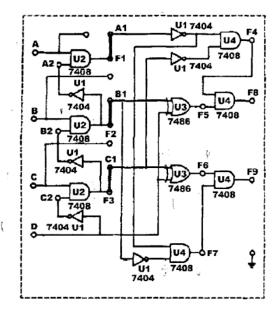


Fig. 2-65



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D	C	R	Α	F8	F9
D 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	C 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1	B 0 0 1 1 0 0 1 1 0 0 1 1	A 0 1 0 1 0 1 0 1 0 1 0 1 0 1	F8	<u>F9</u>
1 1 1 1 1 1 1	00001111	00110011	01010101		

Table 2-29

- 6. Compare the outputs staes in Table 2-28 and 2-29. What is the difference between them?
- (b) Constructing a 9-to-4 Encoder with TTL IC
 - The 74147 (U7) on block a of module KL-33006 is used in this section of the experiment. Connect Vcc to +5V.

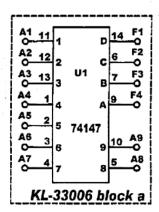


Fig. 2-66

 Connect inputs A0~A8 to DIP Switches 1.0~1.7, A9 to 2.0. Connect outputs F1~F4 to Logic indicators L1~L4. Follow the input sequences given in Table 2-30 and record output states. University of Anbar College of Engineering Dept. of Electrical Engineering



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Α9	A8	A7	Α6	Α5	A4	А3	A2	Α1	F4	F3	F2	<u>F1</u>
0	1	1	1	1	1	1	1	1				
0	0	1	1	1	1	1	1	1				
1	1	1	1	1	1	1	1	0				
1	1	1	1	1	1	1	0	0				
1	1	1	1	1	1	0	1	1				
1	1	1	1	1	0	0	0	0				
1	1	1	1	0	1	1	1	1				
1	1	1	1	0	0	0	1	1				
1	1	1	0	1	1	1	0	0				
1	1	0	1	1	0	1	1	0				
1	1	0	0	0	1	1	1	1				
1	0	0	0	0	0	1	1	1				

Table 2-30

DISCUSSION:

- 1- Design an encoder for coding 4 inputs and 2 outputs (Encoder 4× 2)?
- 2- Design with drawing an octal-to-binary Encoder?
- 3- Design the decimal to BCD Encoder?