Flip-Flops

OBJECTIVE

Study the differences between combinational and sequential logic circuits; and the applications of various memory units.

Summary

Two NOT, or INVERTER gate ICs are shown in Fig. 4-1, output of IC2 is connected to IC1's input. Assuming IC1's output is "1", IC2's output will be "0". Because IC2's output is connected to IC1's input, IC1's input will be inverted to "1" again. If an external pulse is connected to IC1's input, output of IC1 will be "0" while IC2's output is "1" (output of IC1 goes back to "0").

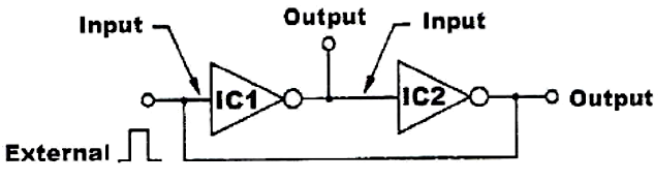


Fig. 4-1

If the external pulse is designated as A, and IC2's output as B, when either A or B is "1", output of IC1 is "0".

If the NOT gates of Fig. 4-1 are replaced by two NOR gates and the two inputs are designated as R and S, a R-S flip-flop Fig. 4-2 is created. See Fig. 4-2.

R = Reset, output Q is reset to binary 0
S = Set, output Q is set to binary 1

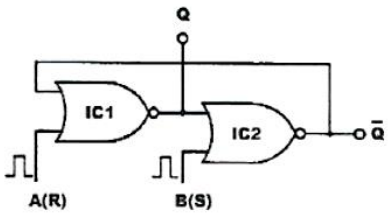


Fig. 4-2

Output of IC1 is called Q (normal output) while IC2's output is called Q (complement output). A flip-flop will change its logic state when an appropriate logic input is applied. It will remain in the stable state as long as power is supplied or until the input changes.

In most cases, flip-flops are constructed with NOR or NAND gates. Fig. 4-3 shows a positive logic NOR R-S flip-flop. Fig. 4-3 is a negative logic NAND R-S flip-flop.

The R-S flip-flop is the simplest form of flip-flop and can be used to construct other flip-flops, hence a R- S flip-flop is also called "basic flip-flop". Table 4-1 is the truth table of a R-S flip-flop. Qn is the current output state while Qn+1 is the next output state.

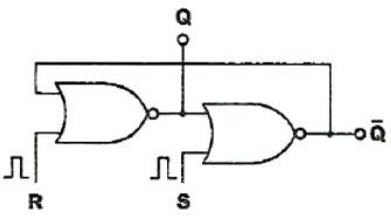


Fig. 4-3

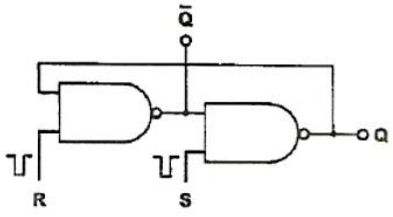


Fig. 4-4

R	S	Qn+1
0	0	Qn
0	1	1
1	0	0
1	1	?

Table 4-1 R-S flip-flop truth table

The following characteristics of R-S flip-flop can be observed from the truth table :

(1) when R=0 and S=0, Qn+1=Qn so Qn+1 is equal to the previous Qn, which could be either "0" or "1".

(2) when R=0 and S=1, the flip-flop is set to binary "1" so Qn+1="1".

(3) when R=1 and S=0, the flip-flop is reset to binary "0" so Qn+1="0".

(4) when R=1 and S=1, Qn+1 could be either "0" or "1" simultaneously. Since the output can't possibly exist in two states at the same time, Qn+1 is "undefined" or in "limbo" state when R=S=1.

Fig. 4-5 shows the complete symbol of a R-S flip-flop. CK is the clock signal, the flip-flop will change state after the presence of CK is detected.

PR = Preset; regardless of CK, PR will set output Q to "1"

CL = Clear; regardless of CK, CL will set output Q to "0".

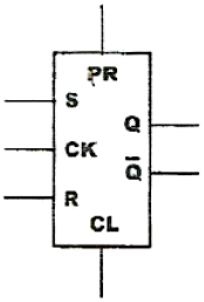


Fig. 4-5 R-S flip-flop

A D flip-flop can be constructed using a R-S flip-flop. Refer to the symbol of D flip-flop and the schematics of D flip-flop constructed with R-S flip-flop in Fig. 4-6 (a) and (b) respectively.

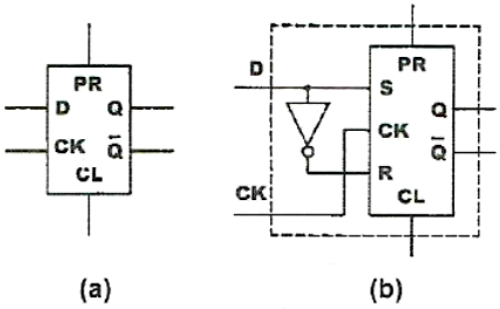


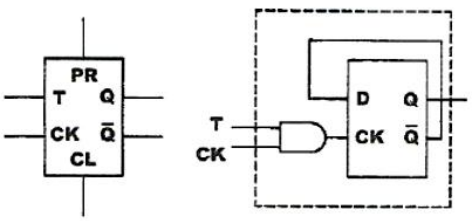
Fig. 4-6 D flip-flop

D flip-flop are used mostly for data transmission. Table 4-2 is its truth table.

CK	D	Qn+1
0	0	Qn
0	1	Qn
1	0	0
1	1	1

Table 4-2 D flip-flop truth table

A T flip-flop can be constructed using a D flip-flop. Refer to the symbol of D flip-flop, and the schematic of a T flip-flop constructed with D flip-flop in Fig. 4-7 (a) and (b) respectively. Table 4-3 is the truth table for T flip-flop.



(a) (b)

Fig. 4-7 T flip-flop

CK	T	Qn+1
0	0	Qn
0	1	Qn
1	0	Qn
1	1	$\overline{Qn}$

Table 4-3

From Table 4-3, we can see that T flip-flop change its output state only when T=1 and CK=1. Assuming Qn="0" initially, at T=1 and CK=1, output of the T flip-flop will become binary "1". Output of the flip-flop will remain binary "1" until T=1, CK=1 again, At that point the output will return to binary "0".

Output of T flip-flop output alternates between binary "0" and "1" when T=1, CK=1. This unique characteristic of the T flip-flop means that "divide-by-2" circuits can be constructed with T flip-flop. Refer to the waveforms in Fig. 4-8, there are two input waveforms but only one output waveform. T flip-flops are usually used in the delay circuits of counters.

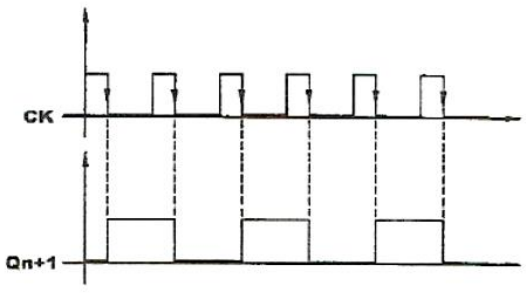


Fig. 4-8

The J-K flip-flop can eliminate the "undefined" state of R-S flip-flop. Symbol of a J-K flip-flop is shown in Fig. 4-9.

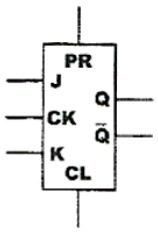


Fig. 4-9

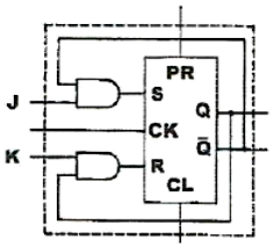


Fig. 4-10

Fig. 4-10 shows an equivalent J-K flip-flop constructed with R-S flip-flop. Refer to the truth table (Table 4-4). The J-K flip-flop is the same as the R-S flip-flop except at J=1, K=1 and CK=1 when the J-K flip-flop is similar to a T flip-flop.

CK	J	K	Qn+1
0	0	0	Qn
0	0	1	Qn
0	1	0	Qn
0	1	1	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	$\overline{Qn}$

Table 4-4 J-K flip-flop truth table

Since the J-K flip-flop has no undefined state and can be used to construct just about any flip-flop, it is also referred to as an "universal flip-flop".

Fig. 4-11 is the circuit of a master-slave J-K flip-flop.

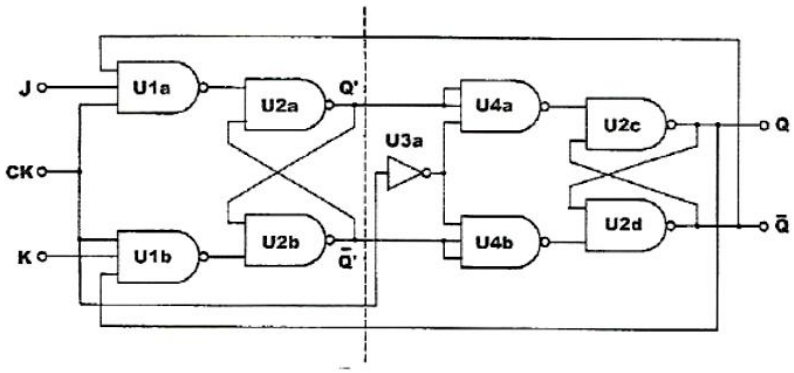


Fig. 4-11 Master-Slave J-K flip-flop

At CK=0, the master flip-flop can't accept new inputs so its outputs Q and $\overline{Q}$' remains the same, Q and $\overline{Q}$' are transmitted to the slave flip-flop's outputs Q and $\overline{Q}$'.

At CK=1, the master flip-flop can accept new inputs, but Q and $\overline{Q}$ of the slave flop-flop does not change.

Fig. 4-12 is the timing diagram of the master-slave flip-flop. When CK=1, the input changes continuously until at the negative edge of CK the last input value is latched. At CK=0, the output of master flip-flop is send to the slave flip-flop so it is a negative edge triggered CK.

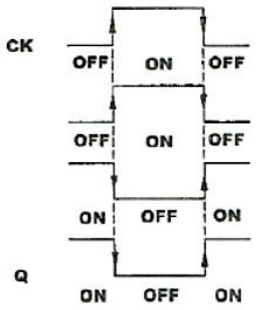


Fig. 4-12

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Module KL-33008

PROCEDURES

4-1 Constructing a R-S Flip-Flop with Basic Logic Gates

1. Connect inputs A3, A4 to Pulser Switches SWA $\overline{A}$ (TTL), SWB $\overline{B}$ (TTL) output. Connect outputs F6 and F7 to Logic Indicators L1, L2. What is the states of F6 and F7? Turn the power off for a few seconds and turn it back on. What is the states of F6 and F7 now?

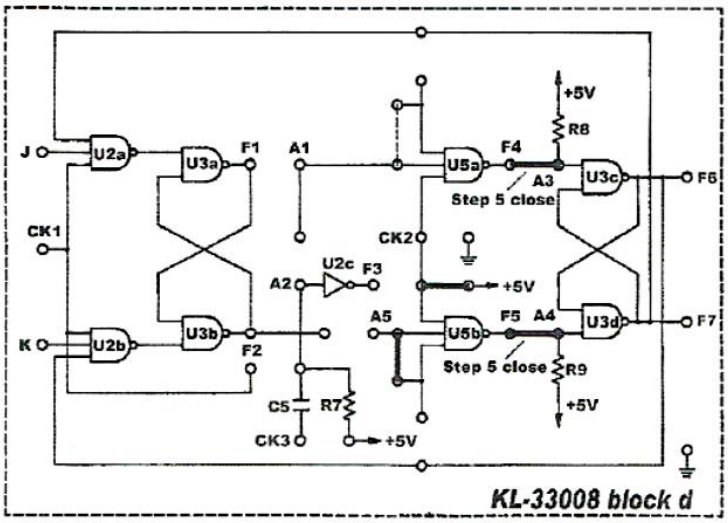


Fig. 4-13

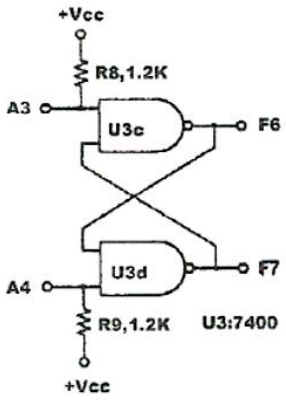


Fig. 4-14

2. Follow the input sequences in Table 4-5. Observe and record F6, F7.

STATES	A4	A3	F6	F7
0	0	0		
1	0	⊔		
2	⊔	0		
3	⊔	⊔		

Table 4-5

3. Determine the Q and $\overline{Q}$ output, the R and S input. (set Pulser Switch to "1" first, then "0" and "1" again)

4. Insert connection clips according to Fig. 4-13 to construct the circuit of Fig. 4-15. Connect inputs A1, A2 to Pulser Switches SWA A, SWB B output.

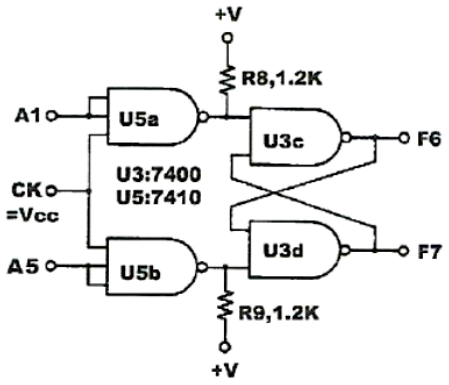


Fig. 4-15

Follow the input sequences in Table 4-6. Observe and record F6, F7.

STATES	A5	A1	F6	F7
0	0	0		
1	0	⊓		
2	⊓	0		
3	⊓	⊓		

Table 4-6

4-2 Constructing a D Flip-Flop with R-S Flip-Flop

1. Insert connection clips according to Fig. 4-16 to construct the D flip-flop circuit of Fig. 4-17.

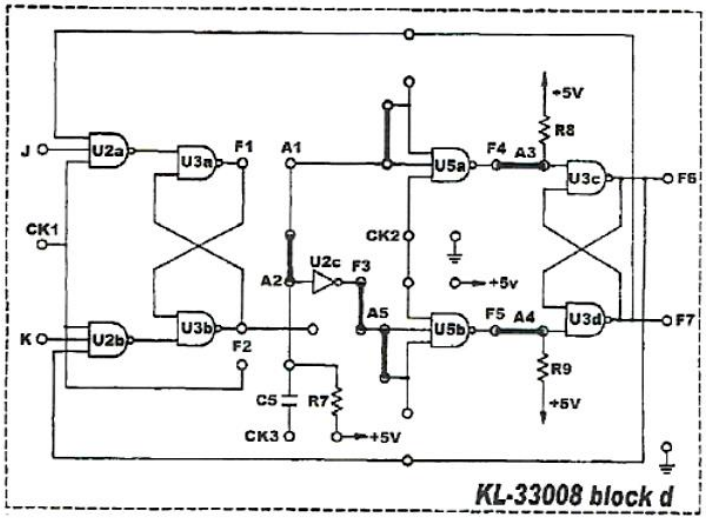


Fig. 4-16

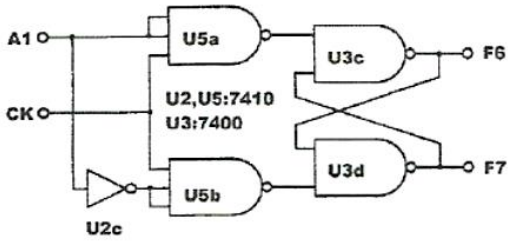


Fig. 4-17

2. Connect A1 to SW1; CK2 to SWA A output and F6 to L1.

3. Follow the input sequences in Table 4-7. Observe and record the output states.

CK	A1	F6
0	0	
0	1	
⎍	0	
⎍	1	

Table 4-7

4-3 Constructing a J-K Flip-Flop with D Flip-Flop

1. Insert connection clips according to Fig. 4-18 to construct the T flip-flop circuit of Fig. 4-19. Connect CK2 to SWB B output; A1 to SW0; A5 to SW1; F6 to L1.

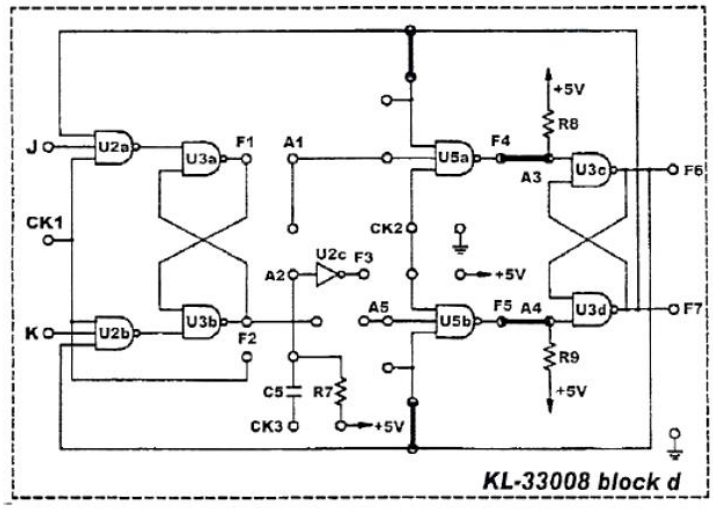


Fig. 4-18

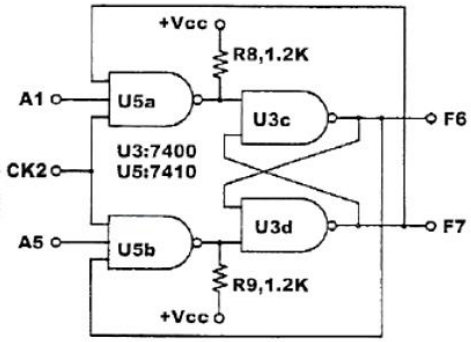


Fig. 4-19

2. Follow the input sequences in Table 4-8. Observe and record output states.

INPUT			OUT
CK2	A5	A1	F6
⎍	0	0	
⎍	0	1	
⎍	1	0	
⎍	1	1	

Table 4-8

4-4 Constructing a J-K Flip-Flop with R-S Flip-Flop

1. Insert connection clips according to Fig. 4-20 to construct the J-K flip-flop circuit of Fig. 4-21. Connect CK1 to SWA A output; J to SW0; K to SW1; F1, F2, F6, F7 to L0, L1, L2, L3 respectively.

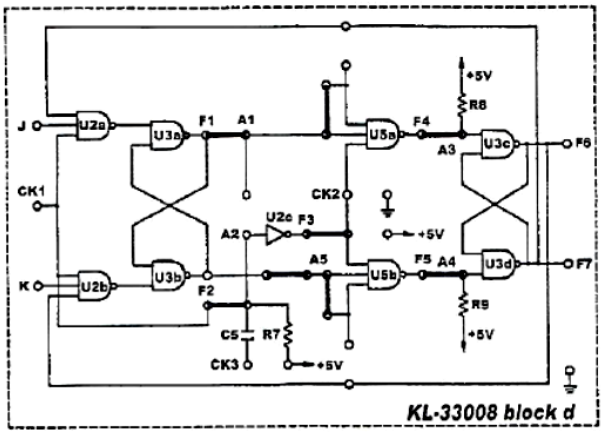


Fig. 4-20

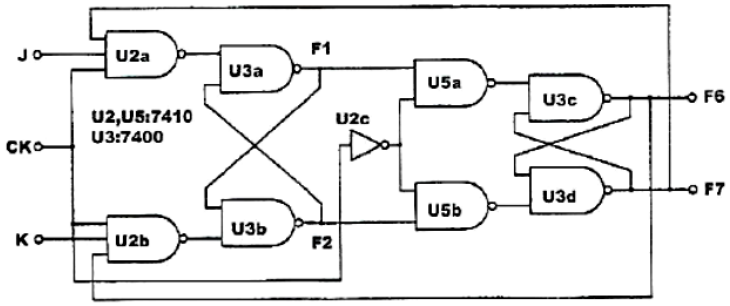


Fig. 4-21

3. Follow the input sequences in Table 4-9. Observe and record the output states.

INPUT			OUT			
CK	K	J	F1	F2	F6	F7
0	0	0				
1	0	0				
0	0	0				
0	0	1				
1	0	1				
0	0	1				
0	1	0				
1	1	0				
0	1	0				
0	1	1				
1	1	1				
0	1	1				

Table 4-9

DISCUSSION:

1- There are four types of flip-flops, what are these types, then draw each one of them?

2- Describe briefly, with truth table and drawing the Asynchronous SR-latch?

3- Describe briefly, with truth table and drawing the synchronous J-K Flip-Flop ?

4- Show Q-output waveform for positive edge triggered of SR-FF(using NAND gates) in relation to input waveform, where S=1001001 , R=0100100 , start with Q=0 ?

5- Show Q-output waveform for positive edge triggered of D-F,F (using NAND gates) in relation to input waveforms, where D=1001001, start with Q=0 ?

6- Convert from SR to J-K Flip-Flop?