J-K Flip-Flop Circuits

OBJECTIVE

Study the principles of counters and how to construct counters with J-K flip-flops.

Counters are constructed with flip-flops and basic logic gates. From the previous experiment, we found that the T flip-flop alternates its output state between binary "0" and "1" when its inputs T=1 and CK=1.

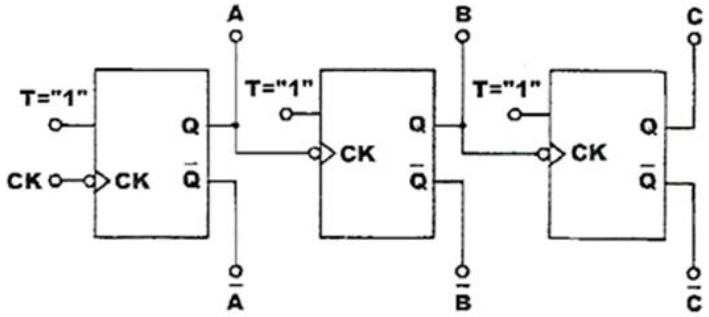


Fig. 4-26

Refer to Fig. 4-26 where three T flip-flops are connected in series. The Q outputs of the flip-flop in front are used as the CK input for each succeeding flip-flop. Assuming the number of flip-flops connected in series is "n" and there are "n" inputs, the output of the last flip-flop will be $n/2^n$. The output waveforms are shown in Fig. 4-27.

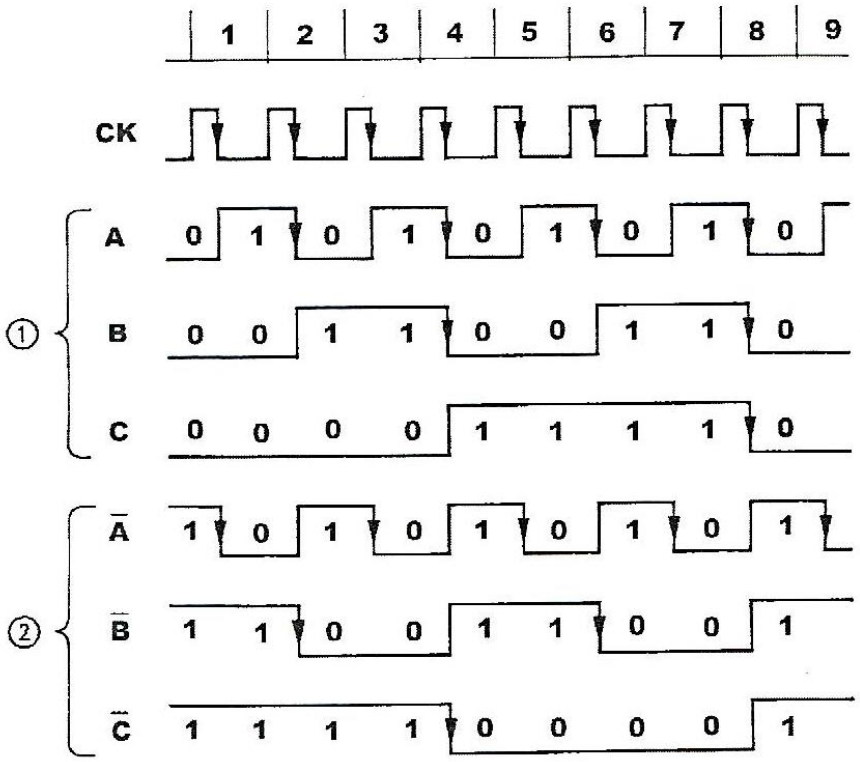


Fig. 4-27

We can see from Fig. 4-27 that the normal outputs A, B, C are counting "up" while the complement outputs $\bar{A}$, $\bar{B}$, and $\bar{C}$ are counting "down" so CK is triggered at the negative edge.

A has twice the cycle and half the frequency of CK.
B has twice the cycle and half the frequency of A.
C has twice the cycle and half the frequency of B.

If CK is triggered at the positive edge, the output waveforms are as shown in Fig. 4-28. Clearly A, B and C are counting up. The circuit of Fig. 4-26 will count "up" when CK is connected to Q. When CK is connected to $\bar{Q}$, the circuit will count "down".

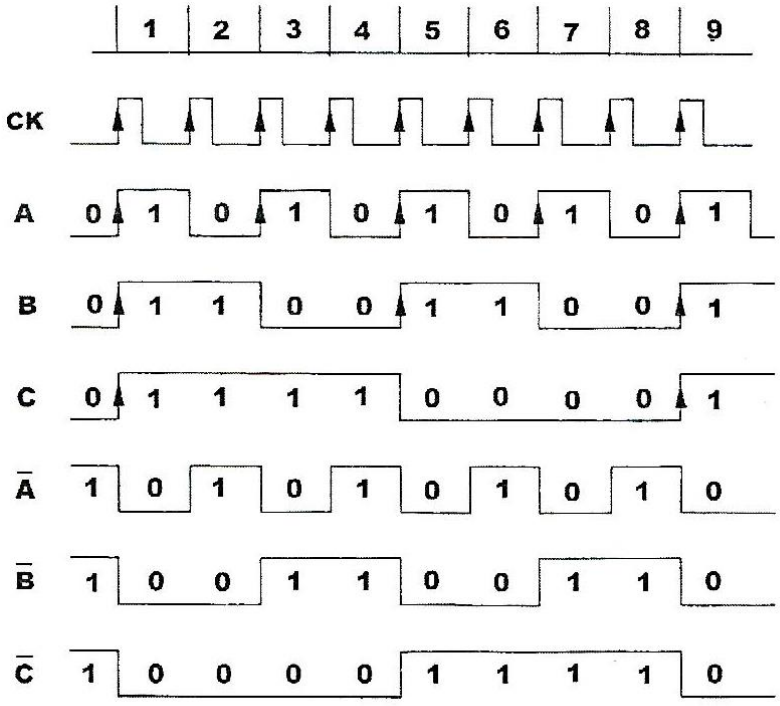


Fig. 4-28

The J-K flip-flop is an universal flip-flop that will be used in this experiment to construct basic counters. The circuit of Fig. 4-29 is an up/down counter constructed with J-K flip-flops connected in series.

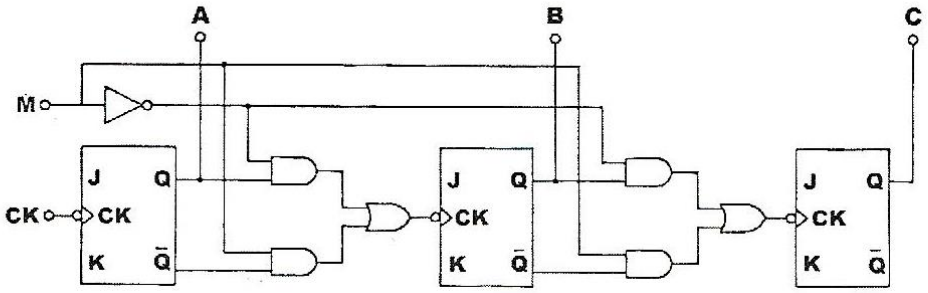


Fig. 4-29

When M=0, CK connects to Q and the circuit will count "UP".
When M=1, CK connects to $\bar{Q}$ and the circuit will count "DOWN".

Serial connections, such as Fig. 4-29, are referred to as "Asynchronous Counting". In order to have the "Divide-by-n" effect, the output must be connected to the "CLEAR" pin.

Fig. 4-30(a) shows a divide-by-5 circuit. We can see from its truth table (Fig. 4-30(b) that the "0" and "5" states are equal, forming a loop called divide-by-5 circuit.

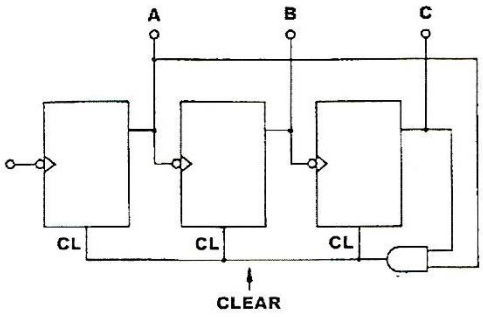


Fig. 4-30 (a)

STATE	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0
6	0	0	1

Fig.4-30 (b)

In Fig. 4-30(a), A and C are connected to "CL" through the AND gate. Since the "5" state is 101, when CBA=101 the counter is resetted.

Another method of achieving the asynchronous divide-by-N operation is shown in Fig. 4-31, which is a divide-by-5 counter circuit. At CBA="100", the output of C is connected to CL through an AND gate. A capacitor is added to CL to prolong the "CLEAR" function. The capacitor will maintain the "1" state and keep the flip-flop in "CLEAR" mode when CK is dropping. At the negative edge of CK, the counter is still disabled.

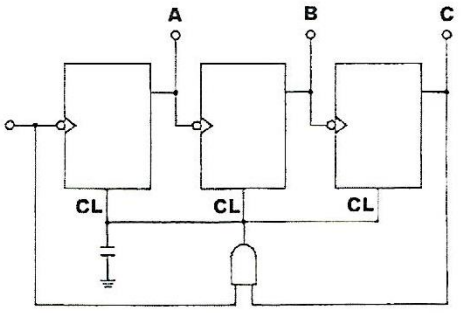


Fig. 4-31

Serial connection between divide-by-2 and divide-by-5 circuits forms a BCD counter. A 1Hz timing signal can be generated when industrial counters such as divide-by-10 or divide-by-6 are used in conjunction with 60Hz AC power. If all CKs are connected together, a synchronous counter is formed. Its operating speed is a lot faster than serially connected asynchronous counters but designing non 2^n counters with synchronous counters are much more complexed.

Fig. 4-32 shows a 4-bit divide-by-16 counter.

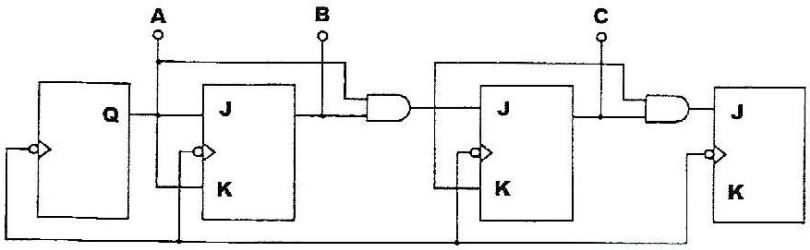


Fig. 4-32

Fig. 4-33 shows a synchronous divide-by-5 counter circuit. It is obviously that its structure is more complexed than the asynchronous counter.

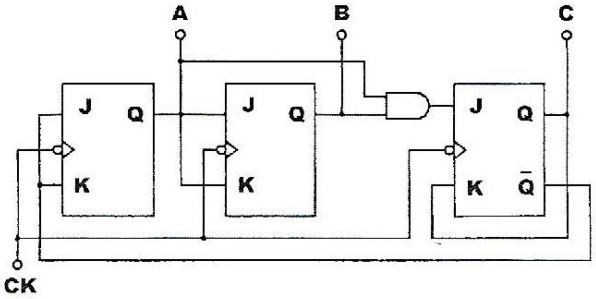


Fig. 4-33 Synchronous divide-by-5 counter

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Module KL-33009/KL-33010; Oscilloscope

PROCEDURES

(a) Asynchronous Binary Up-Counter

1. Insert connection clips according to Fig. 4-34 to construct the circuit of Fig. 4-35.

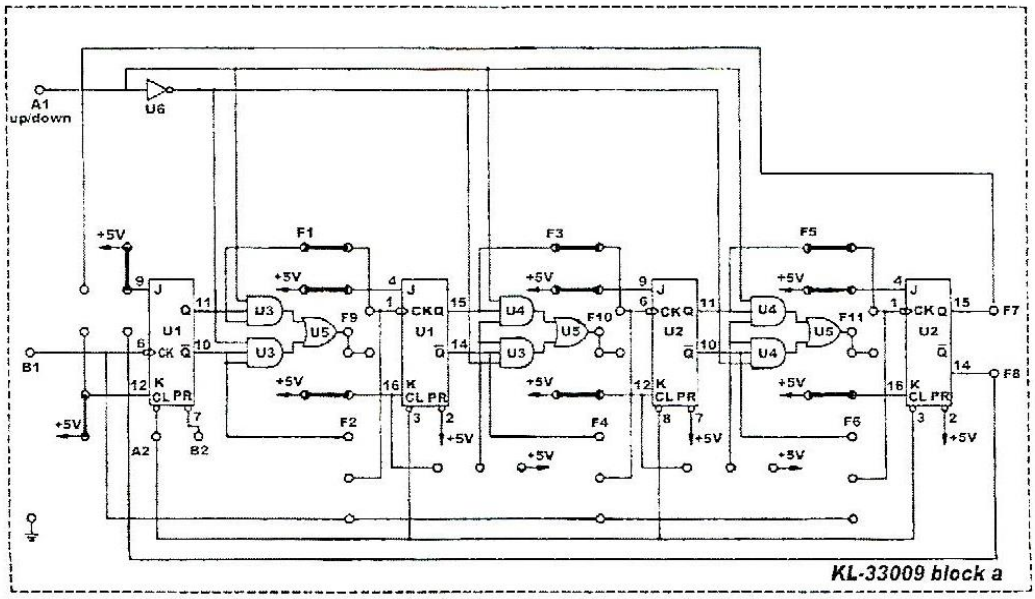


Fig. 4-34

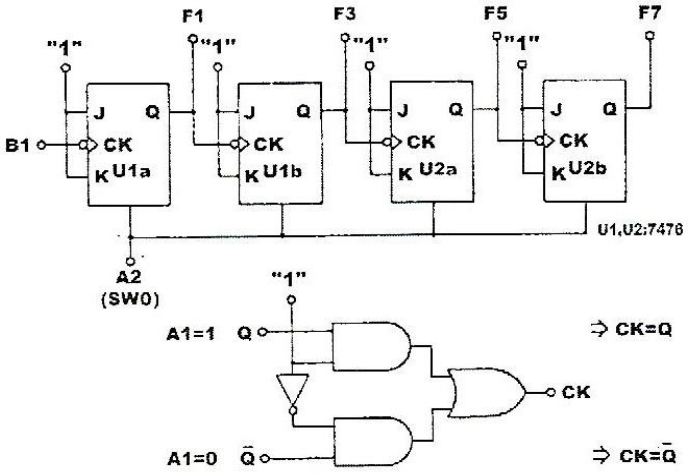


Fig. 4-35

2. Connect A2(Clear) to SW0; A1 to +5V; outputs F1, F3, F5, F7 to L1~L4 respectively and B1(CK) to the Clock Generator, adjust the output frequency to 1KHz.
3. Set SW0 to "1" initially to clear the output; then set SW0 to "0" to begin counting. Measure CK and the outputs with the oscilloscope, record the outputs in Fig. 4-36.

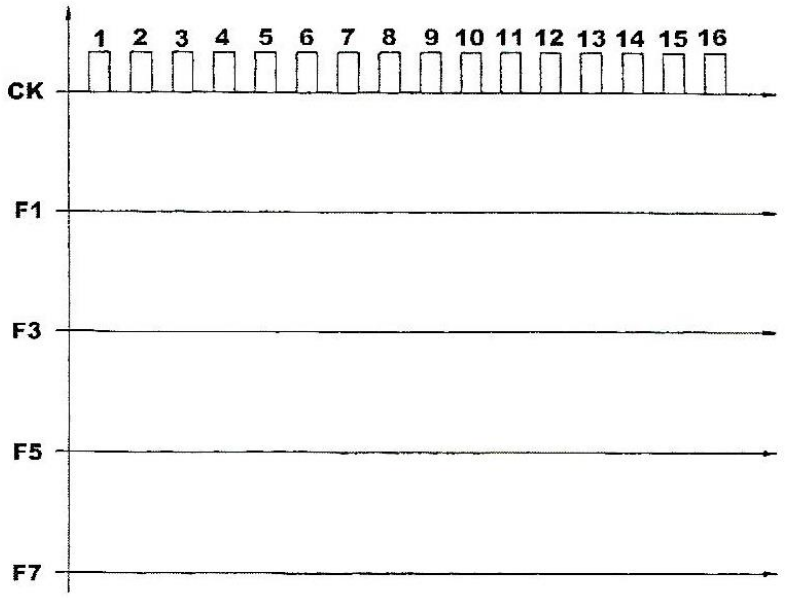


Fig. 4-36

4. What happens if SW0 is set to "1" during the counting process?

(b) Asynchronous Decade Up-Counter

1. U4 (7490) on module KL-33010 block d, shown on Fig. 4-37, will be used in this section of the experiment. Functional block diagram of U4 is shown in Fig. 4-38.

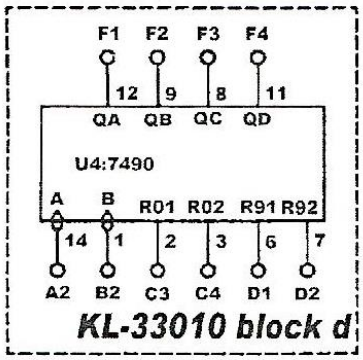


Fig. 4-37

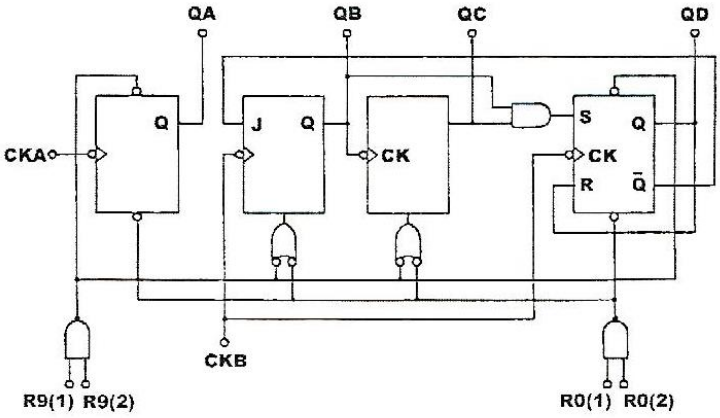


Fig. 4-38

2. Connect C3, C4 to SW0 and SW1; D1, D2 to SW2 and SW3; F1~F4 to L1~L4; A2 to SWA Q output; B2 to SWB Q output.

3. (A) Connect C3, C4, D1, D2 to ground and A2 to SWA Q pulse. Measure and record output waveforms in Fig. 4-39.

   (B) Connect C3, C4, D1, D2 to ground and B2 to SWB Q pulse. Measure and record output waveforms in Fig. 4-40.

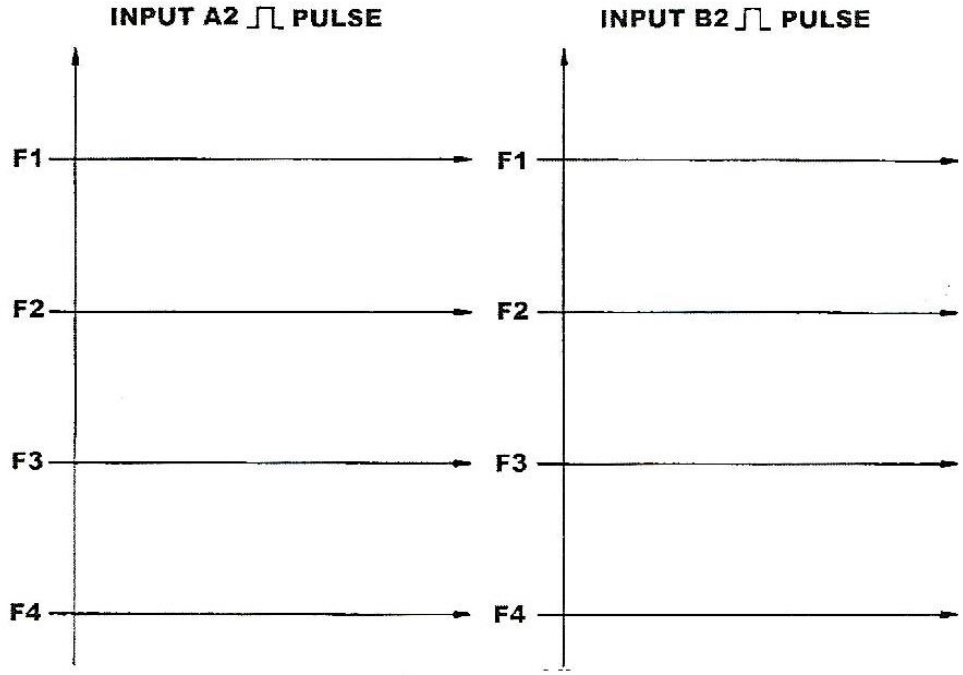


Fig. 4-39

Fig. 4-40

4. Connect F1 to B2; A2 to 1KHz pulse. Measure and record A2(CK), F1, F2, F3, F4 in Fig. 4-41.

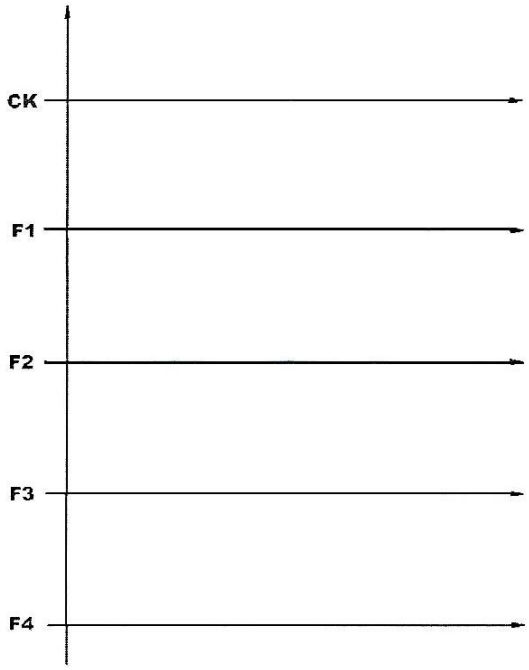


Fig. 4-41

5. Connect C3, C4 to +5V; D1, D2 to ground. What are the outputs?

6. Connect D1, D2 to +5V; C3, C4 to ground. What are the outputs?

(c) Asynchronous Divide-by-N Up-Counter

1. U3 (7493) on module KL-33010 block c, shown on Fig. 4-42, will be used in this section of the experiment. Functional block diagram of U3 is shown in Fig. 4-43.

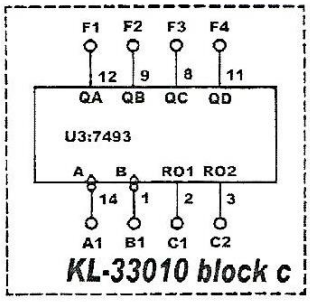


Fig. 4-42

LOGIC DIAGRAM

LS93

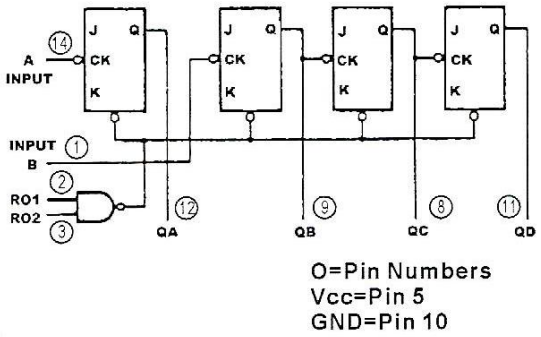


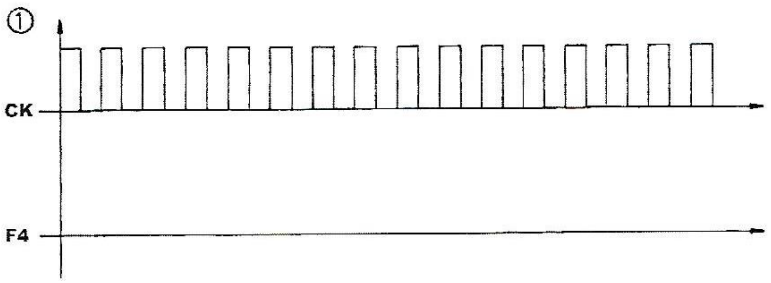
Fig. 4-43 Asynchronous divide-by-n counter

2. Connect B1(CK) to the output of the Clock Generator and connect outputs F2, F3, F4 to L2, L3, L4.

3 Connect inputs C1 and C2 (Clear) to one or two of the outputs F2, F3, F4 as indicated by Table 4-13. Observe and record the states of F2, F3, F4 in Table 4-13. Measure CK and F4 with an oscilloscope and sketch the output wavrforms. Determine which type of counter each connection represents.

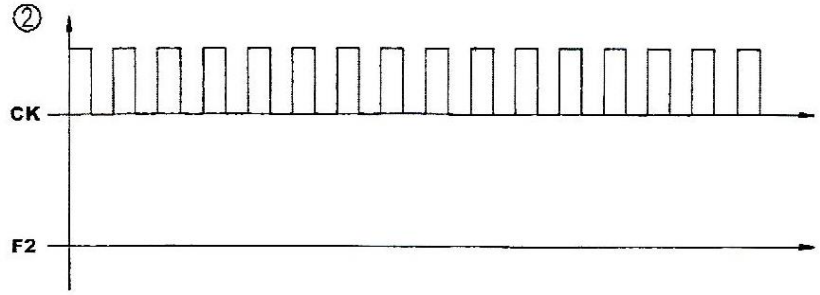
C1 C2	F2	F3	F4
① CONNECT F2			
② CONNECT F3			
③ CONNECT F4			
④ CONNECT F2 F3			
⑤ CONNECT F2 F4			
⑥ CONNECT F3 F4			

Table 4-13



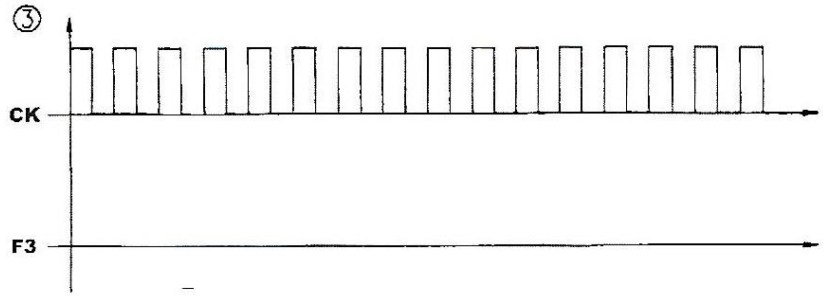
This is a divide-by-_____ circuit

②



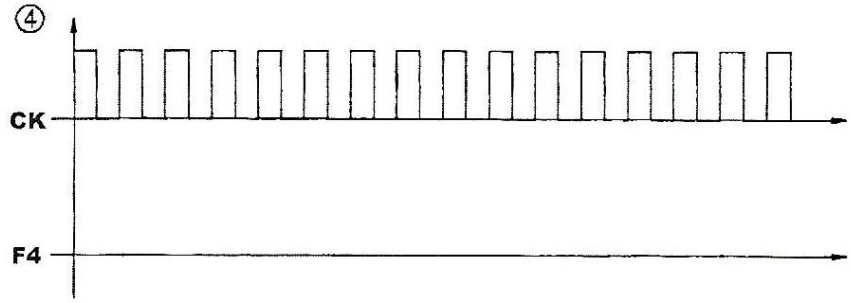
This is a divide-by-_____circuit

③



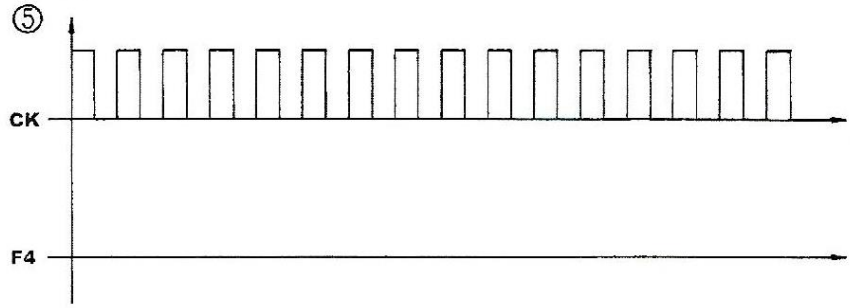
This is a divide-by-_____circuit

④

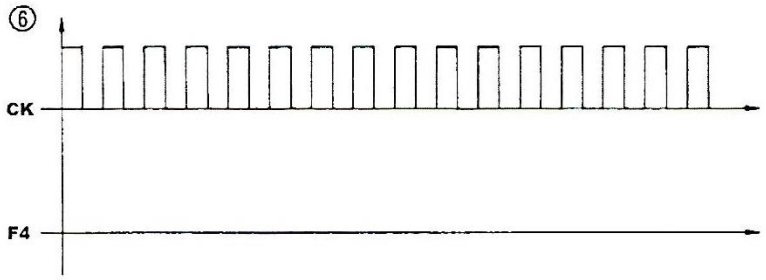


This is a divide-by-_____circuit

⑤



This is a divide-by-_____circuit



This is a divide-by-_____circuit

(d) Asynchronous Binary Down-Counter

1. Insert connection clips according to Fig. 4-44 to construct the circuit of Fig. 4-45.

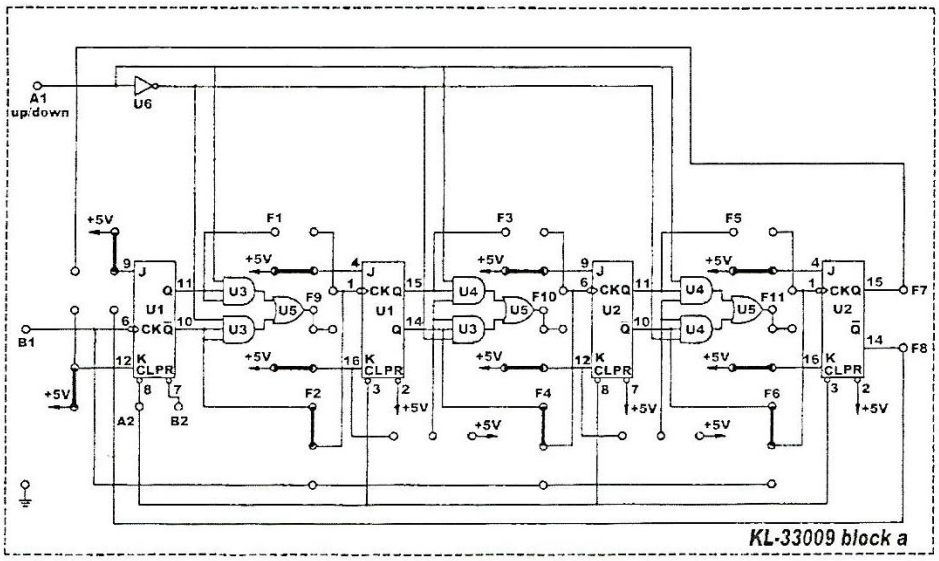


Fig. 4-44

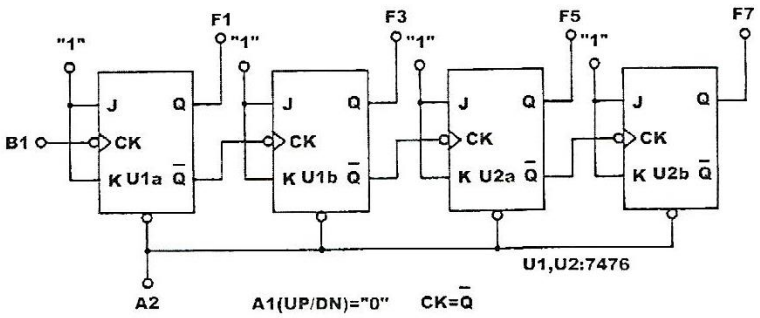


Fig. 4-45

2. Connect A2 (Clear) to SW0=5V; A1 to +5V; B1(CK) to 1KHz output of the Clock Generator.

   Connect F2, F4, F6, F8 to L5~L8. Measure the outputs with an oscilloscope. Sketch the output waveforms in Fig. 4-46

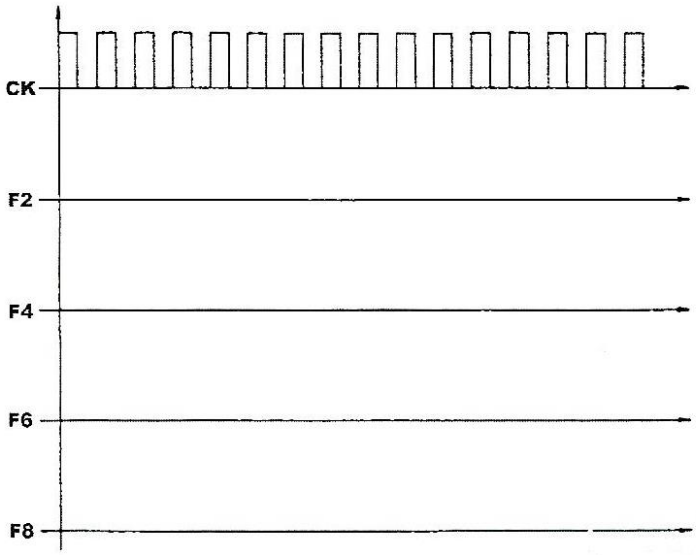


Fig. 4-46

(e) Synchronous Binary Up-Counter

1. Insert connection clips according to Fig. 4-47 to construct the circuit of Fig. 4-48.

2. Connect A1 to +5V; A2 (Clear) to SW1=5V; B1 (CK) to 1KHz output of the Clock Generator. Measure output waveforms with an oscilloscope. Sketch the output waveforms in Fig. 4-49.

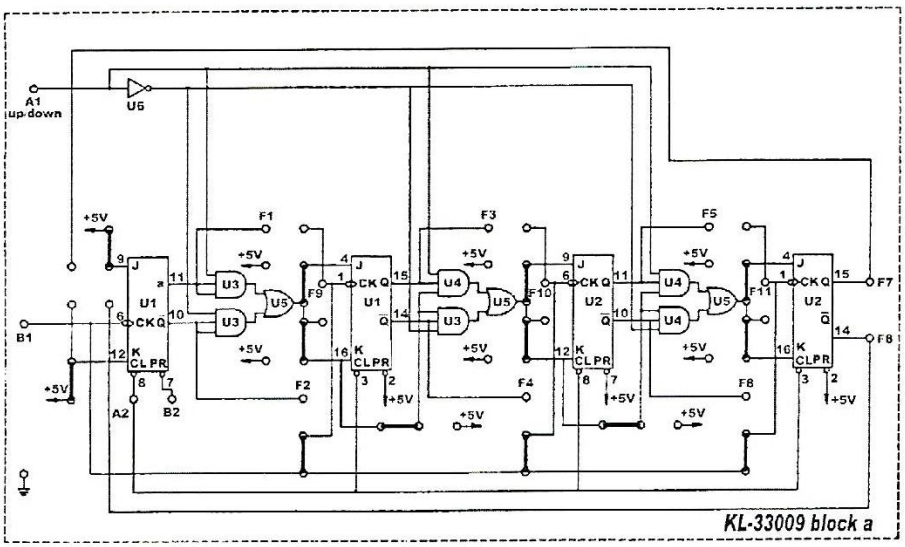


Fig. 4-47

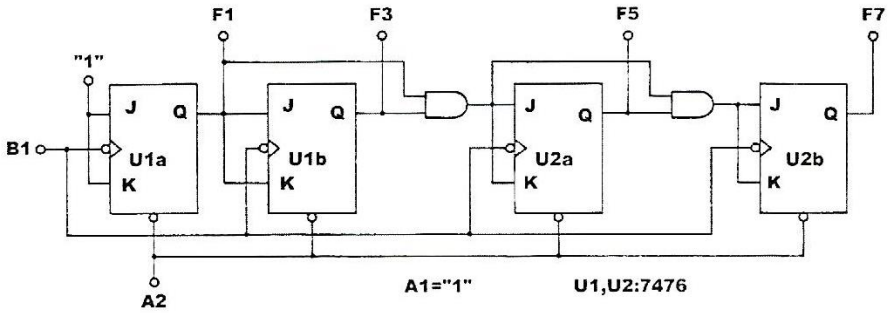


Fig. 4-48

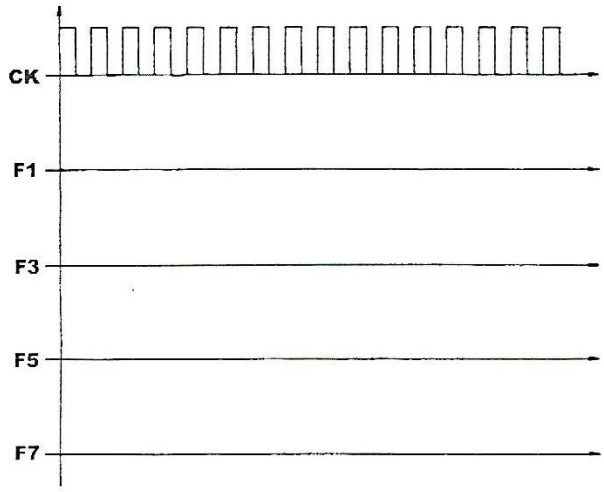


Fig. 4-49

(f) Synchronous Binary Up/Down Counter

1. Insert connection clips according to Fig. 4-50 to construct the circuit of Fig. 4-51.

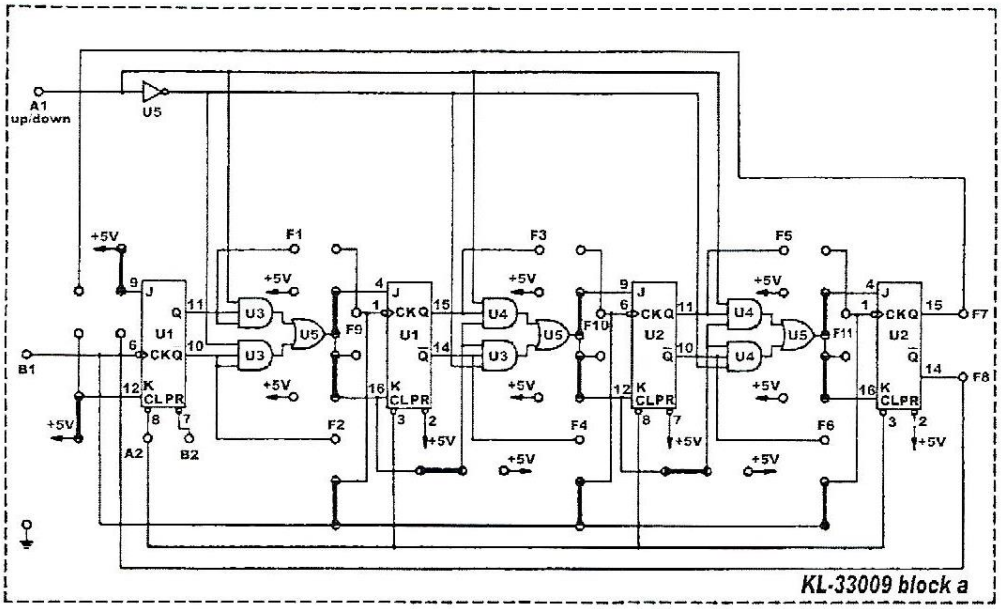


Fig. 4-50

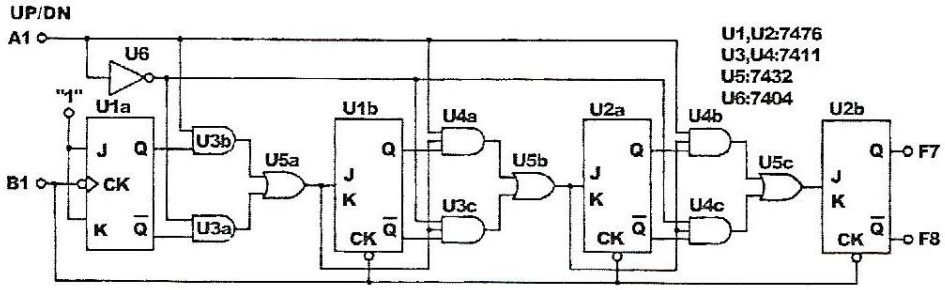


Fig. 4-51

2. Connect A2 (Clear) to SW1; A1 to SW2; B1 to 1KHz output of the Clock Generator.

   (A) At A1="1", measure waveforms at CK, F1, F3, F5, F7 with an oscilloscope. Sketch the output waveforms in Fig. 4-52.

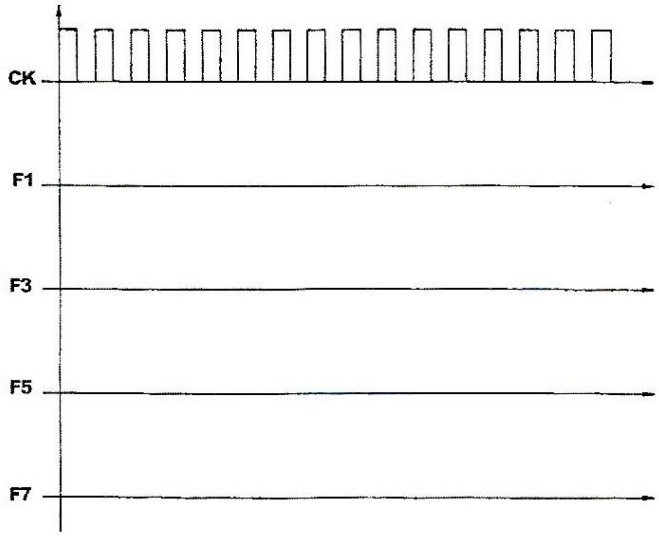


Fig. 4-52

(B) At A1="0", measure waveforms at CK, F1, F3, F5, F7 with an oscilloscope. Sketch the output waveforms in Fig. 4-53.

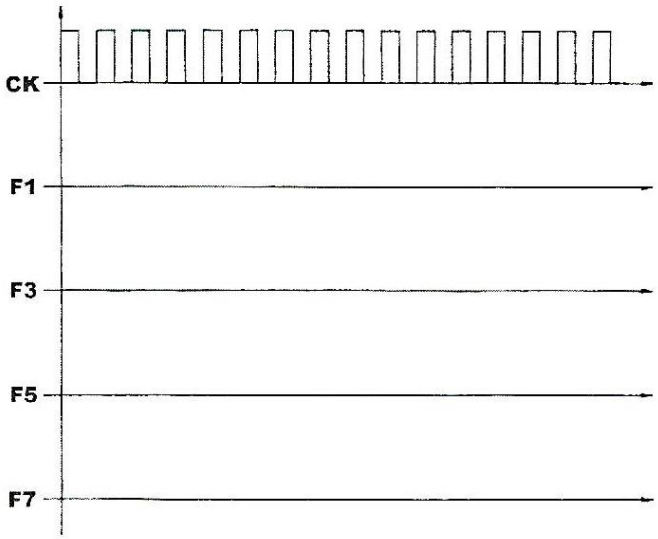


Fig. 4-53

Presetable Binary Up/Down Counter

1. U1 (74193) on module KL-33010 block a will be used in this section of the experiment. Table 4-14 is the truth table for the 74193.

DISCUSSION:

1 - Design 4-bit asynchronous down-counter?

2 - Design 4-bit asynchronous up/down counter?

3 - Design 3-bit up-synchronous counters by using T-F-F ?

4 - Design BCD counter using J-K F/F using Excitation table ?

5 - Design 3-bit up/down synchronous counter ?