Experiment No.7

Characteristics of Bipolar Junction

Object

The purpose of this experiment is to determine and graph the input and output characteristics of a bipolar junction transistor (BJT) in the common emitter configuration, and to measure its h-parameters at a given DC bias point.

Required Parts and Equipment's

1. Electronic Test Board. (M90)
2. Dual DC Power Supply.
3. Digital Multi-meters.
4. NPN Transistors (BC337).
5. Resistors 33kΩ,120Ω
6. Leads and Wires.

Theory

A bipolar junction transistor (BJT) is a three-terminal device capable of amplifying a small AC signal. The three terminals are called the base, emitter, the collector. BJTs consist of a very thin base material sandwiched between two of the opposite type materials. Bipolar transistors are available in two forms, either NPN or PNP. The middle letter indicates the type of material used for the base, while the outer letters indicate the emitter and collector terminals. The emitter is heavily doped, the base is lightly doped, and the collector is intermediately doped. Fig.1 shows BJT transistor construction and symbols.

As shown in Fig.1, two P-N junctions are formed when a transistor is made, the junction between the base and emitter, and the junction between the base and collector. These two junctions form two diodes, the emitter-base diode and the collector-base diode.

There are three configurations in connecting the BJT depending on which of the three terminals is used as the common terminal. These configurations are the common emitter (CE), the common base (CB), and the common collector (CC).

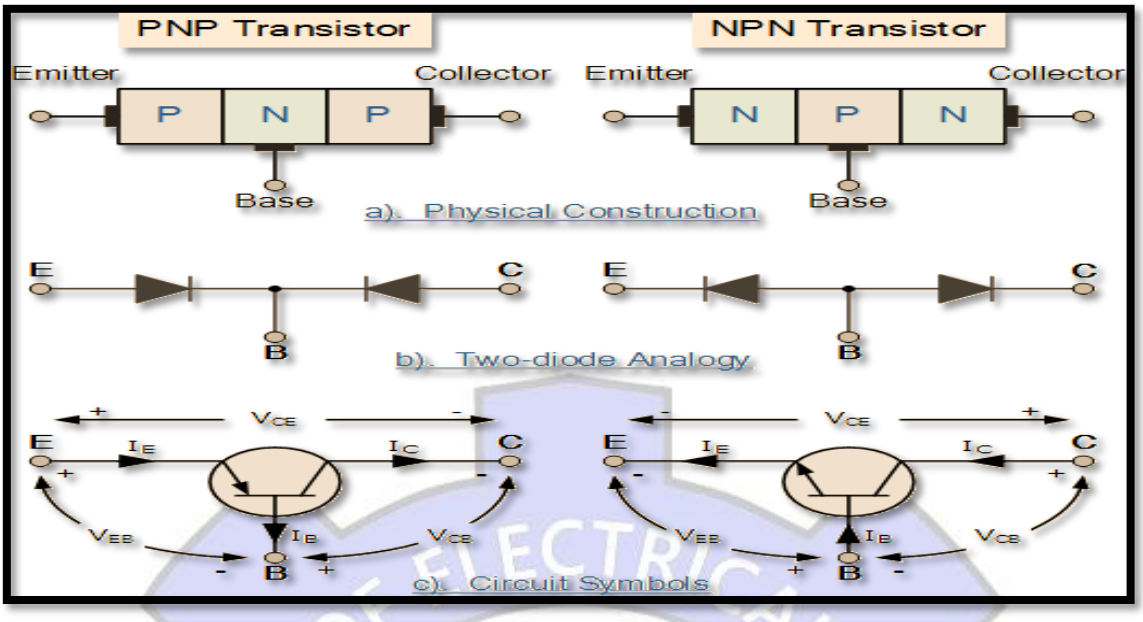


Figure 1: Types of BJT Transistors

Common emitter configuration is most effective because of its high current gain, high voltage gain and power gain. In common emitter configuration, emitter terminal is made common to both input and output circuits as shown in Fig.2. Input junction (Emitter-Base Junction) is forward biased and output junction (Collector-Base Junction) is reverse biased so that the input junction is having low resistance (since it is forward biased) and the output junction is having high resistance (since it is reverse biased).

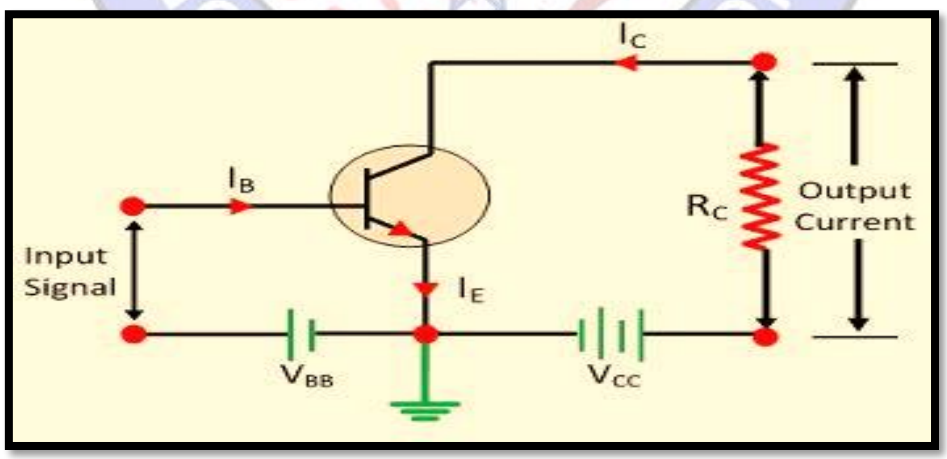


Figure 2: Common Emitter Transistor Configuration

Bipolar transistors are primarily current amplifiers. In the CE configuration, a small base current is amplified to a larger current in the collector circuit. The

ratio of the DC collector current I_C to the DC base current $I_B$is called the DC beta (β_{dc}) of the transistor. Thus:

$$\beta_{dc} = \frac{I_C}{I_B}$$

Typical values of β_{dc} range from 20 to 250 or higher. β_{dc} is usually designated as h_{FE}in transistor datasheets. Hence:

$$h_{FE}=\beta_{dc}$$

Another useful parameter in bipolar transistors is the DC alpha (α_{dc}). It is defined as the ratio of the DC collector current I_C to the DC emitter current I_E. Thus:

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Typically, values of αdc range from 0.95 to 0.99, but αdc is always less than 1.

- **Common Emitter Input and Output Characteristics**

Two sets of characteristics are necessary to describe fully the behavior of the common emitter configuration: the input (or base) characteristics, and the output (or collector) characteristics. Input characteristics of a transistor are curves showing the variation of input (base) current IB as a function of input (base-emitter) voltage V_{BE}, when the output (collector-emitter) voltage VCE is kept constant. Fig.3 depicts the input characteristics for a typical transistor.

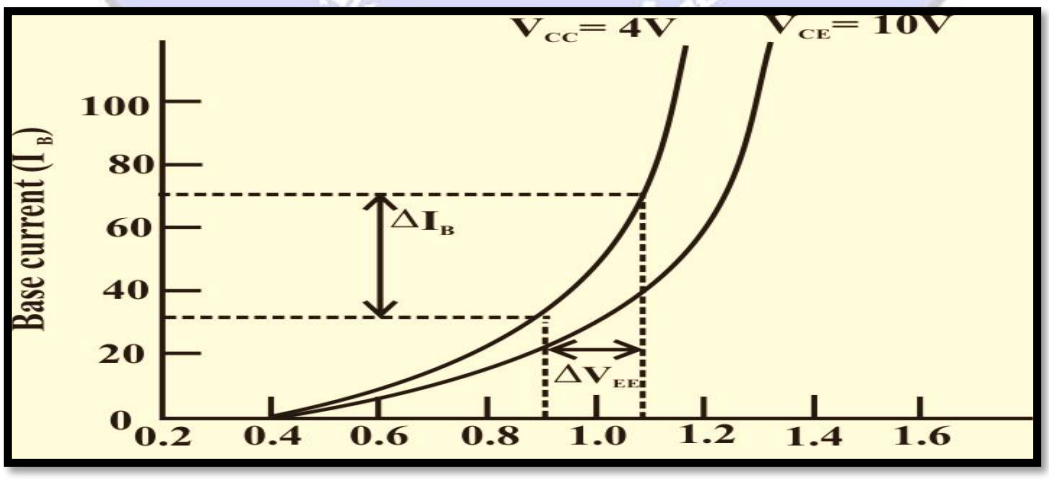


Figure 3: Typical Input Characteristics of a Silicon NPN Transistor in the Common Emitter Configuration

As shown from Fig.3, the input characteristics are similar to that of a forward-biased diode since the emitter-base junction is forward-biased. Note also the slight shift in the curves when increasing V_{CE}.

Output characteristics of a transistor are curves showing the variation of the output current I_C as a function of output voltage V_{CE}, when the input current I_B is kept constant. Fig.4 depicts the output characteristics for a typical transistor.

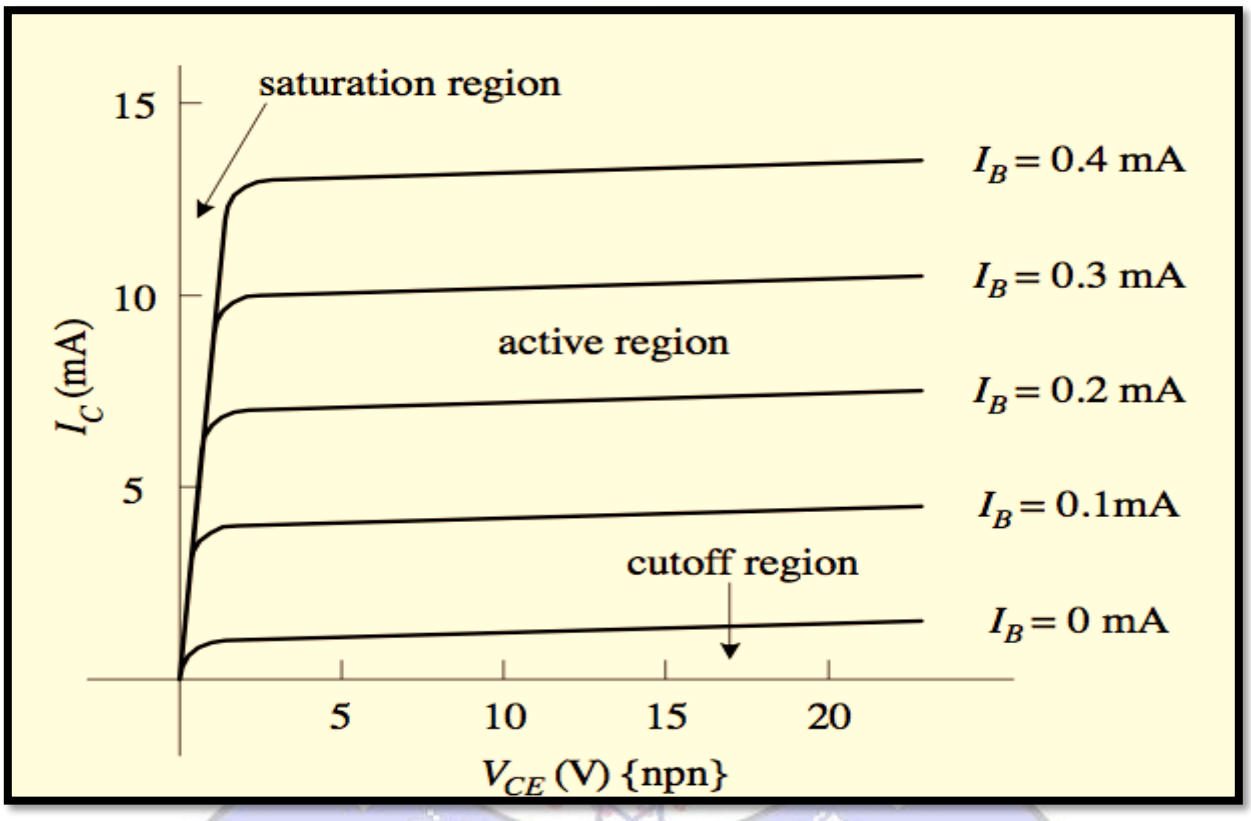


Figure 4: Typical Output Characteristics of a Silicon NPN Transistor in the Common Emitter Configuration

As shown from Fig.4, for very small values of V_{CE} the collector-base junction is forward biased and the transistor is in the saturation region. In this portion of the curves, I_C is increased linearly with V_{CE}. As V_{CE} increases, the collector-base junction becomes reverse-biased and the transistor goes into the active region. In this portion of the curves, I_C remains essentially constant (for a given value of I_B) as V_{CE} continues to increase. Actually, I_C increases very slightly as V_{CE} increases due to widening of the collector-base depletion region. For this portion of the characteristic curves, the value of I_C is only determined by the expression:

$$I_C = \beta_{dc} I_B$$

Fig.5 shows a common emitter circuit that can be used to generate the input and output characteristic curves. The purpose of RB in this circuit is to limit the base current to a safe level.

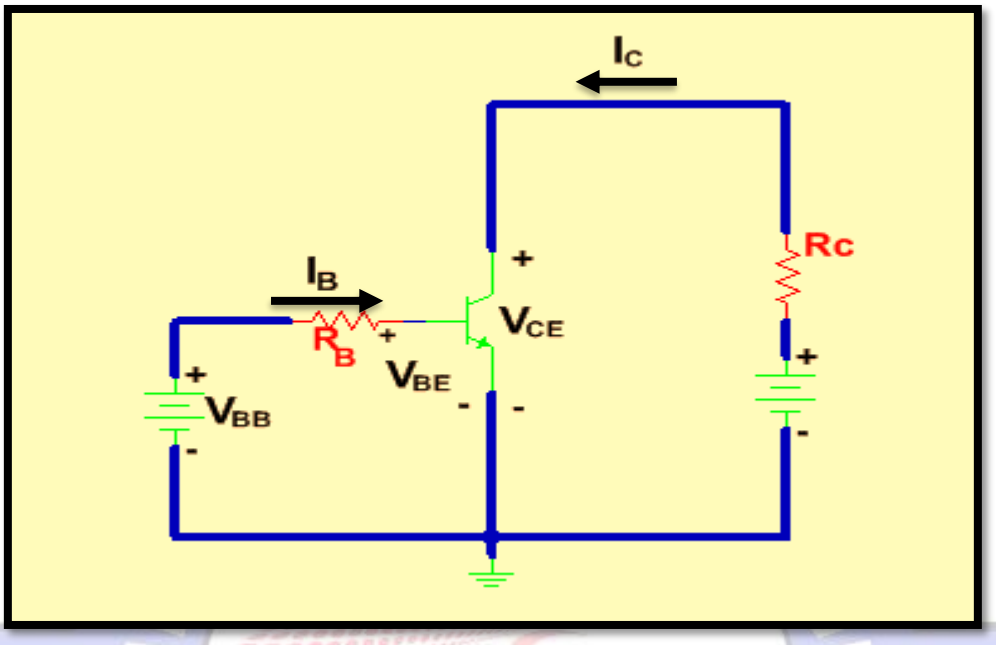


Figure 5: Test Circuit used to generate the Common Emitter Input and Output Characteristics

- **Transistor h-parameters**

In order to analyze transistor amplifier operation, an AC small signal model for the BJT is required. The most widely used equivalent circuit model to describe the transistor behavior at low and mid-band frequencies is the h-parameter model. For the common emitter configuration, when the transistor is considered as a linear two port network, the input small signal AC voltage (v_{be}) and the output small signal AC current (i_c) can be expressed in terms of the input current (i_b) and output voltage (v_{ce}) by the following equations:

$$v_{be} = h_{ie}.i_b + h_{re}.v_{ce}$$
$$i_c = h_{fe}.i_b + h_{oe}.v_{ce}$$

The common emitter hybrid parameters in equation 4 are defined as:

h_{ie}= input resistance $= \frac{v_{be}}{i_b} \Big|_{v_{ce}=0}$

h_{re}= reverse transfer voltage ratio = $\frac{v_{be}}{v_{ce}} \Big|_{i_{b=0}}$

h_{fe}= forward transfer current ratio = $\frac{i_c}{i_b} \Big|_{v_{ce=0}}$

h_{oe}= output conductance = $\frac{i_c}{v_{ce}} \Big|_{i_{b=0}}$

The unit of h_{ie} is the Ohm, and that of h_{oe} is the Siemens, while hfe and hre are unit-less. This versatility in the units is the reason behind the name of the hybrid parameters.

Fig.6 shows the small-signal AC equivalent circuit of the transistor in the common emitter configuration.

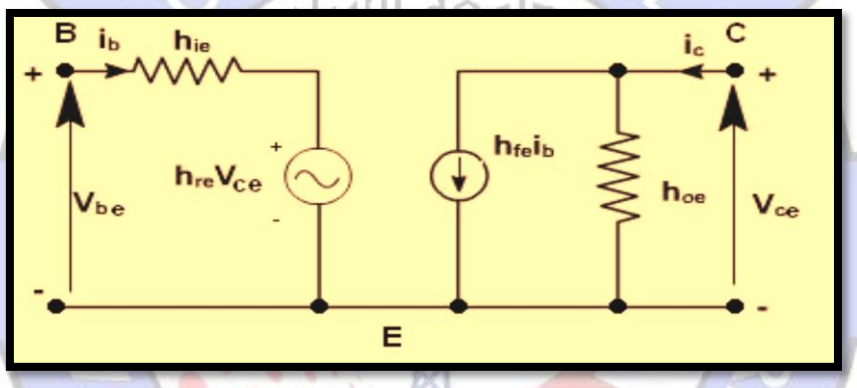


Figure 6: Common Emitter Transistor Hybrid Equivalent Circuit Model

The h-parameters of the transistor can be determined graphically from its input and output characteristics. The parameters h_{ie} and hre are determined from the input (or base) characteristics, while the parameters h_{fe} and h_{oe} are obtained from the output (or collector) characteristics.

Fig.7 presents the method of finding the input resistance h_{ie} graphically at the specified Q-point of the transistor. It should be noted that h-parameters depend on the specific operating point (Q-Point) of the transistor. As observed from the figure, h_{ie} is determined from the equation:

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE=const.}}$$

The small increments ΔI_B and ΔV_{BE} should be taken around the Q-point as depicted in Fig.7.

The parameter h_{re} can also be obtained from the input characteristics as shown in Fig.8. In this case:

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\Big|_{I_{B=const.}}$$

The base current I_B should be taken as the Q-point operating value I_{BQ}. The parameter h_{re} is very low and can be ignored in most practical cases.

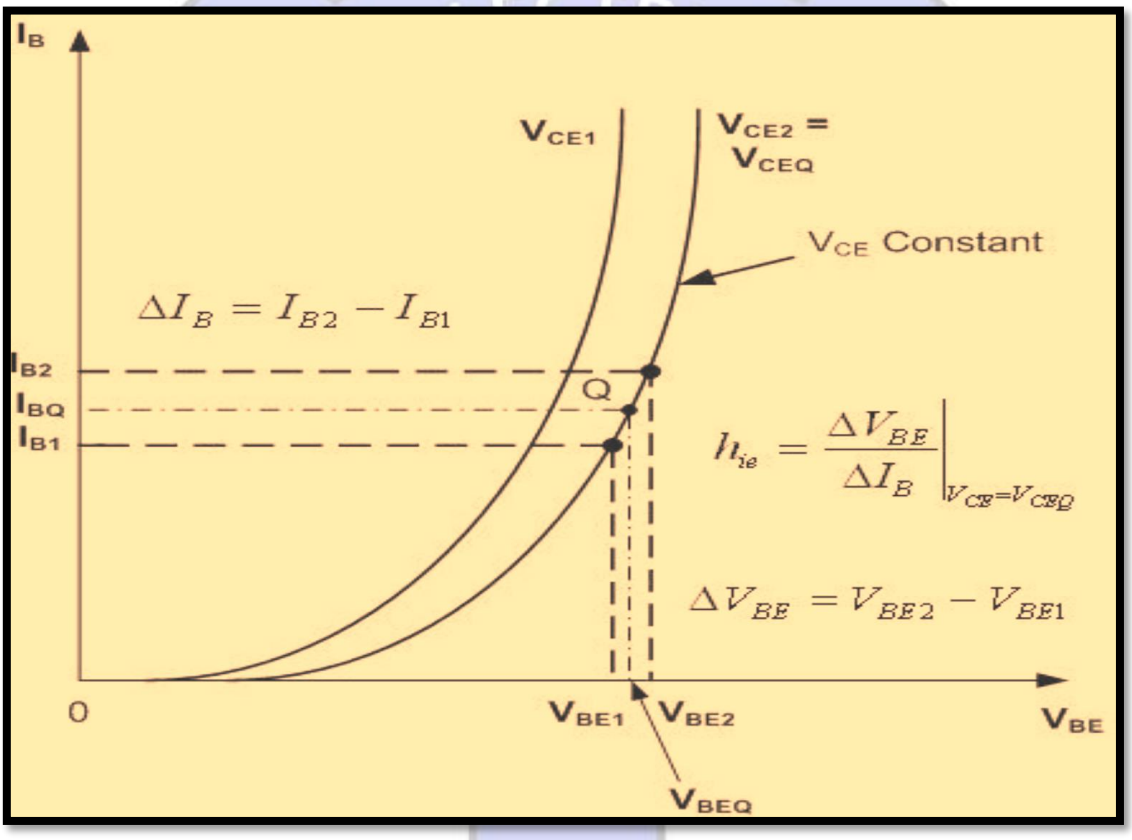


Figure 7: Graphical Determination of h_{ie} from the Input Characteristics

The small signal current gain h_{fe} can be determined from the output characteristics of the transistor as shown in Fig.9. As shown from this figure, h_{fe} can be found from:

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE=const.}}$$

Actually, h_{fe} represents the AC beta of the transistor:

$$h_{fe} = \beta_{ac}$$

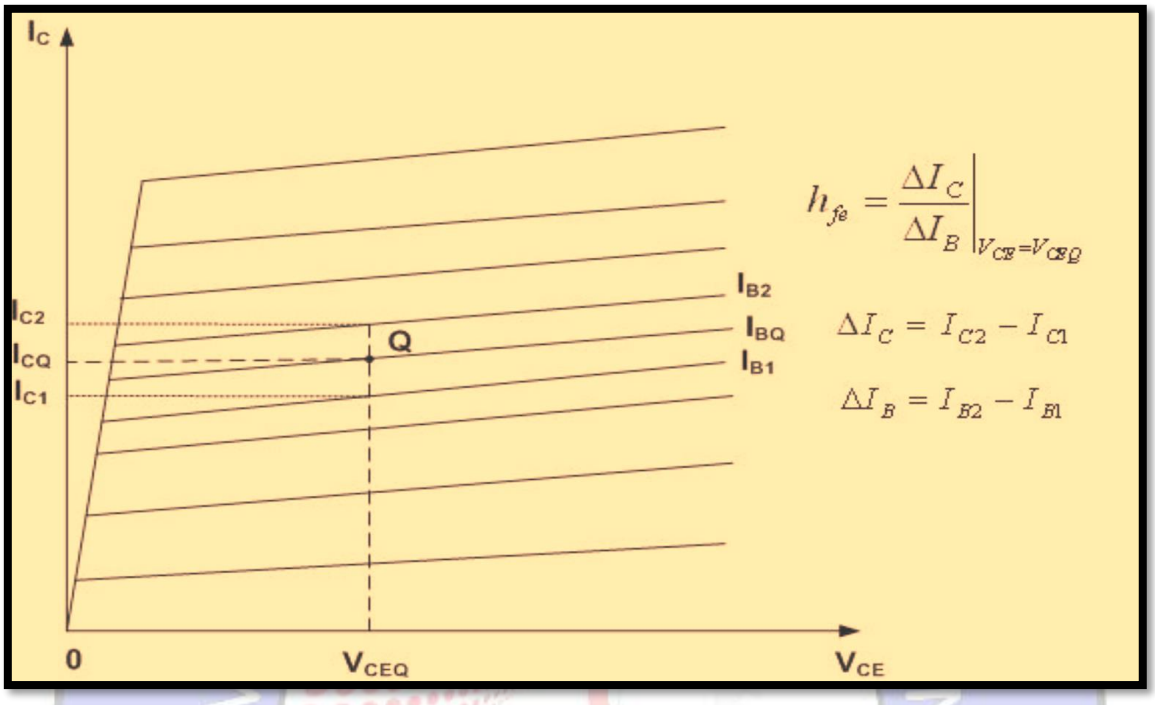


Figure 9: Graphical Determination of h_{fe} from the Output Characteristics

If I_C is plotted against I_B for a given V_{CE}, then an approximate linear relation can be obtained in the active region of the transistor as shown in Fig.10.

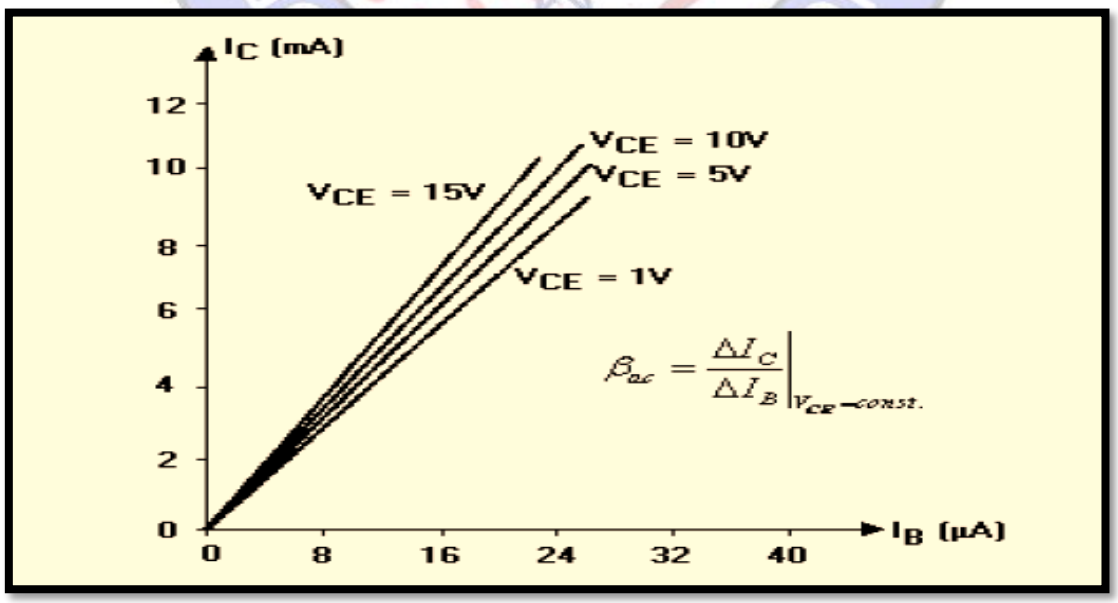


Figure 10: I_C versus I_B for a Typical Transistor in the Active Region

The output conductance h_{oe} can also be gotten from the output characteristics of the transistor at a specific Q-point as shown in Fig.11. In this case:

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \Big|_{I_{B=const.}}$$

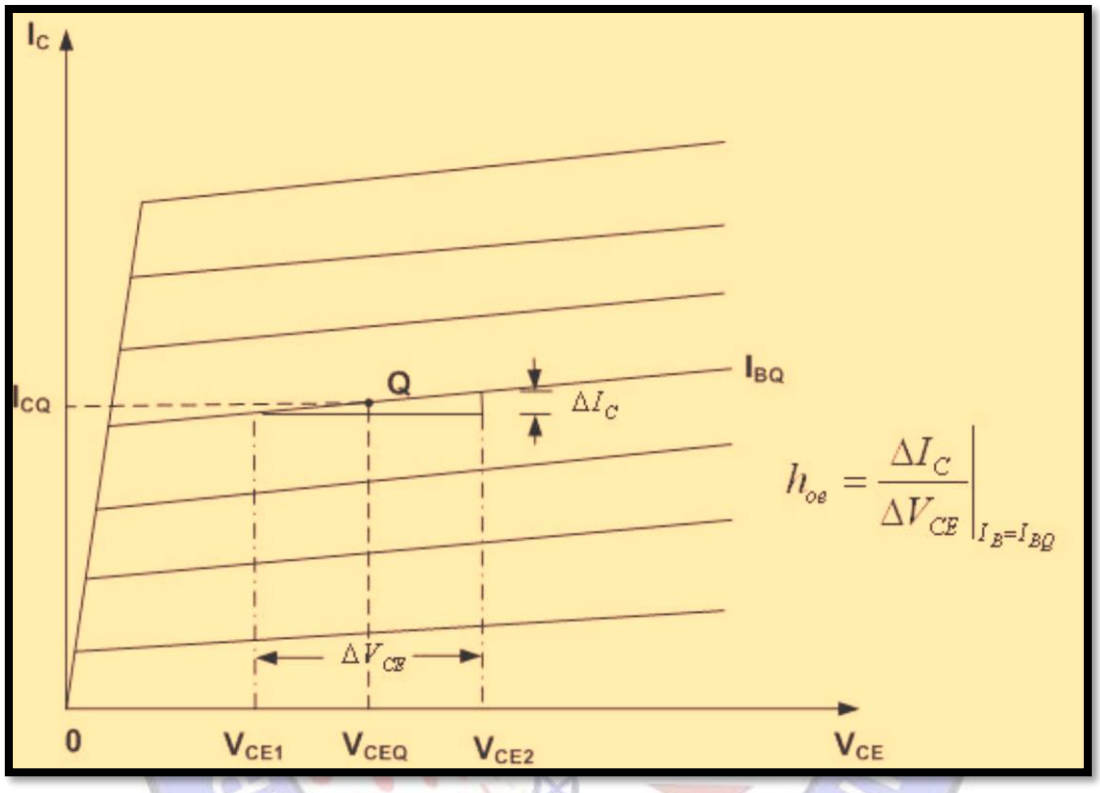


Figure 11: Graphical Determination of hoe from the Output Characteristics

Procedure

1. Connect the common emitter test circuit shown in Fig.12. Try to identify the leads of the BC337 transistor correctly. It is built in a M90 package as depicted in Fig.12.
2. Set V_{CE} = 0V, and increase the base current I_B in several steps from 0 to 100µA by varying the DC supply voltage V_{BB}, and record V_{BE} in each step as shown in Table-1.
3. Reduce V_{BB} to 0V and set V_{CE} = 5V by adjusting the DC power supply V_{CC}. Increase I_B from 0 to 100µA (by slowly increasing V_{BB}) in several steps and record V_{BE}. V_{CE} should be kept constant at 5V in each step by adjusting V_{CC}.

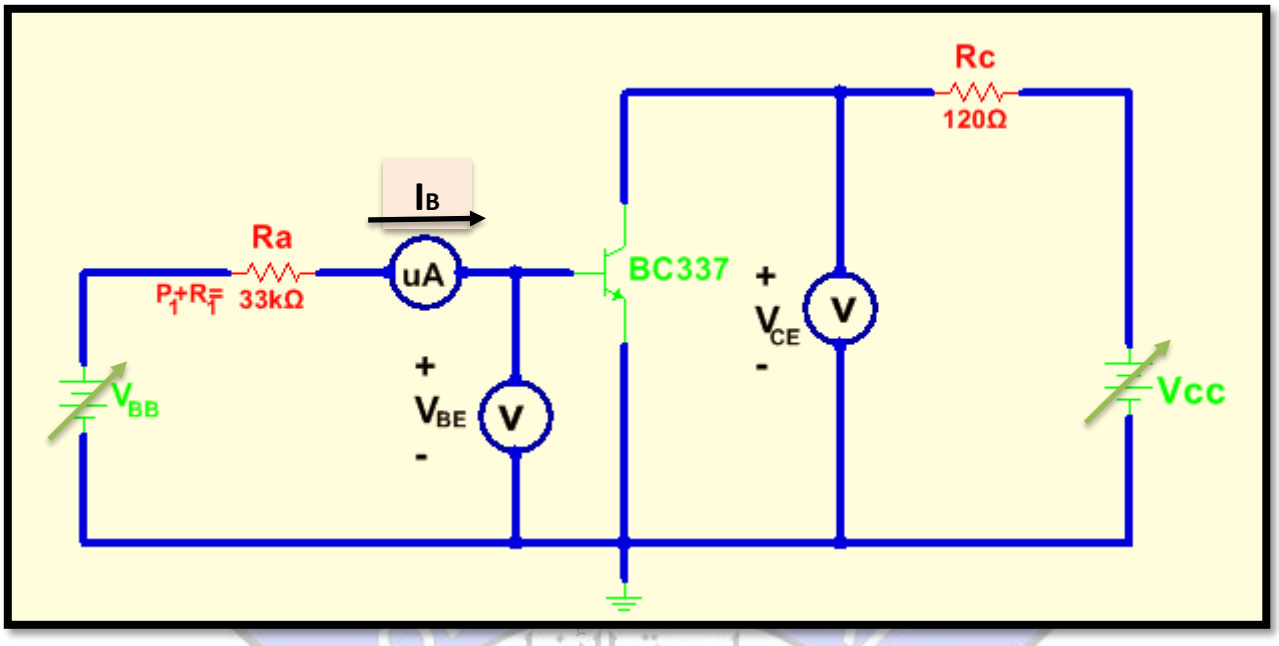


Figure 12: Transistor Test Circuit Used to obtain the Input Characteristics

V_{CE} = 0V		V_{CE} = 5V	
I_B(μA)	$V_{BE(V)}$	I_B(μA)	V_{BE}(V)
0		0	
10		10	
20		20	
30		30	
40		40	
50		50	
60		60	
70		70	
80		80	
90		90	
100		100	

Table-1: Recorded Data for the Transistor Input Characteristics

4. Connect the circuit shown in Fig.13 to obtain the output characteristics of the transistor.

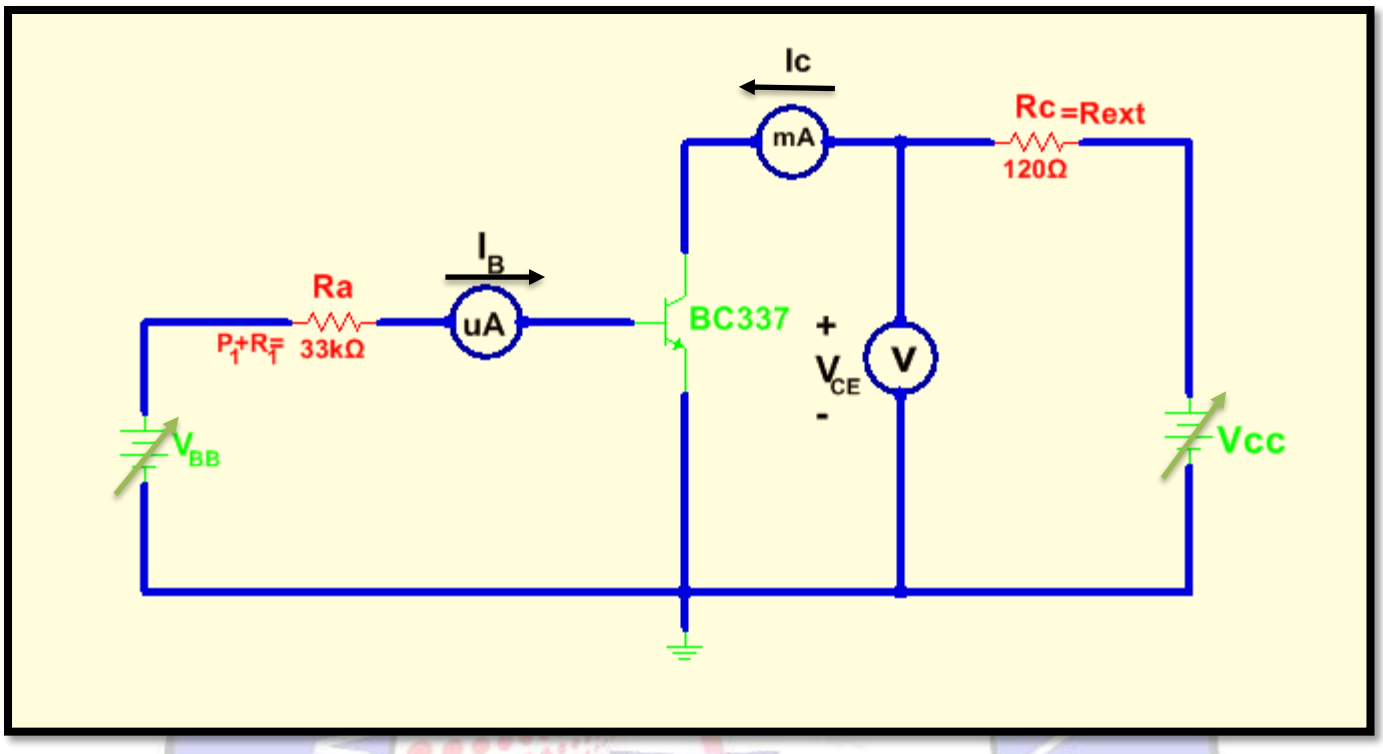


Figure 13: Transistor Test Circuit Used to obtain the Output Characteristics

5. Start with both power supplies set to 0V. Slowly increase V_{BB} until $I_B = 20\mu A$. Now slowly increase V_{CC} in several steps and record V_{CE} and I_C in each step as shown in Table-2.
6. Repeat step 5 for base current values of 40μA, and 60μA respectively. Record data as illustrated in Table-2.

$I_B(\mu A)$ =20		$I_B(\mu A)$ =40		$I_B(\mu A)$ =60	
$V_{CE(V)}$	I_C (mA)	$V_{CE(V)}$	I_C (mA)	$V_{CE(V)}$	I_C (mA)
0		0		0	
0.1		0.1		0.1	
0.2		0.2		0.2	
0.4		0.4		0.4	
0.6		0.6		0.6	

0.8		0.8		0.8	
1		1		1	
3		3		3	
5		5		5	
8		8		8	
10		10		10	

Table-2: Recorded Data for the Transistor Output Characteristics

Discussion

1. From the obtained data in Table-1, plot the input characteristic curves of the transistor.
2. Sketch the three output characteristic curves of the transistor from the results obtained in Table-2.
3. Find the *h-parameters* of the transistor at I_B = 40μA and V_{CE} = 5V from the plotted input and output characteristics.
4. Use the plotted characteristic curves to determine the DC current gain β_{dc} for the transistor at V_{CE} = 3.0V and base current of 20μA, 40μA, and 60μA respectively. Repeat for V_{CE} = 5.0V. Tabulate your results as illustrated in Table-3 below.
5. Does the experimental data indicate that β_{dc} is constant at all points? Does this have any effect on the linearity of the transistor? What effect would a higher β_{dc} have on the characteristic curves you measured?
6. What is the maximum power dissipated in the transistor for the data taken in the experiment?
7. Show that the DC alpha of the transistor is given by: 1+

$$\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc} + 1}$$

   Compute α_{dc} for your transistor at V_{CE} = 5.0V and I_B = 40μA.

8. What value of V_{CE} would you expect if the base terminal of the transistor is opened? Explain your answer.

Experiment No.8

Transistor DC Biasing Circuits

Object

The purpose of this experiment is to determine the DC operating point (Q-point) for the transistor fixed-bias circuit, and the voltage divider bias circuit, and also to compare between their bias stabilities against changes in the transistor beta.

Required Parts and Equipment's

1. Electronic Test Board. (M90, M100)
2. DC Power Supply.
3. Digital Multi-meters.
4. NPN Transistors (BC337).
5. Resistors.M90 (470kΩ, 1.74KΩ), M100(39KΩ,3.3KΩ,4.7KΩ,470Ω)
6. Leads and Wires.

Theory

The analysis or design of a transistor amplifier requires knowledge of both the DC and the AC response. The analysis or design of any amplifier therefore has two components: the DC portion and the AC portion. In fact, the improved output AC power level is the result of a transfer of energy from the applied DC supplies.

The term biasing refers to the application of DC voltages to establish a fixed level of current and voltage. For transistor amplifier, the resulting DC current and voltage establish an operating point on the characteristics that define the region that will be employed for the amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (Q-point). The biasing circuit should be designed to set the device operation at a Q-point within the active region. For the BJT to be biased in the active region, the following must be verified:

1. The base-emitter junction must be forward-biased, with a resulting forward-bias voltage of about 0.6 to 0.7V.

2. The base-collector junction must be reverse-biased, with the reverse-bias voltage being any value within the maximum limits of the device.

- **The Fixed-Bias Circuit**

The Fixed-Bias circuit of Fig.1 is the simplest DC bias configuration.

In the base-emitter loop, applying KVL yields:

$$V_{CC} = I_B.R_B + V_{BE}$$

Solving for I_B, we have:

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

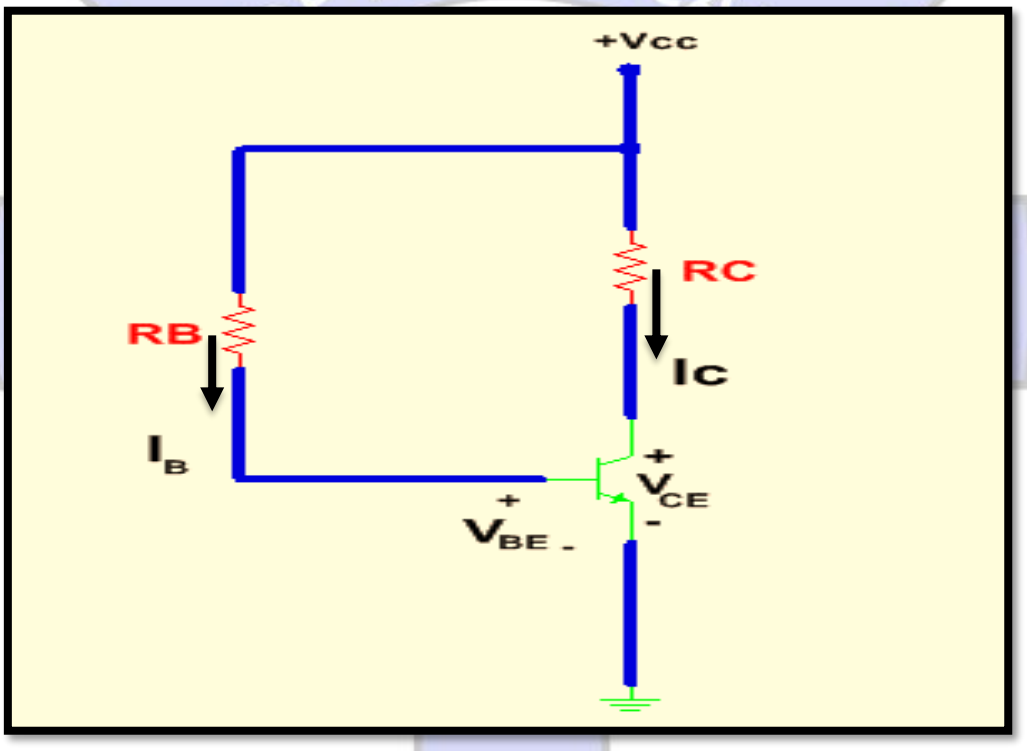


Figure 1: The Fixed -Bias Transistor Circuit

The collector current is related to base current by:

$$I_{CQ} = \beta.I_{BQ}$$

Therefore,

$$I_{CQ} = \beta(\frac{V_{CC} - V_{BE}}{R_B})$$

In the collector-emitter loop, we have:

$$V_{CC} = V_{CEQ} + I_{CQ}.R_C$$

Solving for V_{CE} yields:

$$V_{CEQ} = V_{CC} - I_{CQ}.R_C$$

The transistor operating point is I_{CQ}, V_{CEQ}.

To sketch the DC load line, the saturation and cut-off limits should be obtained.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE(off)} = V_{CC}$$

Although the fixed-bias circuit is very simple in construction, it has poor stability, and the Q-point may change or shift considerably if the transistor parameters (β and V_{BE}) change with temperature. This will result in change in the characteristics of the amplifier circuit.

The value of V_{BE} can be taken as 0.7V theoretically for silicon transistors. However, the measured practical value may be slightly different from the theoretical value.

- **The Voltage-Divider Bias Circuit**

In the fixed bias circuit, the bias current I_{CQ} and voltage V_{CEQ} are functions of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, this may result in change in bias current and voltage. Therefore, it would be desirable to develop a bias circuit that is independent of the transistor beta. The voltage divider circuit shown in Fig.2 is such a circuit. Voltage-Divider bias circuit is often used because the base current is made small compared to the currents through the two base (voltage-divider) resisters. Consequently, the base voltage and therefore the collector current are stabilized against changes in the transistor beta.

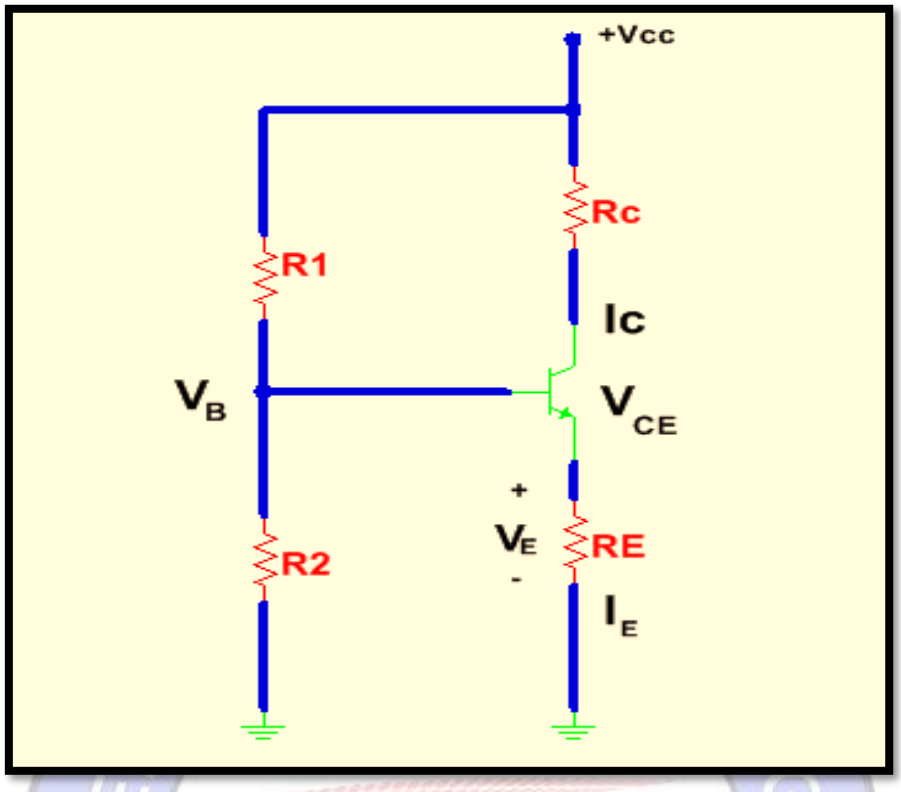


Figure 2: The Voltage-Divider Bias Circuit

The approximate analysis of the voltage divider bias circuit can be established by neglecting the base current I_B when compared to the current flowing in resistor R_2 .This is justified by assuming that the input resistance seen from the base is much greater than R_2 ($R_{i=}$ β. R_E $>> R_2$). Thus, the necessary condition for the approximate analysis of the circuit is:

$$\beta . R_E \geq 10R_2$$

In this case, the base voltage is given by:

$$V_B = \frac{V_{CC} . R_2}{R_1 + R_2}$$

The DC emitter voltage is given by:

$$V_E = V_B - V_{BE}$$

Quiescent DC collector current can be found from:

$$I_{CQ} \cong I_{EQ} = \frac{V_E}{R_E}$$

Collector voltage is found as:

$$V_C = V_{CC} - I_{CQ}.R_C$$

The quiescent DC collector-to-emitter voltage is calculated from:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

The collector saturation current in this case is given by:

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C + R_E}$$

$V_{CE(sat)}$ is approximately equal to 0.2V for silicon transistors. The collector-emitter voltage at cut-off is:

$$V_{CE(off)} = V_{CC}$$

Procedure

1. Connect the circuit shown in Fig.3. Use the NPN transistor BC337 in (M90).

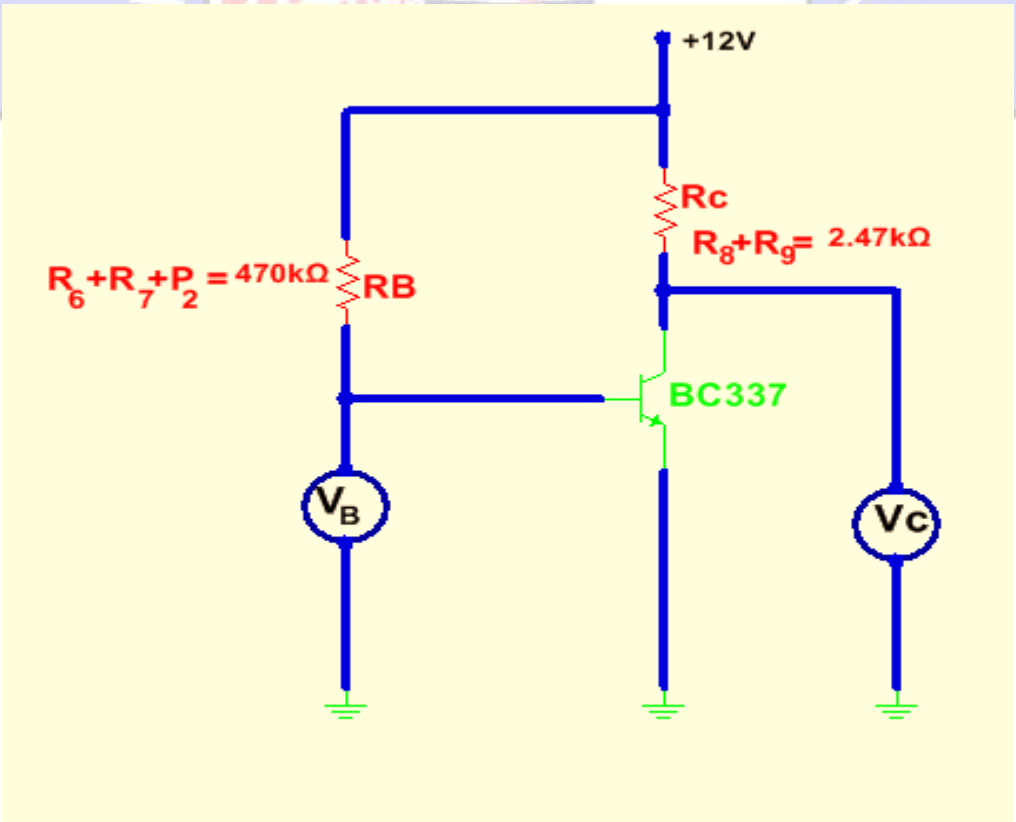


Figure 3: Practical Fixed Bias Transistor Circuit

2. Measure the DC voltages V_C and V_B using digital multi-meters. Determine the quiescent base current, collector current, and collector- emitter voltage, where:

$$I_{BQ} = \frac{V_{CC} - V_B}{R_B}$$

$$I_{CQ} = \frac{V_{CC} - V_C}{R_C}$$

$$V_{CEQ} = V_C$$

$$V_{BEQ} = V_B$$

3. Measure the transistor current gain as follows:

$$\beta_{dc} = \frac{I_{CQ}}{I_{BQ}}$$

4. Calculate the expected values of I_{BQ}, I_{CQ}, and V_{CEQ}. Use the value of β determined in step 3 above. Assume that V_{BE} = 0.7 theoretically. Tabulate you results as shown in Table 1.

Transistor 1 BC337		
Quantity	Measured	Calculated
V_B		
V_C		
V_{BEQ}		
V_{CEQ}		
I_{BQ}		
I_{CQ}		
V_{CEQ}		
β_{dc}		

Table 1: Measured and Calculated Transistor Parameters for the Fixed Bias Circuit

5. Connect the voltage-divider bias circuit shown in Fig.4. (use npn transistor in (M100)).

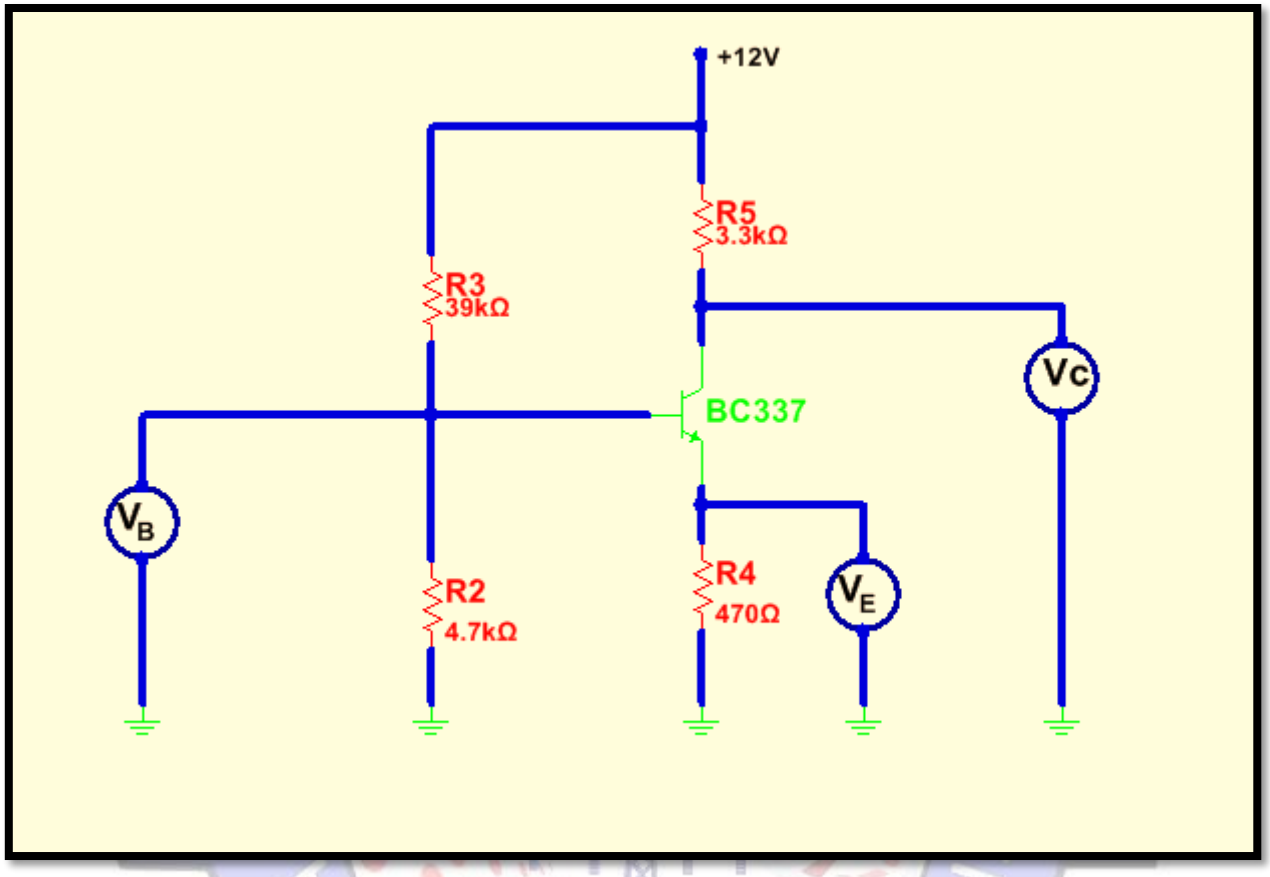


Figure 4: Practical Voltage-Divider Transistor Bias Circuit

6. Measure the DC voltages V_B, V_E, and V_C using digital multi-meters. Determine the quiescent point of the transistor as follows:

$$I_{CQ} \cong I_{EQ} = \frac{V_E}{R_E}$$

$$V_{CC} = V_{CEQ} + I_{CQ}.R_C$$

$$V_{CEQ} = V_{CC} - I_{CQ}.R_C$$

Discussion

1. Perform the theoretical calculations to determine the Q-point for both circuits and for each transistor, and compare them with the measured values.
2. Determine the drift in the Q-point for the two biasing circuits and therefore compare their bias stabilities.
3. Sketch the DC load line for the fixed bias circuit for each transistor case and place the Q-point on it.
4. Sketch the DC load line for the voltage divider bias circuit for each transistor case and place the Q-point on it. Is there a difference between the load lines in this case?
5. What is the effect of increasing resistor R_2 in the voltage-divider bias circuit on I_{CQ}? How should we select its practical value for better stability considerations?
6. What is the effect of decreasing resistor R_B on I_{CQ} for the fixed – bias circuit? What is its minimum value to ensure that the transistor is working in the active region?
7. For the fixed bias circuit of Fig.3, if the minimum β of the transistor is specified in the datasheet as 50, and the maximum value is 250, then determine the range of the Q-point of the transistor.
8. Sketch the circuit diagram of the collector-feedback bias circuit and compare its stability with that of the voltage-divider bias circuit.

Experiment No.3

Logic Gate Circuits

Object

The purpose of this experiment is to implement the basic logic gate circuits and verify them.

Required Parts and Equipment's

1. Electronic Test Board. (M60, M90)
2. 5V DC Power Supply.
3. Digital Voltmeter.
4. Two BC 337 NPN silicon Transistors.
5. Resistors.M90 (10kΩand 1KΩ)
6. Two 1N4001 Silicon Diodes.

Theory

A logic gate is a switching circuit with two or more inputs and whose output will be either a high voltage or a low voltage, depending on the voltages on the various inputs. Logic gates are widely used in computers and in all types of digital circuits and systems.

Digital circuits are characterized by the fact that they contain voltages that exist at either of two levels, for example 0V and 5V. In other words, at any instant of time each circuit input and output voltage will either be at some LOW voltage (V_L) or some HIGH voltage (V_H). In practice, the LOW level is actually a range of voltages, as is the HIGH level. For example, between 0V and 0.8V might be the low level, and between 2V and 5V might be the HIGH level. The range of voltages between 0.8V and 2V is not allowed except during transitions between V_H and V_L. This concept is illustrated in Fig.1.

There are several types of logic gates, and many different ways to construct each type using discrete components. The basic logic gates are the OR gate, AND Gate, NOT gate, NOR gate, and NAND gate.

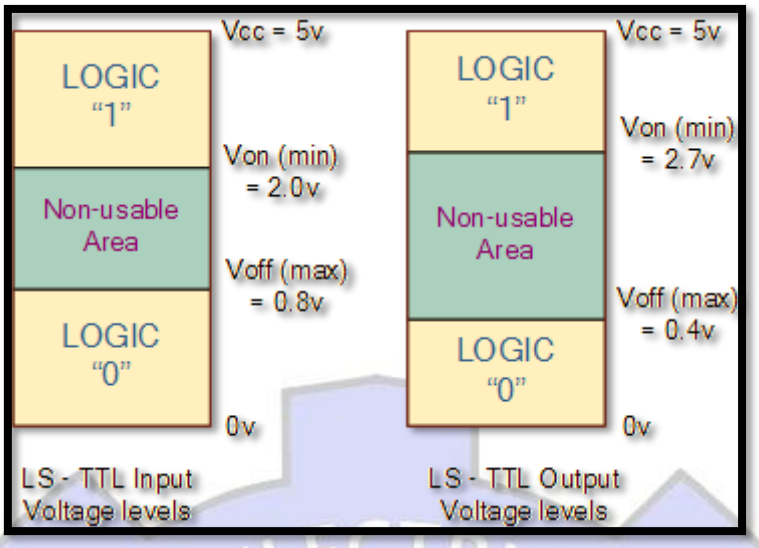


Figure1: Typical Voltage Levels in a Digital System

- **Diode OR Gate**

An OR gate is a circuit that has two or more inputs and whose output is equal to the OR sum (Logical Addition) of the inputs. Fig.2 shows the logic symbol and truth table of a two input OR gate.

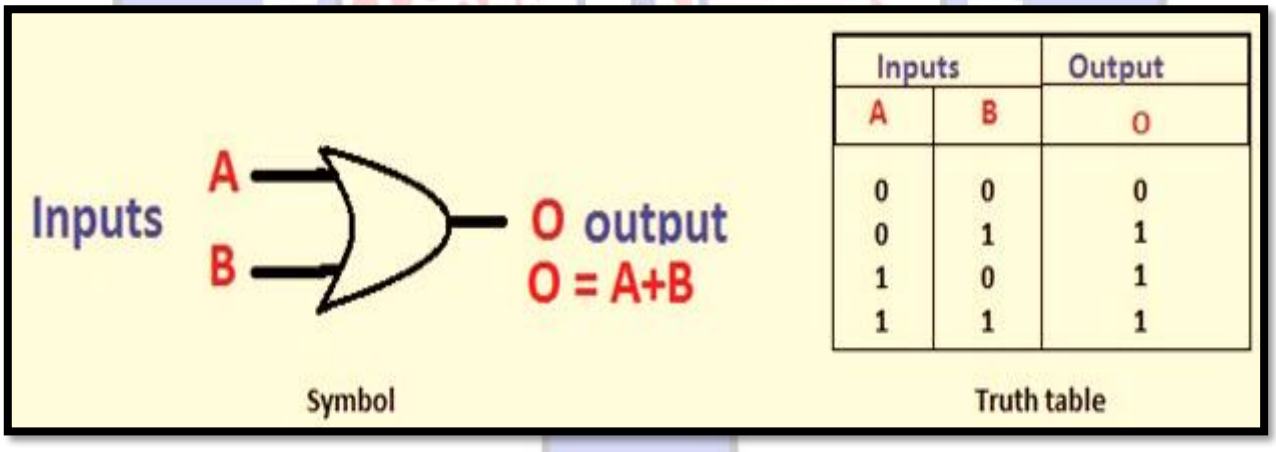
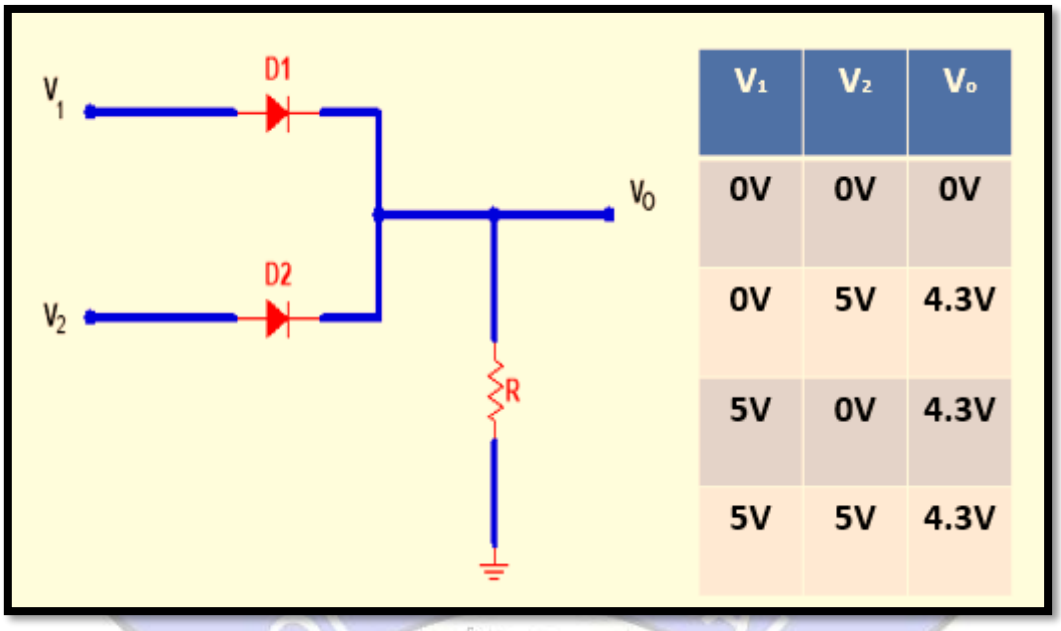


Figure 2: The Logic Symbol and Truth Table of the OR Gate

The OR gate operates such that its output is HIGH (Logic 1) if either input A or B or both are at a logic -1 level. The OR gate output will be LOW (logic 0) only if all its inputs are at logic- 0. Fig.3 presents a discrete circuit for the OR gate using two diodes and a resistor. Each input can be at either 0V or 5V, so there are four possible input combinations.



V_1	V_2	V_o
0V	0V	0V
0V	5V	4.3V
5V	0V	4.3V
5V	5V	4.3V

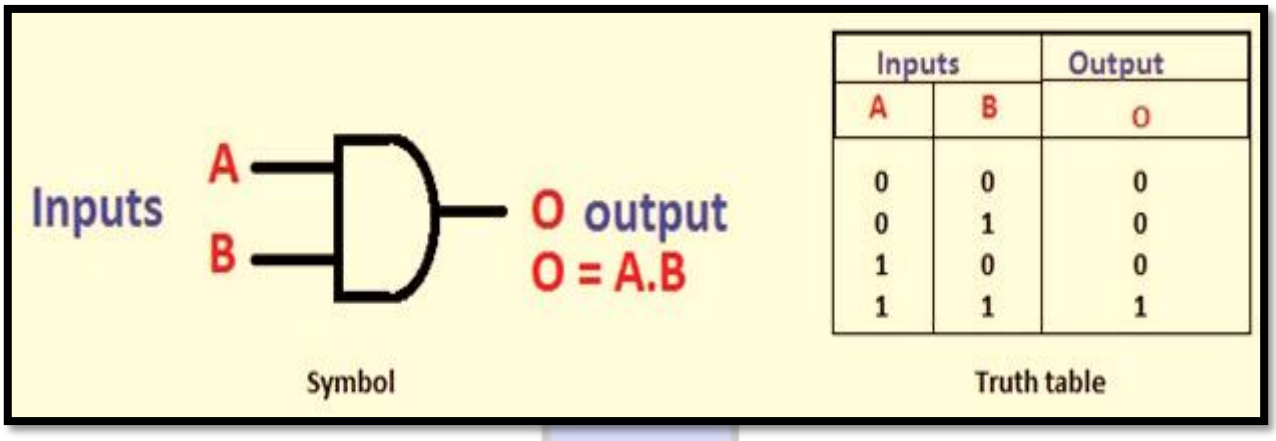
Figure 3: Two-input OR Gate Circuit

Examination of the truth table shows that the output will be at a HIHG level when either V_1 or V_2 or both are at a HIHG level. The value of V_o is LOW only when both inputs are at a LOW level.

Consider first the case where $V_1 = V_2 = 0V$. In this case neither diode will conduct; thus, no current flows in the circuit, and the output voltage is zero. When $V_1 = 0V$ and $V_2 = 5V$ then diode D_2 will be forward biased because its anode is made positive relative to its cathode. Thus, current will flow through D_2 and R. If the diodes are assumed to be silicon, the forward voltage drop across D_2 will be 0.7V, so V_0 must equal 5V - 0.7V = 4.3V. Diode D1 is reverse biased because its cathode is at +4.3 V relative to ground, and its anode is at 0V. The third case, where V1 = 5V and $V_2 = 0V$, will obviously be the same as the second case except that D1 will be ON, and D_2 will be OFF. In the final case, where both V_1 and V_2 are 5V, both diodes are ON, so each will have a 0.7V drop. Again, the output will be 4.3V.

- **Diode AND Gate**

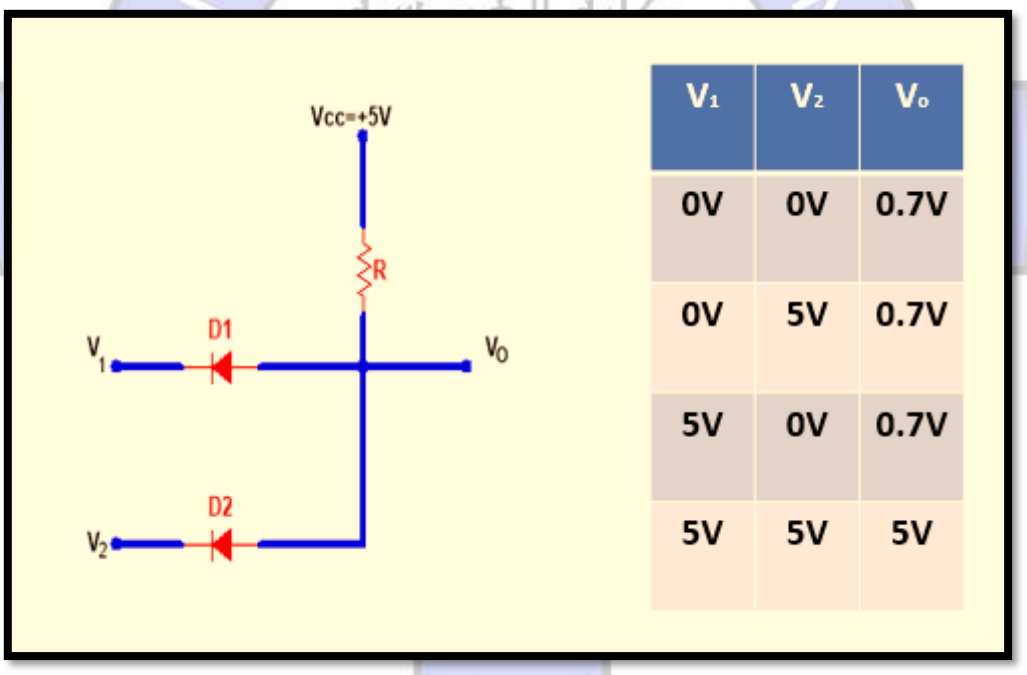
The second logic gate is the AND gate. Its symbol and truth table are presented in Fig.4. The output is equal to the AND product of the logic inputs (Logical Multiplication). The AND gate operates such that its output is HIGH only when all its inputs are HIGH. For all other cases the AND gate output is LOW.



Inputs		Output
A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4: The Logic Symbol and Truth Table of the AND Gate

The electronic circuit for the AND gate is shown in Fig.5. Consider the first case when $V_1 = V_2 = 0V$. In this case both diodes will be forward-biased and conduct current.



V_1	V_2	V_o
0V	0V	0.7V
0V	5V	0.7V
5V	0V	0.7V
5V	5V	5V

Figure 5: Two-input AND Gate Circuit

The output voltage in this case will equal the voltage drop across the diodes, which is 0.7V. When $V_1 = 0V$ and $V_2 = 5V$, diode D_1 will have its cathode at 0V, and thus will be forward - biased. So, current will flow from the 5V supply through R and D_1. Diode D_2 is OFF, since its cathode is at +5V. The output voltage V0 will be 0.7V, which is the voltage drop across D_1. In the third case when $V_1 = 5V$ and V_2

= 0V, diode D_1 will be OFF and D_2 will be ON and V0 will equal the voltage drop across D_2 which is 0.7V. Finally, when $V_1 = V_2 = 5V$, both diodes will be OFF and thus no current will flow through resistor R resulting in a zero voltage across R and 5V across the output ($V_0 = V_{CC} - V_R = 5V - 0 = 5V$).

- **The NOT Gate Circuit**

The NOT gate has a single input and output. The output equals the inverse of the input or the complement of the input. Fig.6 shows the symbol for the NOT gate, which is also called an inverter.

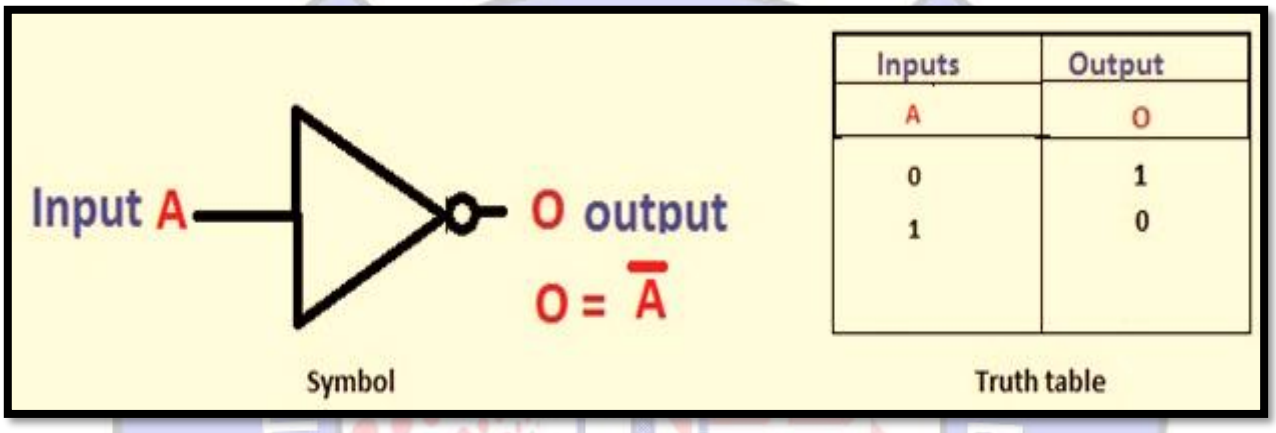


Figure 6: The Logic Symbol and Truth Table for the NOT Gate

The most widely used inverter circuit uses a bipolar transistor in the common-emitter configuration as shown in Fig.7. The input signal is applied to the base and the output is taken from the collector.

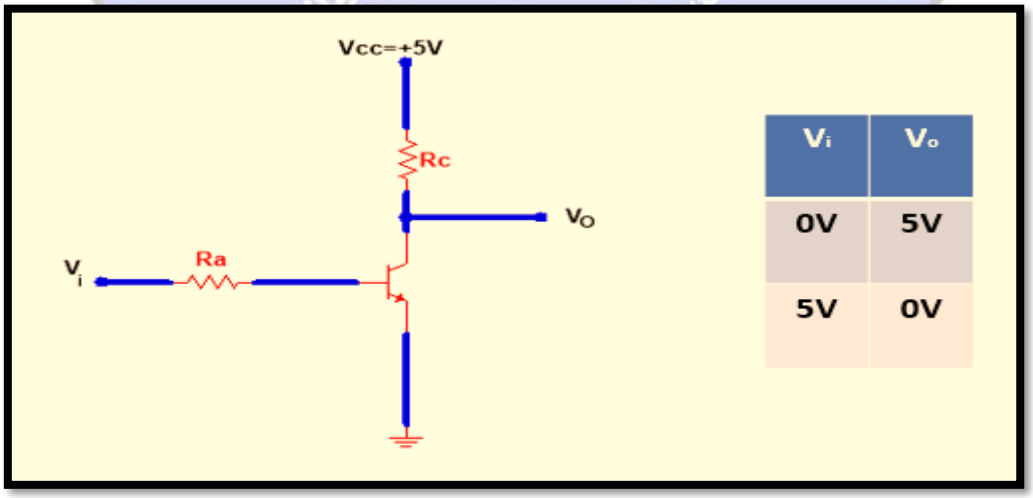


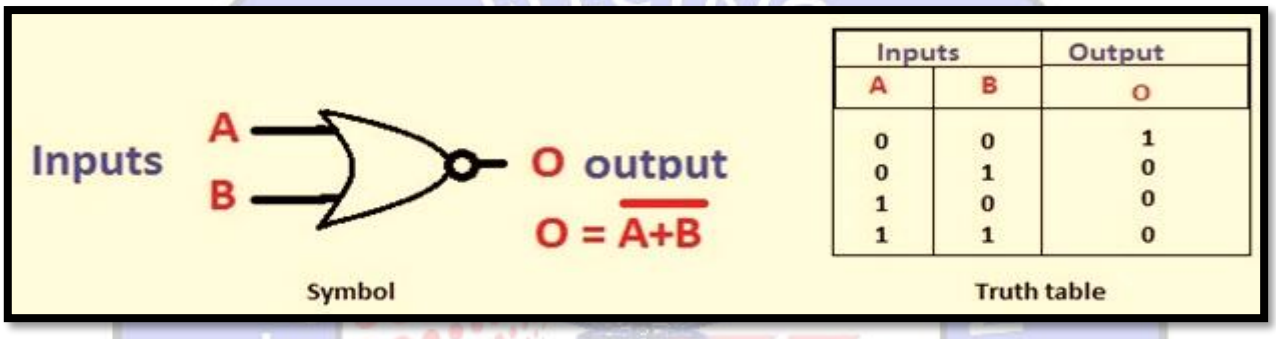
Figure 7: Transistor Inverter Circuit

The circuit operates so that when V_i = 0V, the transistor is OFF. Therefore, I_C is zero and no current flows through R_C. This means that the voltage drop across R_C is zero and the collector is at +5V above ground, producing V_0 = 5V.

When V_i = 5V, the transistor becomes ON and enters the saturation region when I_B is large enough. So, the collector voltage will be $V_{CE\,(sat)}$, and this produces $V_0 = V_{CE\,(sat)} \approx 0V$.

- **The NOR Gate Circuit**

Figure 8 shows the logic symbol for a two-input NOR gate. The operation of the NOR gate is equivalent to the OR gate followed by an inverter.

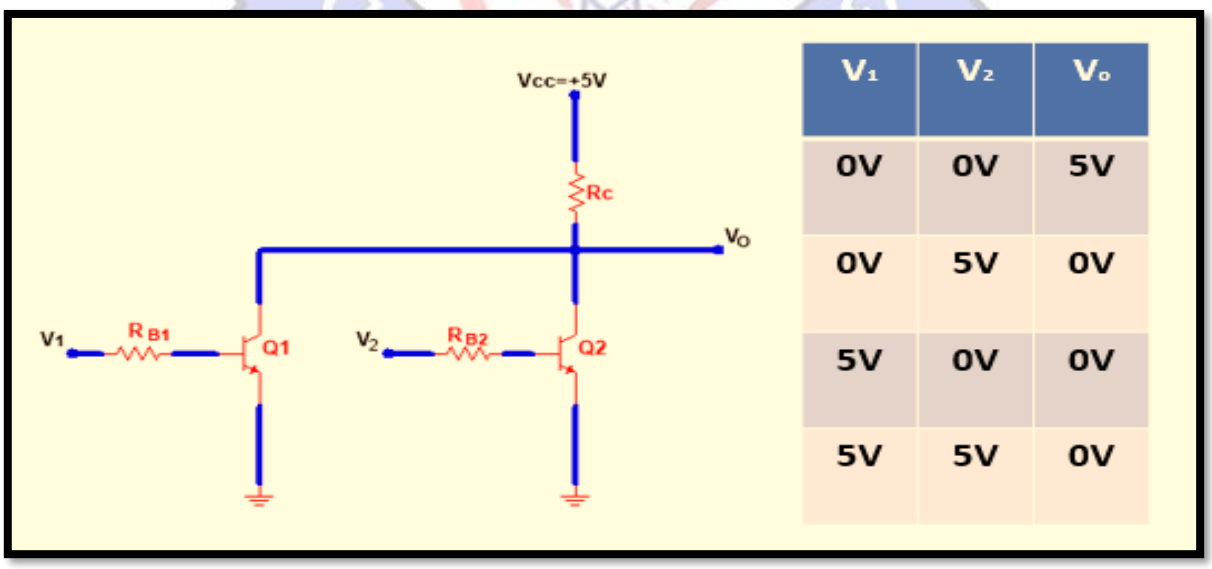


Inputs		Output
A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

Figure 8: The Logic Symbol and Truth Table for the NOR Gate

Figure 9 shows a practical electronic circuit for implementing the NOR gate. It consists of two transistors connected in parallel.



V_1	V_2	V_o
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

Figure 9: The NOR Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are in the cut-off region (OFF), and hence no current flows in resistor R_C. Therefore, the output voltage V_0 equals V_{CC} and is +5V.When $V_1=0$ and $V_2=5V$, transistor Q_1 will be OFF and transistor Q_2 will now be ON and enters the saturation

region. In this case, the current will flow in R_C through transistor Q_2. The output voltage will equal the saturation voltage of Q_2 and is approximately 0V ($V_o = V_{CE2(sat)} \approx 0V$).

When $V_1 = 5V$ and $V_2 = 0V$, the situation will be opposite to the previous case and $V_o = V_{CE2(sat)} \approx 0V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will conduct, and the output voltage will equal the saturation voltage of the transistors and hence is approximately 0V ($V_o = V_{CE\,(sat)} \approx 0V$).

- **The NAND Gate Circuit**

Figure 10 shows the logic symbol and the truth table of a two-input NAND gate. The operation of the NAND gate can be understood as being constituted from an AND gate followed by an inverter.

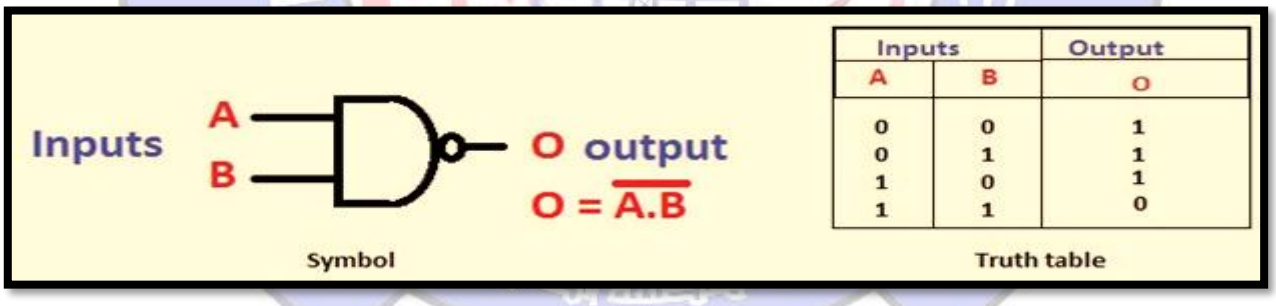
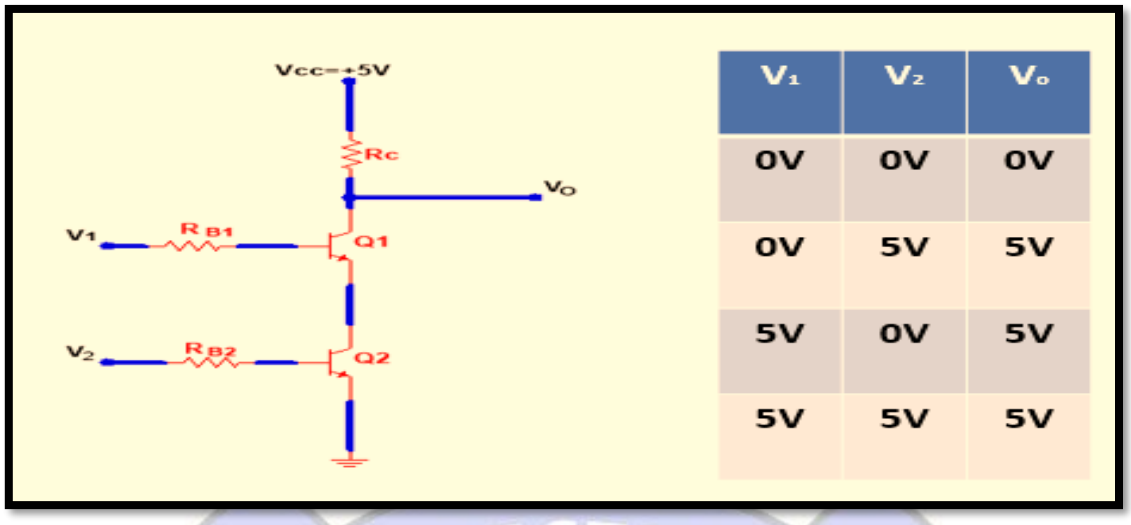


Figure 10: The Logic Symbol and Truth Table for the NAND Gate



V_1	V_2	V_o
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

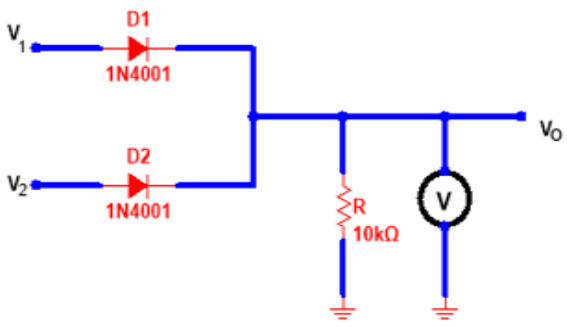
Figure 11: The NAND Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are OFF and no-current flows through RC and therefore $V_o = V_{CC} = 5V$. When $V_1=0$, and $V_2=5V$ transistor Q_2 will be ON, but Q_1 is OFF, and therefore no-current will flow through resistor R_C and V_0 is HIGH and equals 5V. In the third case, when $V_1 = 5V$, and $V_2= 0V$, transistor Q_1 becomes ON and Q_2 will be OFF and no current flows through R_C, and hence $V_0 = V_{CC} = 5V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will be ON and enter the saturation region. So, $V_0 = 2V_{sat} \approx 0V$ and will be LOW.

Procedure

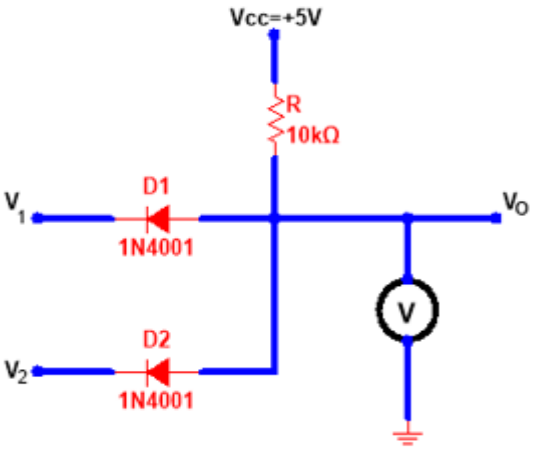
1. Connect the OR gate circuit shown in Fig.12 and verify its operation.



V_1	V_2	V_o
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 12: Practical OR Gate circuit

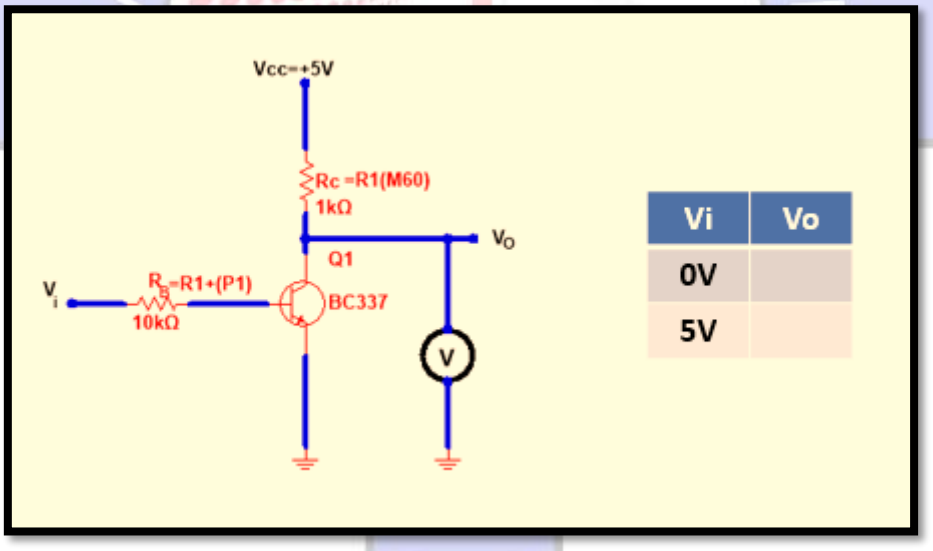
2. Connect the AND gate circuit shown in Fig.13 and verify its truth table.



V_1	V_2	V_o
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 13: Practical AND Gate Circuit

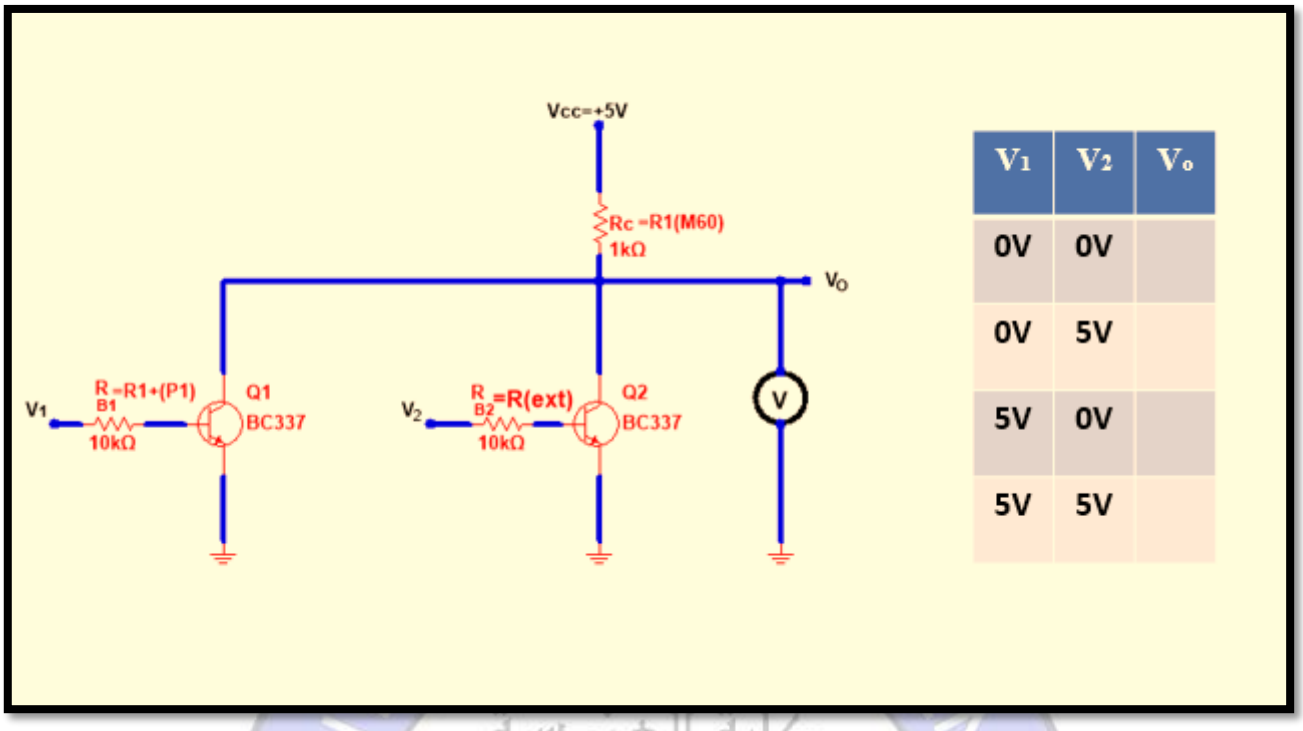
3. Connect the inverter circuit shown in Fig.14 and verify its operation. When Vi = 5V (HIGH), try to measure V_{BE} and V_{CE} of the transistor at saturation.



Vi	Vo
0V	
5V	

Figure 14: Practical Inverter Circuit

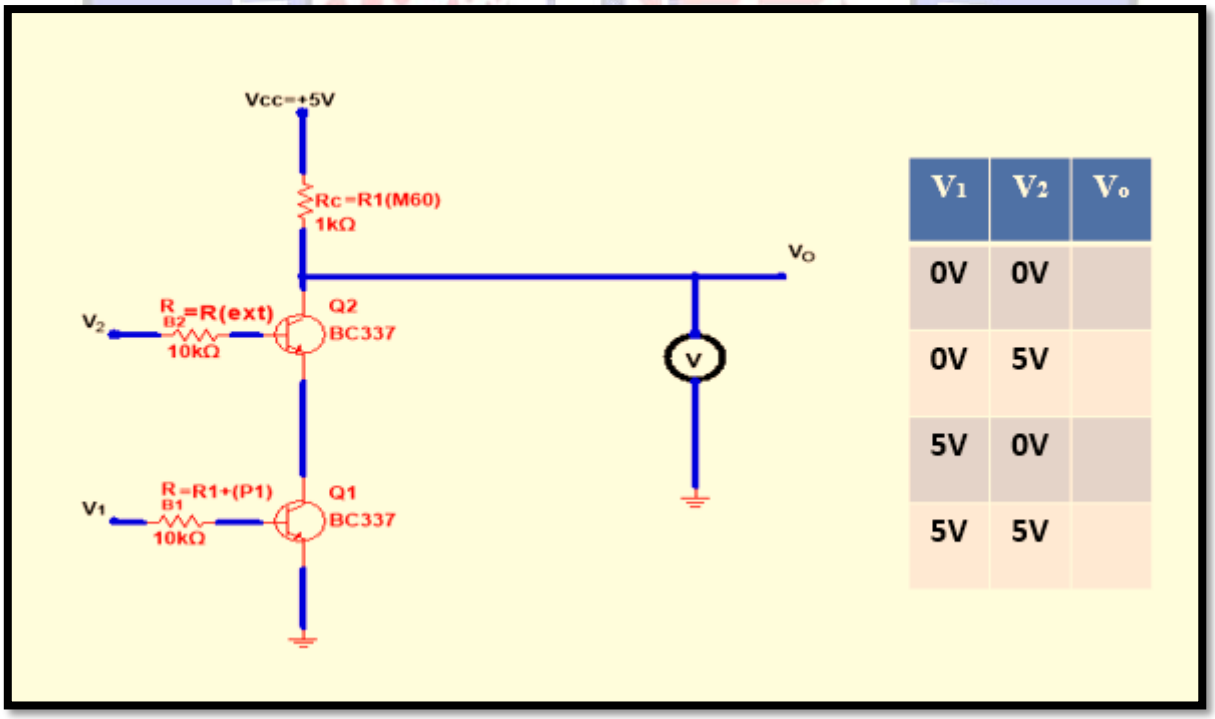
4. Connect the NOR gate circuit shown in Fig.15 and verify its truth table.



V1	V2	Vo
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 15: Practical NOR Gate Circuit

5. Connect the NAND gate circuit shown in Fig.16 and verify its truth table.

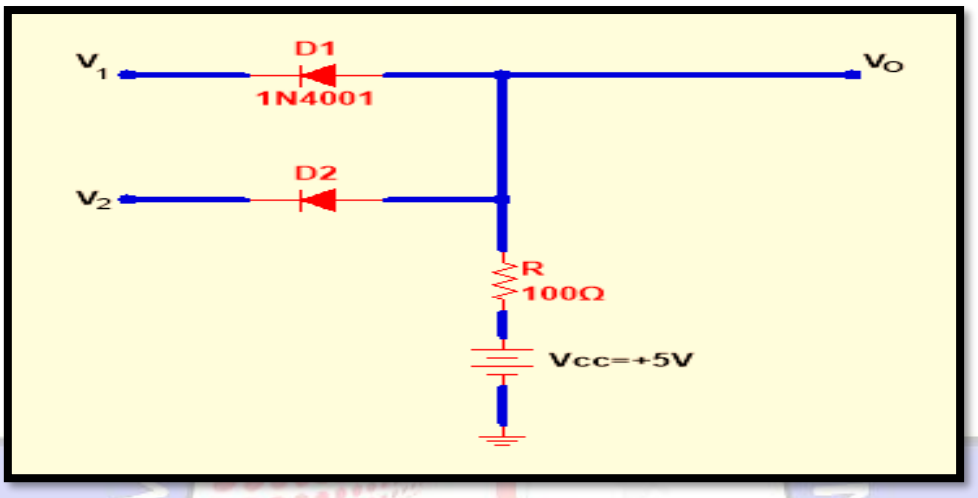


V1	V2	Vo
0V	0V	
0V	5V	
5V	0V	
5V	5V	

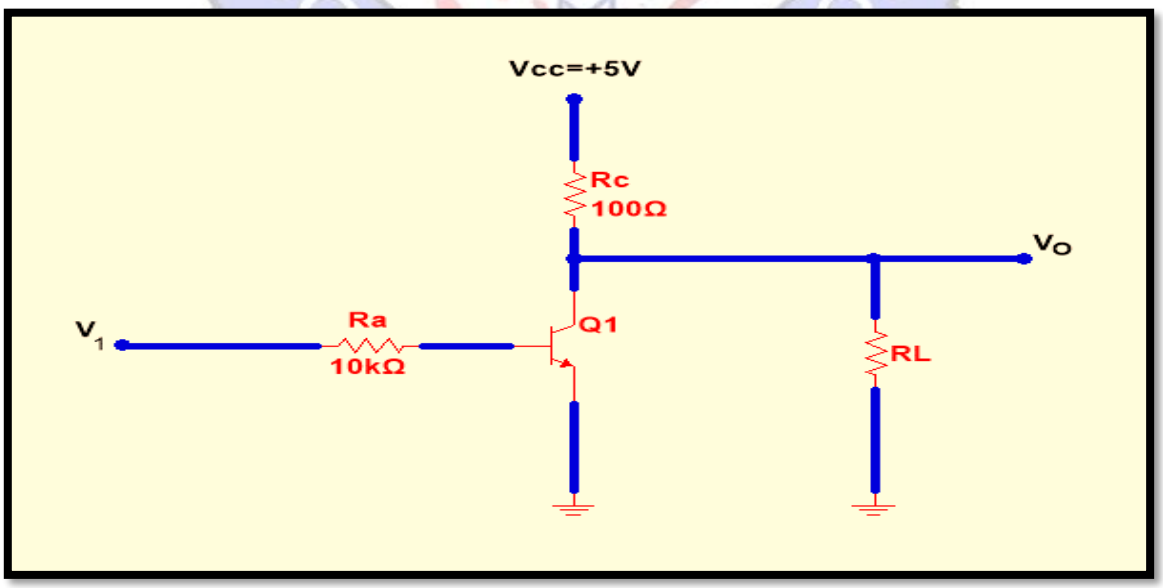
Figure 16: Practical NAND Gate Circuit

Discussion

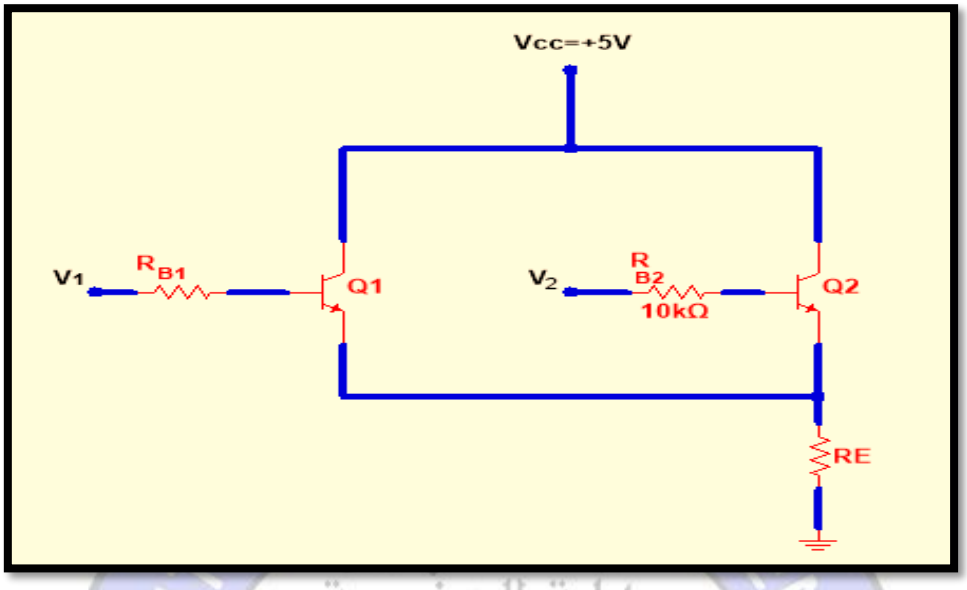
1. Determine the current flowing in each diode in the practical OR logic circuit of Fig.12 when both inputs are HIGH (5V).
2. What is the maximum current rating that each diode should have in the logic circuit shown below? Assume that the voltage drop across the silicon diode is 0.7V when it conducts.



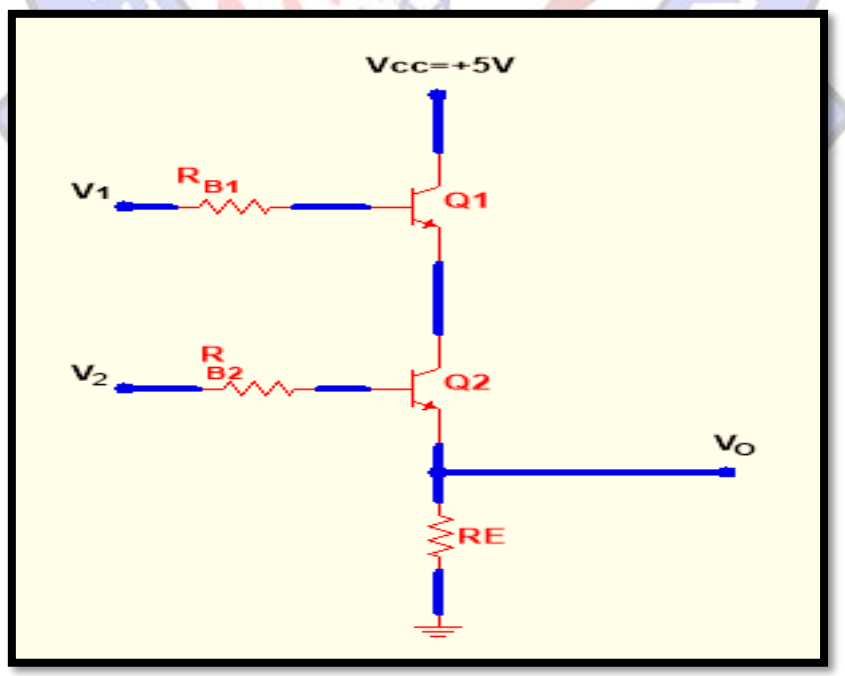
3. For the inverter circuit of Fig.14, prove that the transistor is working deeply in saturation when Vi = 5V. Assume that β = 150 for the BC107 NPN transistor.
4. In the logic circuit shown below, what is the minimum RL that the inverter can drive without causing the output to drop below 4V when Vi = 0V?



5. What is the function of the digital circuit shown below? Describe its operation briefly and find its truth table.



6. Design a NAND Gate digital circuit using an AND gate and an inverter. Describe the operation of the circuit.
7. Design a NOR gate circuit using an OR gate circuit and an inverter. Describe briefly the operation of the circuit.
8. Determine the truth table of the digital circuit shown in the figure below and explain its operation.



University of Anbar
College of Engineering
Dept. of Electrical Engineering

Lab. Name: Electronic I
Experiment no.: 4
Lab. Supervisor: Munther N. Thiyab

Experiment No.4

Small Signal BJT Amplifier

Object

The purpose of this experiment is to demonstrate the operation of the small signal common emitter amplifier and investigate the factors influencing the voltage gain as well as to determine the input and output impedances.

Required Parts and Equipment's

1. Electronic Test Board. (M100)
2. Function Generator
3. DC Power Supply.
4. Two-channel Oscilloscope
5. DC Multimeter
6. BC 337 NPN silicon Transistors.
7. Resistors R_L=10KΩ, R_2=4.7KΩ, R_3=39KΩ, R_C= R_5=3.3KΩ, R_{test}=(P_2) P_2=R_{E2}=1KΩ, R_{E1}=R_4=470Ω,120Ω
8. Capacitors 2.2 µF and 10 µF.C_1=100nf, C_2=C_E=1µf, C_3=100nf

Theory

The common-emitter amplifier is characterized by the application of the input signal to the base lead of the transistor while taking the output from the collector, which always gives 180^o phase shift between the input and output signals. Figure 1 presents a schematic diagram for a typical common-emitter amplifier using the voltage-divider bias configuration.

The DC coupling capacitors C_{in} and C_{out} are used to block the DC current and thus to prevent the source internal resistance and the load resistance R_L from changing the DC bias voltages at the base and collector. Capacitor C_E is a bypass capacitor for the emitter resistor R_E. Resistor R_{E2} is used for bias stability, while R_E is used to minimize the change in the emitter internal AC resistance *re* due to temperature effects, and thereby to obtain a stable voltage gain.

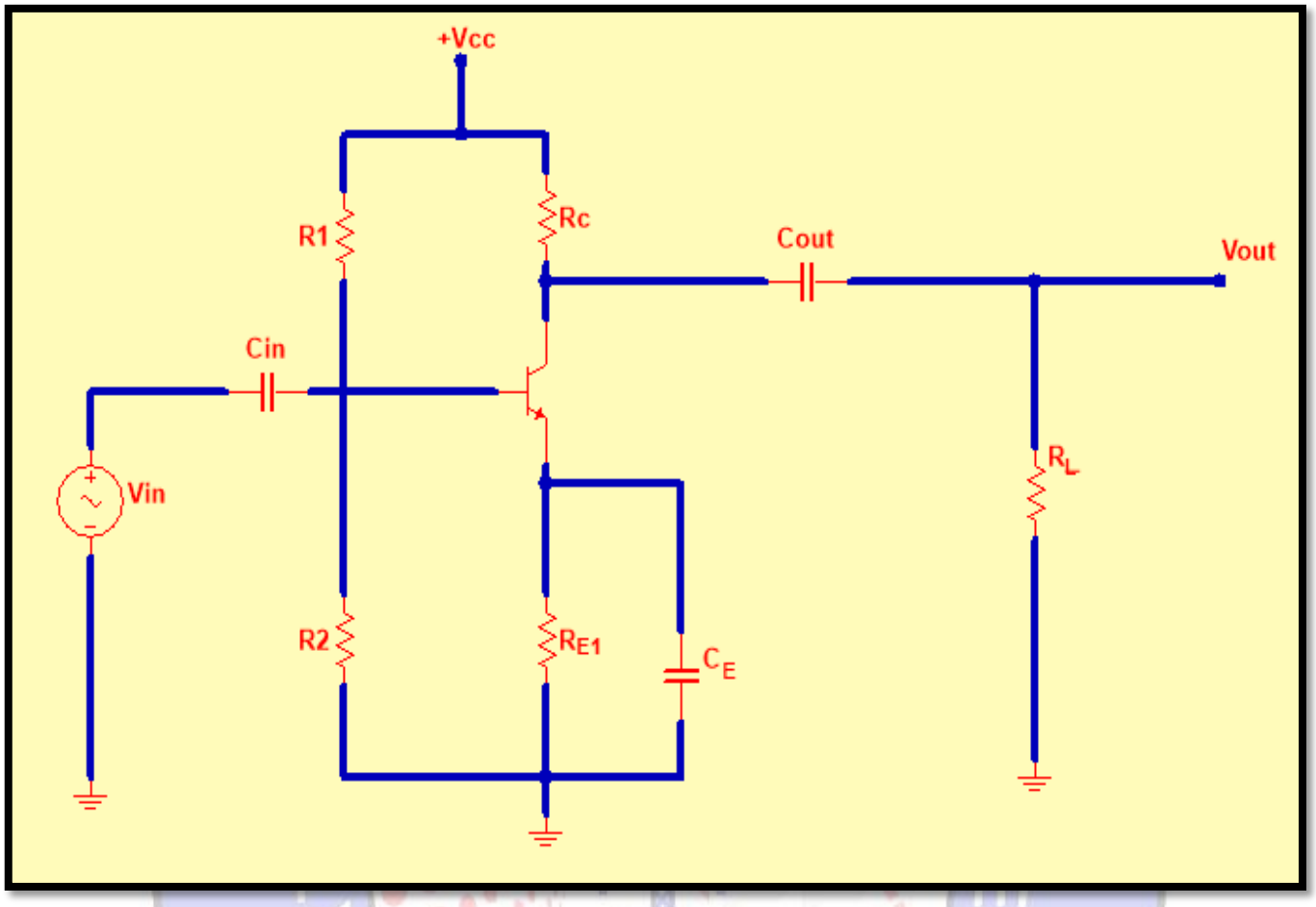


Figure 1: Schematic Diagram for a Typical Common Emitter Amplifier Circuit

The base DC voltage can be calculated approximately from the following equation assuming that β. (R_{E1}) >> R_2:

$$V_B = \frac{R_2 + V_{CC}}{R_1 + R_2} \quad (1)$$

The emitter DC voltage is therefore:

$$V_E = V_B - V_{BE} \quad (2)$$

The emitter DC bias current can be obtained as:

$$I_{EQ} = \frac{V_E}{R_E} \cong I_{CQ} \quad (3)$$

Transistor AC emitter resistance is obtained from:

$$r_e = \frac{V_R}{I_{EQ}} \quad (4)$$

Where V_T = 26 mV at room temperature.

The quiescent DC collector-emitter voltage is calculated from:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) \quad (5)$$

- **Voltage Gain Analysis**

Figure 2 presents the AC small-signal equivalent circuit for the common emitter amplifier. From this circuit, the amplifier voltage gain can be found as:

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{R_C \| R_L}{R_E + r_e} \quad (6)$$

If the load resistor R_L is removed then the voltage gain will become:

$$A_v = -\frac{R_C}{R_E + r_e} \quad (7)$$

On the other hand, if the bypass capacitor C_E is removed, then the voltage gain will be modified as:

$$A_v = -\frac{R_C \| R_L}{R_E + r_e} \quad (8)$$

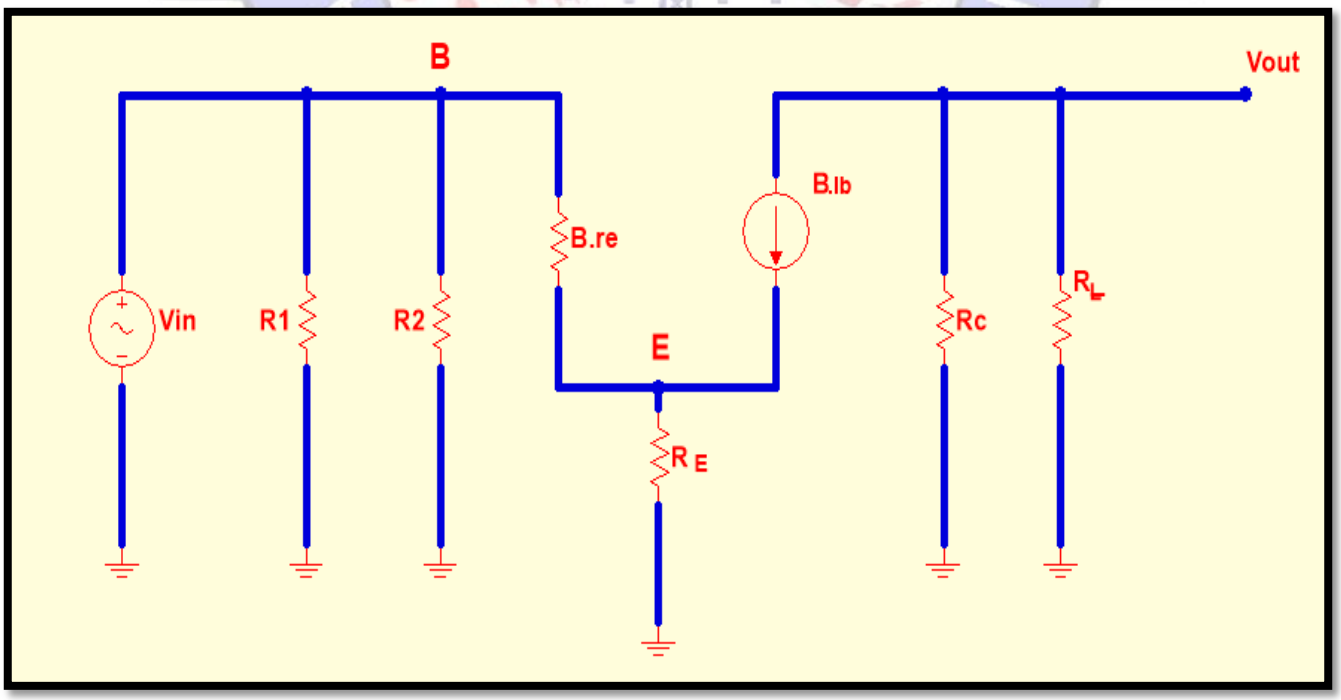


Figure 2: The Small-Signal AC Equivalent Circuit for the Common Emitter Amplifier

- **AC Load Line and Maximum Symmetrical Swing**

The AC load line of the amplifier circuit can be sketched to predict the swing of the output voltage and collector current. Figure 2 shows the AC and DC load lines of the circuit.

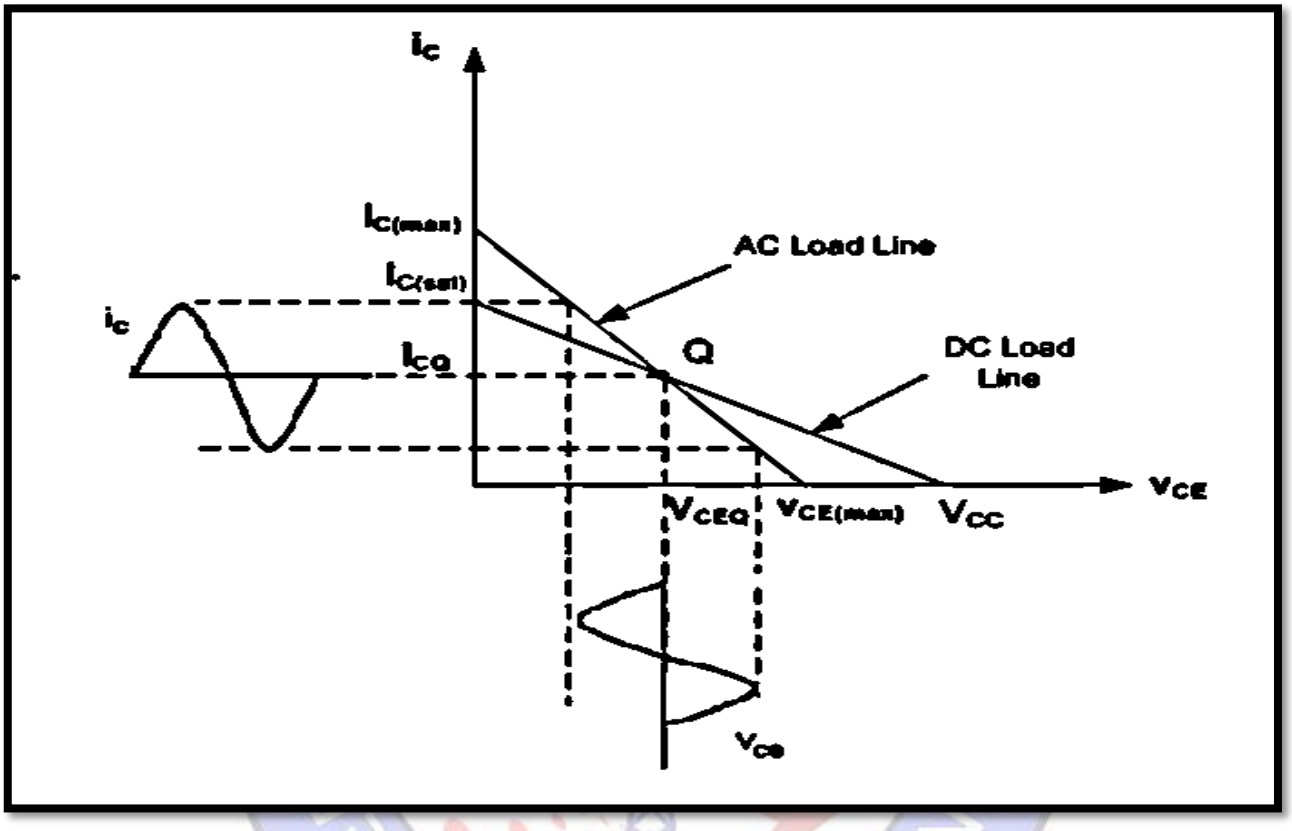


Figure 3: DC and AC Load Lines and Collector Current and Voltage Swing

As shown in Fig.2, both load lines intersect at the Q-point of the transistor. The slope of the AC load line is equal to $-1/R_{ac}$, where R_{ac} is the AC equivalent resistance seen between the collector and emitter terminals. R_{ac} can be obtained from the amplifier's small signal equivalent circuit of Fig.2. The total collector current and voltage can be expressed as the sum of the quiescent values and the AC signal quantities as shown below:

$$i_C = I_{CQ} + i_c \quad (9)$$

$$v_{ce} = V_{CEQ} + v_{ce} \quad (10)$$

It can be shown that $i_{C(max)}$ and $v_{CE(max)}$ in Fig.3 are given by:

$$i_{C(\max)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \quad (11)$$

$$v_{CE(\max)} = V_{CEQ} + I_{CQ}.R_{ac} \quad (12)$$

Where:

$$R_{ac} = R_E + R_C \parallel R_L \quad (13)$$

Maximum symmetrical swing in the output signal can be obtained if the Q-point bisects the AC load line. The AC load line concept can be used to predict the maximum amplitude in the output signal before clipping.

- **Input and Output Impedances**

The input and output impedances of the amplifier can be found theoretically as the Thevenin equivalent impedances at the input and output terminals respectively. For the equivalent circuit of Fig.2, the input impedance (Z_{in}) of the amplifier seen by the source is:

$$Z_{in} = R_1 \parallel R_2 \parallel \beta(r_e + R_E) \quad (14)$$

Similarly, the output impedance (Z_{out}) seen from the output terminals is:

$$Z_{out} = R_C$$

The amplifier circuit can be represented as a two-port network as illustrated in Fig.4. In this figure, A_{vo} represents the no-load voltage gain of the amplifier, Z_{in} is the amplifier's input impedance, and Z_{out} is the amplifier's output impedance. Resistor R_S is the internal resistance of the signal source, while R_L is the load resistance.

The overall voltage gains of the amplifier taking the effects of R_S and R_L into account can be expressed as:

$$A_v = \frac{v_{in}}{v_s}.\frac{v_{out}}{v_{in}}$$

$$A_v = \frac{Z_{in}}{Z_{in}+R_S}.\frac{A_{vo}.R_L}{R_L+Z_{out}} \quad (16)$$

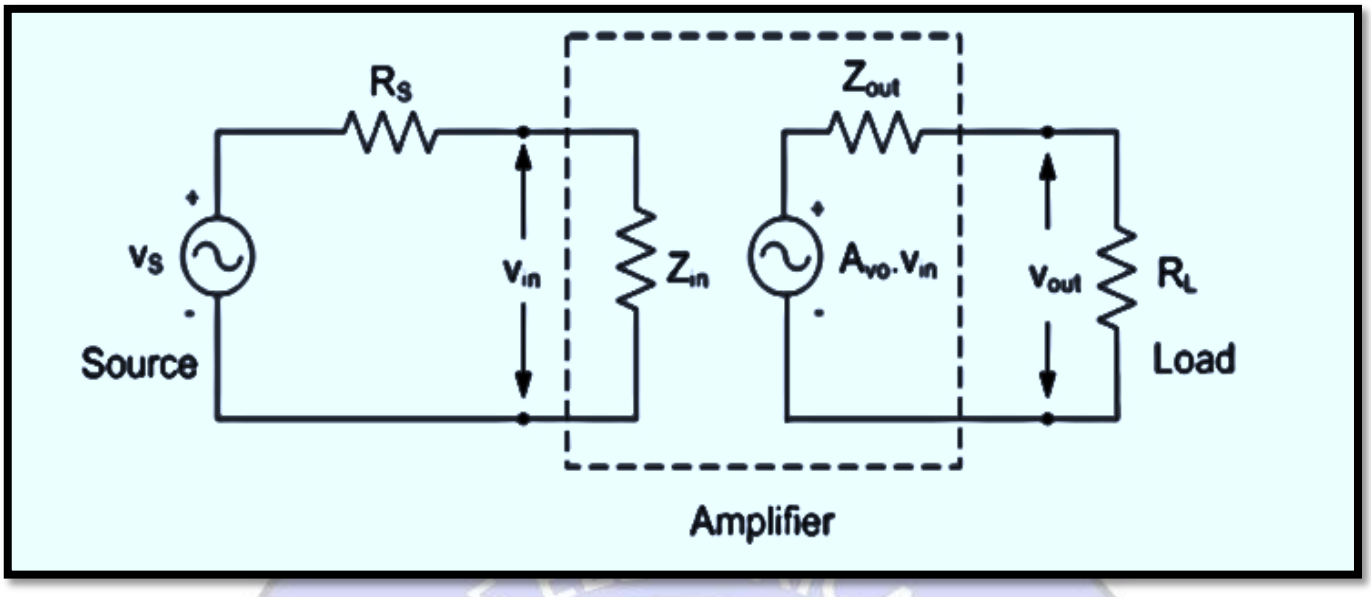


Figure 4: The Amplifier as a Two-Port Network

For the input port, when $R_S = Z_{in}$, we have:

$$v_{in} = \frac{Z_{in}}{Z_{in}+R_S} v_s = \frac{1}{2} v_s$$

Assuming that the amplifier is connected with no-load, we have:

$$A_v = \frac{v_{in}}{v_s} . \frac{v_{out}}{v_{in}} = \frac{1}{2} A_{vo}$$

Thus, the input impedance can be estimated practically by inserting a variable source resistor R_S in series with the source and varying it until the voltage gain of the amplifier equals half the no-load gain A_{vo}. This value of R_S represents the input impedance Z_{in}.

For the output port, when RL = Zout, and assuming that RS = 0, then we have:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{A_{vo}.R_L}{R_L + Z_{out}} = \frac{1}{2} A_{vo}$$

So that the output impedance can be estimated practically by connecting a variable load resistor R_L and varying it until the voltage gain becomes equal to half the value of the no-load gain with $R_S = 0$. This value of R_L represents the output impedance Z_{out}.

Procedure

1. Connect the circuit shown in Fig.5 and measure the DC voltages V_B, V_E, and V_C. Try to measure the DC current gain of the BC337 transistor h_{FE} using a multi-meter. Tabulate your results as illustrated in Table-1.

Table-1: Measured Quantities for the DC Bias Circuit

Parameter	β	V_B	V_E	V_C	I_{CQ}	V_{CEQ}	V_{BEQ}	r_e
Value								

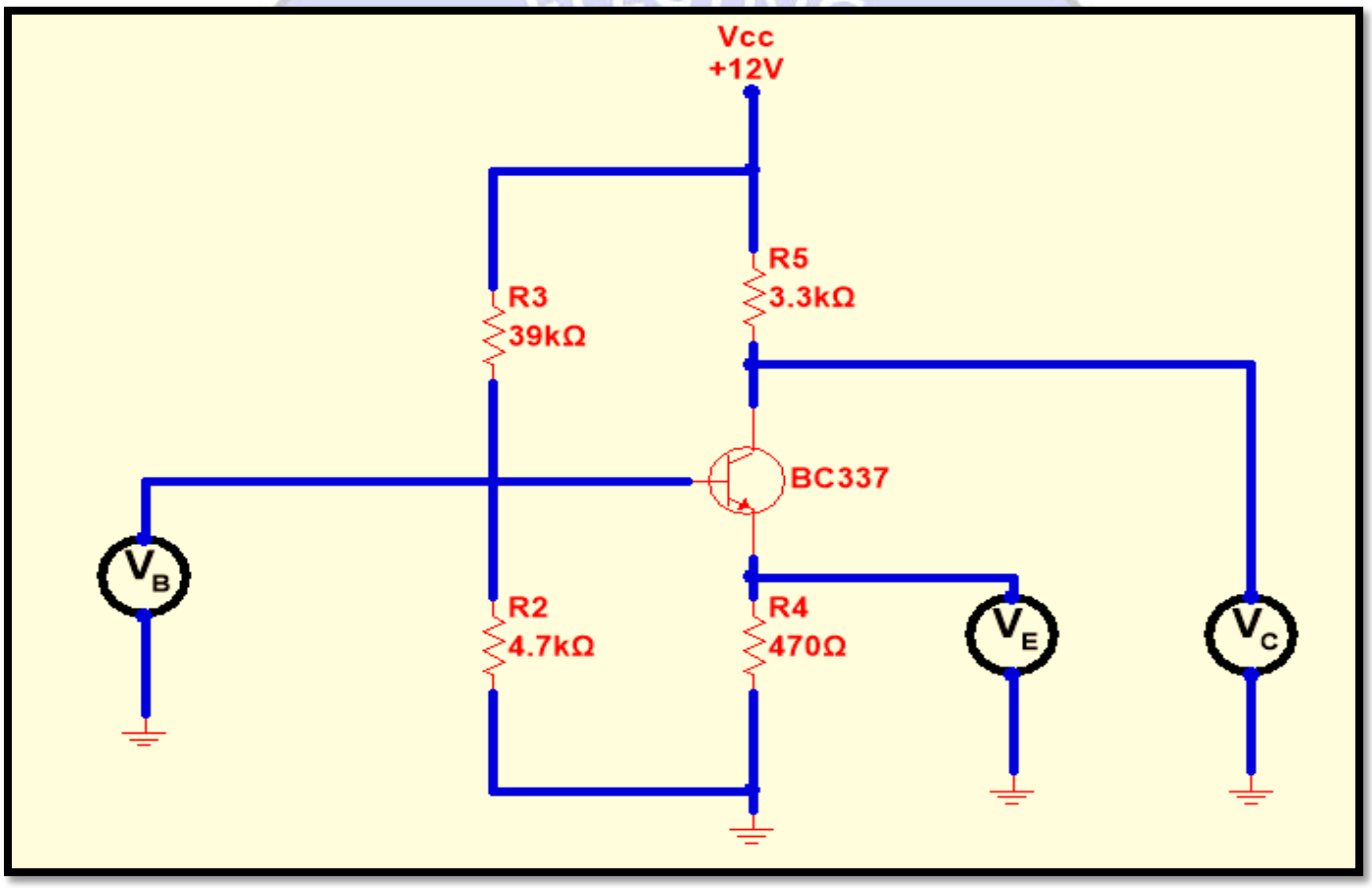


Figure 5: The DC Bias Circuit of the Common Emitter Amplifier

2. Connect the amplifier circuit shown in Fig.6, and apply a sinusoidal source signal with peak amplitude of 0.1V and frequency of 10 KHz. Display both the input (source) and output (load) signals on the oscilloscope. Try to measure the voltage gain Av, where Av = Vout/Vs.

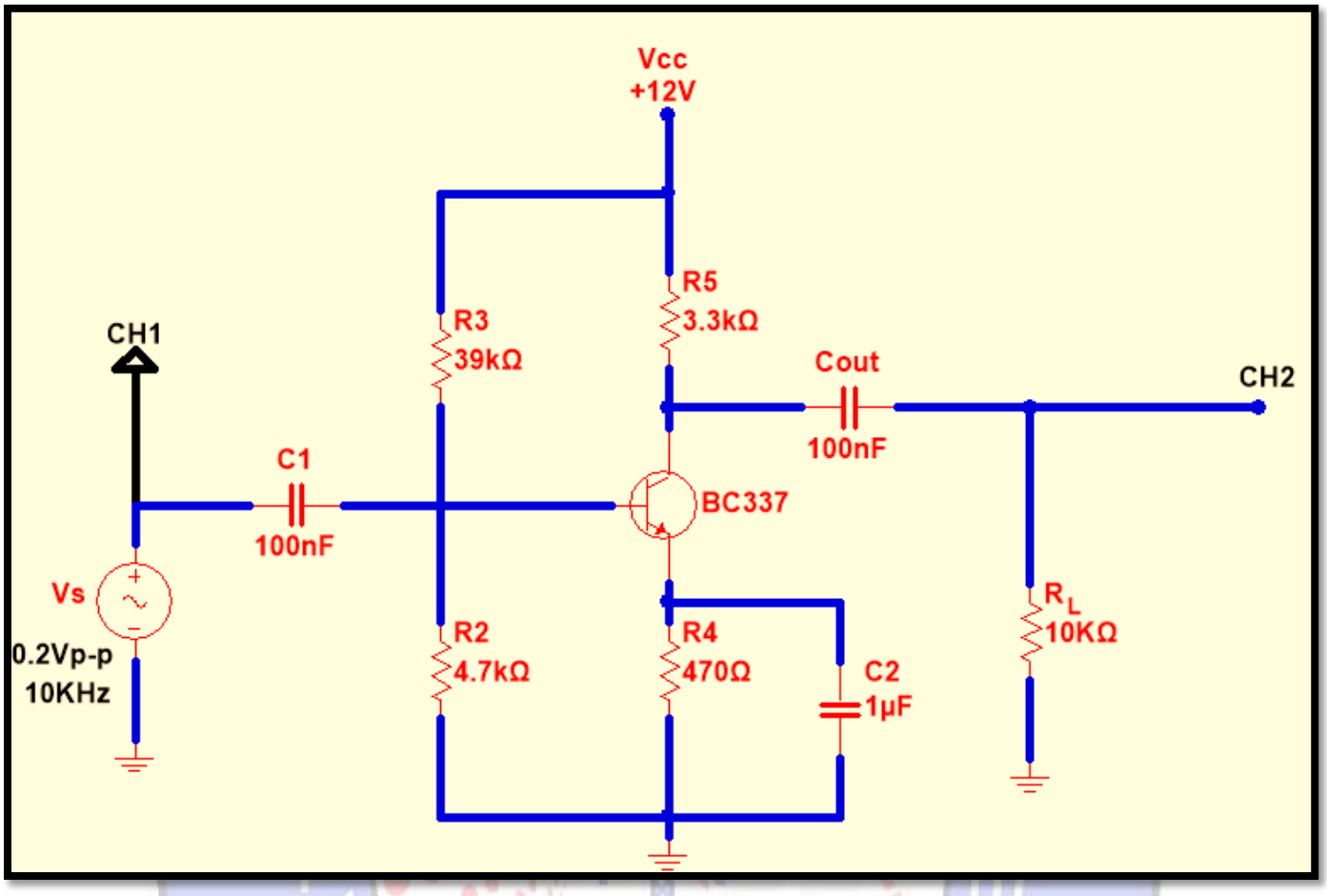


Figure 6: The Practical Common Emitter Amplifier Circuit

3. Remove load resistor R_L and r_e-measure the voltage gain.
4. Remove the bypass capacitor C_E and measure the voltage gain with the load resistor R_L connected at the output. Tabulate your results as shown in Table-2.

Table-2: Voltage Gain for Different Cases

Case	Voltage Gain
Normal (R_L=10KΩ)	
No-Load ($R_L = \infty$)	
No Bypass Capacitor	

5. Increase the amplitude of the source input signal gradually until clipping occurs in the output signal. Find the maximum peak amplitude for v_{out} and vs at the edge of clipping for the three cases illustrated in Table-3.

Table-3: Peak Input and Output Voltages before Clipping

Case	$V_{s(max)}$	$V_{out(max)}$
Normal		
No-Load		
No Bypass Capacitor		

6. Connect the circuit shown in Fig.7, where R_{test} is a variable resistor box. This circuit is used to measure the input impedance of the amplifier.

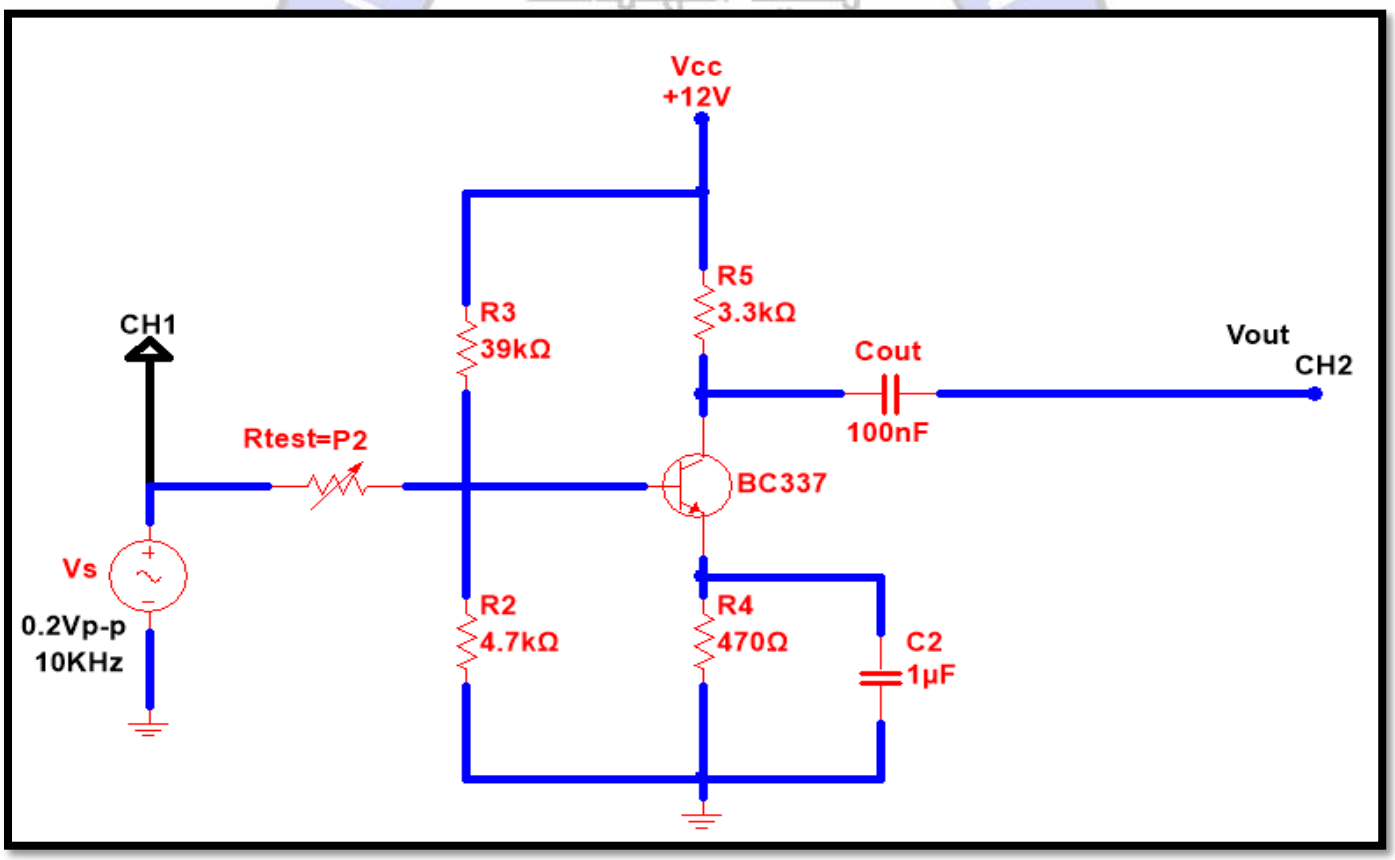


Figure 7: Test Circuit to Measure the Input Impedance of the Amplifier

7. Set R_{test} = 0 Ω initially, and measure the no-load voltage gain A_{vo}.
8. Increase R_{test} in steps until the voltage gain becomes equal to half the no-load gain. Record this value of R_{test} as Z_{in}.
9. Connect the circuit shown in Fig.8 to measure the output impedance of the amplifier. Resistor R_{test} is inserted at the output terminals instead of R_L.

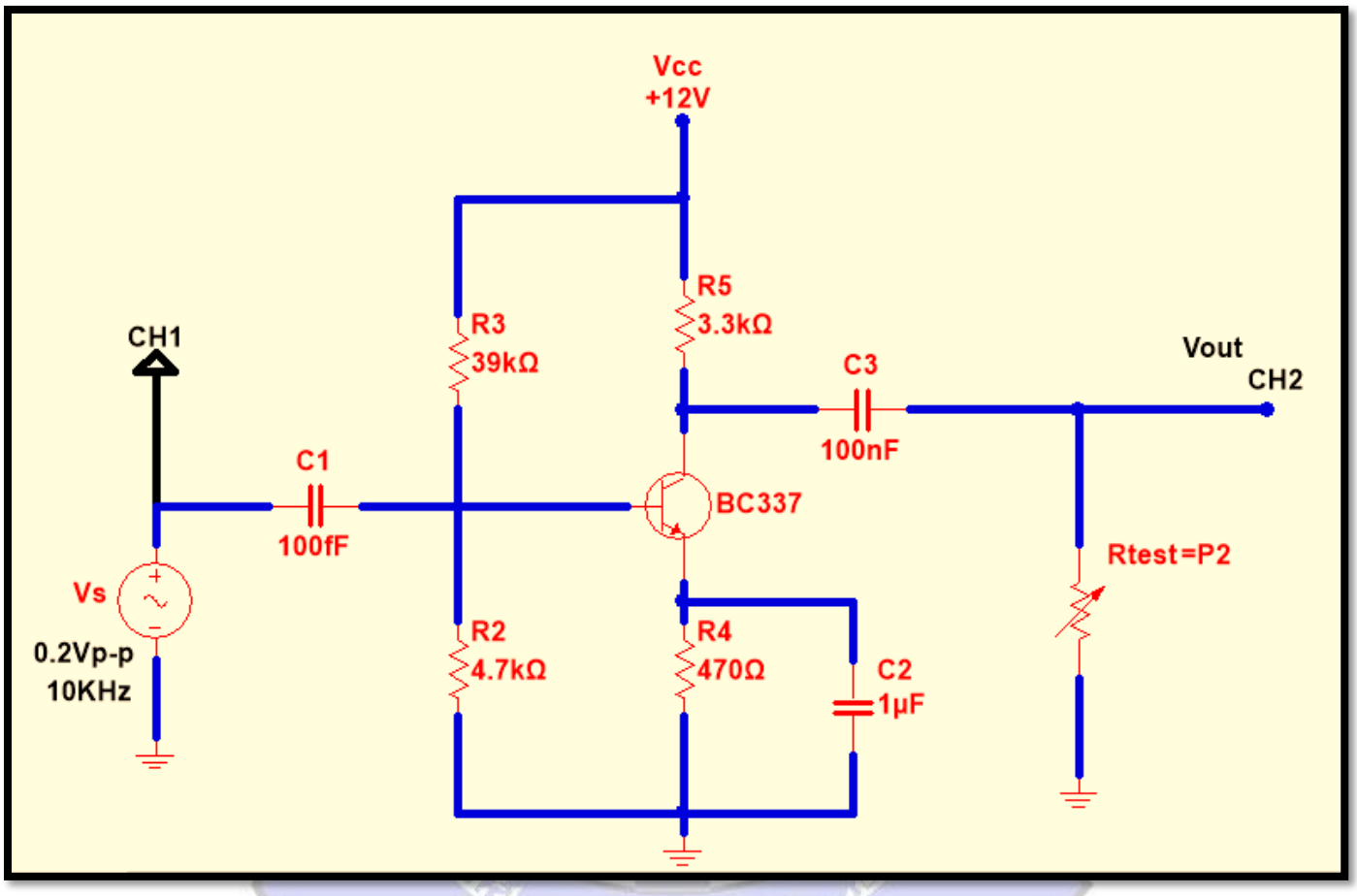


Figure 8: Test Circuit for Measuring the Output Impedance of the Amplifier

10. Vary R_{test} in steps until the voltage gain becomes equal to half the no-load gain. Record this value of R_{test} as Z_{out}.

Discussion

1. Calculate the theoretical DC voltages and currents for the transistor bias circuit and compare them with the practically measured values.
2. Calculate the theoretical values of the voltage gain for the three cases and compare them with the measured quantities.
3. Sketch the AC load line for the amplifier circuit and find the theoretical maximum symmetrical swing in collector voltage v_{ce} before clipping when R_L = 10 KΩ. Determine $V_{out(max)}$ before clipping and compare it with the measured value.
4. Determine the theoretical value of the input impedance and compare it with the measured value.
5. Calculate the theoretical value of the output impedance and compare it with the measured value.
6. If resistor R_2 is opened (or removed) in the circuit of Fig.5, what is its effect on the transistor circuit? Determine the collector current I_C and voltage V_{CE} in this case.
7. Calculate the current gain A_i of the amplifier circuit of Fig.6.

Experiment No.5

JFET Characteristics

Object

The purpose of this experiment is to determine and sketch the characteristics of the JFET and to find its parameters.

Required Parts and Equipment's

1. Electronic Test Board. (M100)
2. Dual Polarity Variable DC Power Supply
3. Digital Multimeters.
4. N-Channel JFET 2N3823/3824
5. Resistors 207KΩ, 220 Ω.

Theory

The Junction Field Effect Transistor (JFET) is a three-terminal device with one terminal (called the gate) capable of controlling the current between the other two terminals (drain and source). The primary difference between FET and BJT transistors is the fact that the BJT transistor is a current-controlled device, while the JFET transistor is a voltage-controlled device. The FET transistor is a unipolar device depending on either electron conduction (N-channel JFET) or hole conduction (P-channel JFET). In contrast, the BJT transistor is a bipolar device, meaning that the conduction depends on two charge carriers (electrons and holes) in the same time.

Another difference between two devices is the high input impedance of the JFET when compared with the BJT. The input impedance is usually larger than 1 MΩ. However, typical AC voltage gains for BJT amplifiers are greater than those for FET amplifiers. Furthermore, FETs are more temperature stable than BJTs and are usually smaller in size, making them particularly useful in integrated circuit chips.

The basic construction of an N-channel JFET is shown in Fig.1 together with its symbol.

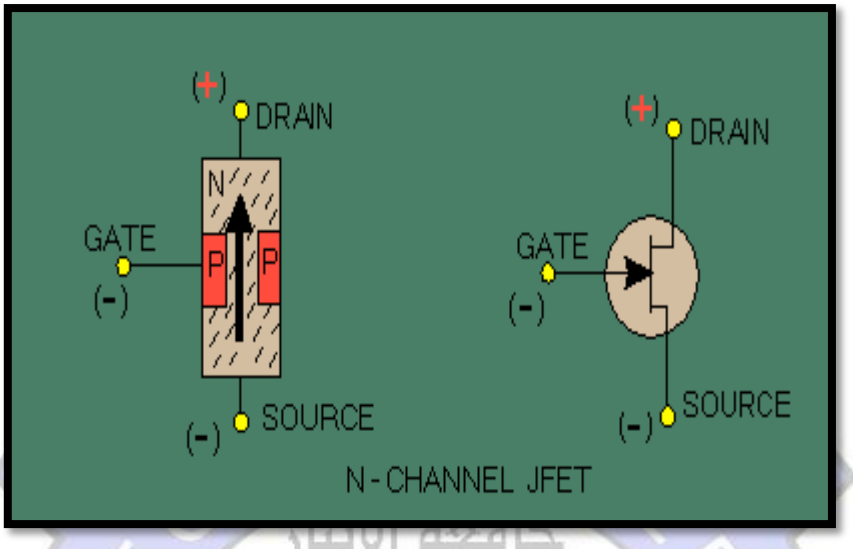


Figure 1: N-Channel JFET Structure and Symbol

The drain current (I_D) of the JFET is controlled by the application of reverse-biased voltage between gate and source terminals (V_{GS}). The relationship between I_D and V_{GS} is defined by the well-known Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....(1)}$$

Where V_P is called the pinch-off voltage and I_{DSS} is known as the drain saturation current. When $V_{GS} = V_P$ then $I_D = 0$, and the FET is in the cut-off region. Equation (1) indicates that the FET is a square-law device.

The relation between I_D and V_{GS} is also referred as the transfer characteristic of the JFET and is presented in Fig.2. This curve is obtained by varying the negative voltage V_{GS} between V_P and 0 and measuring I_D for a given value of the drain to source voltage (V_{DS}). Equation (1) can approximate this curve to an acceptable level.

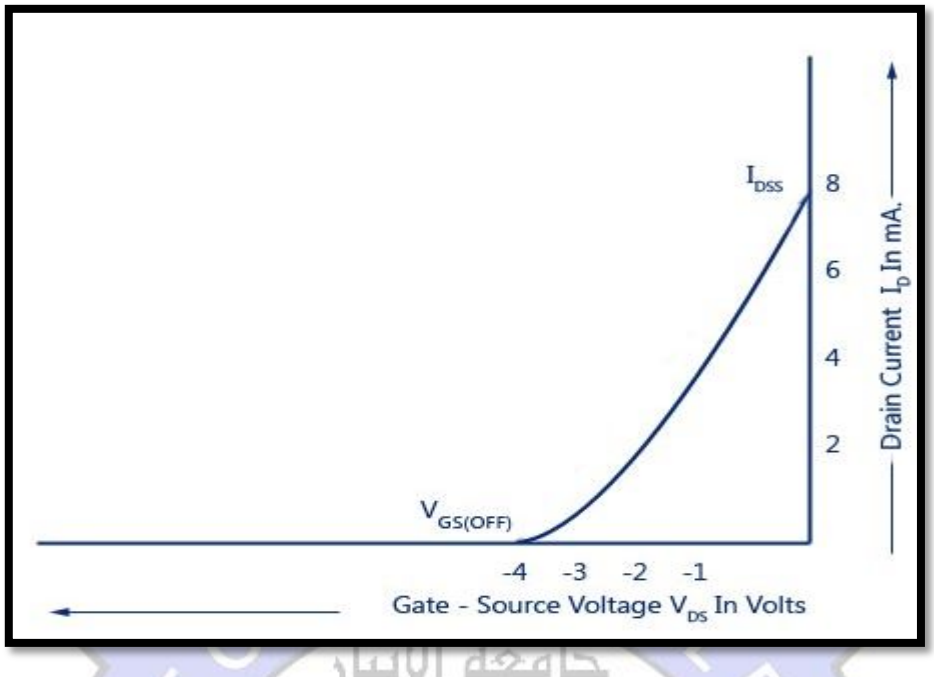


Figure 2: The Transfer Characteristics of the JFET

The circuit used to obtain the JFET characteristics is shown in Fig.3. To obtain the transfer characteristic, the drain supply voltage V_{DD} should be maintained at a certain value, and the gate supply voltage is adjusted to several negative values while recording I_D in each step.

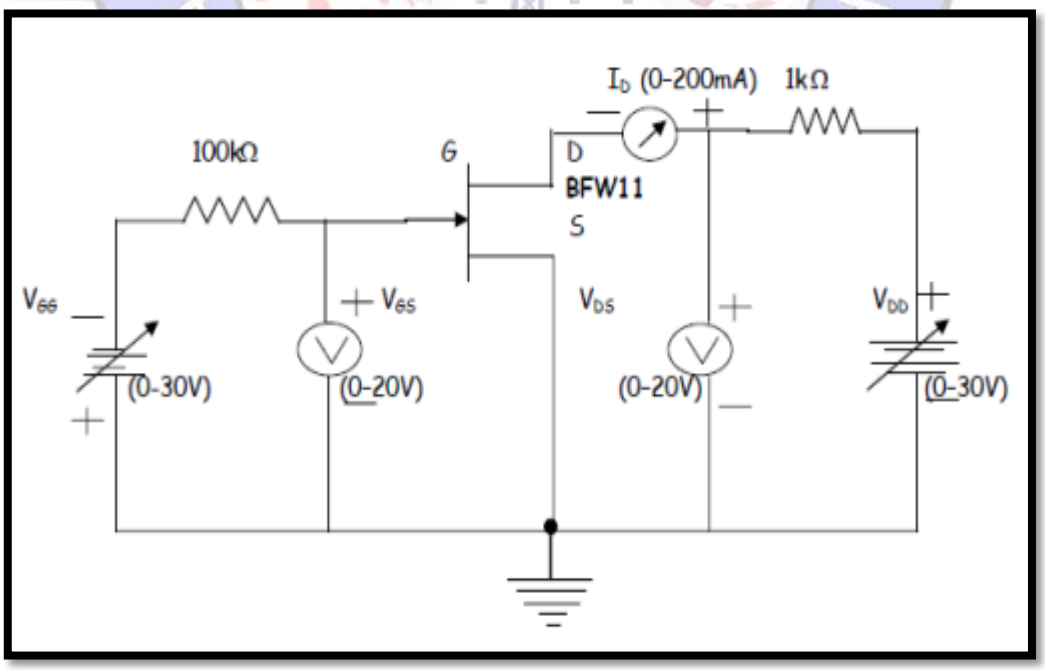
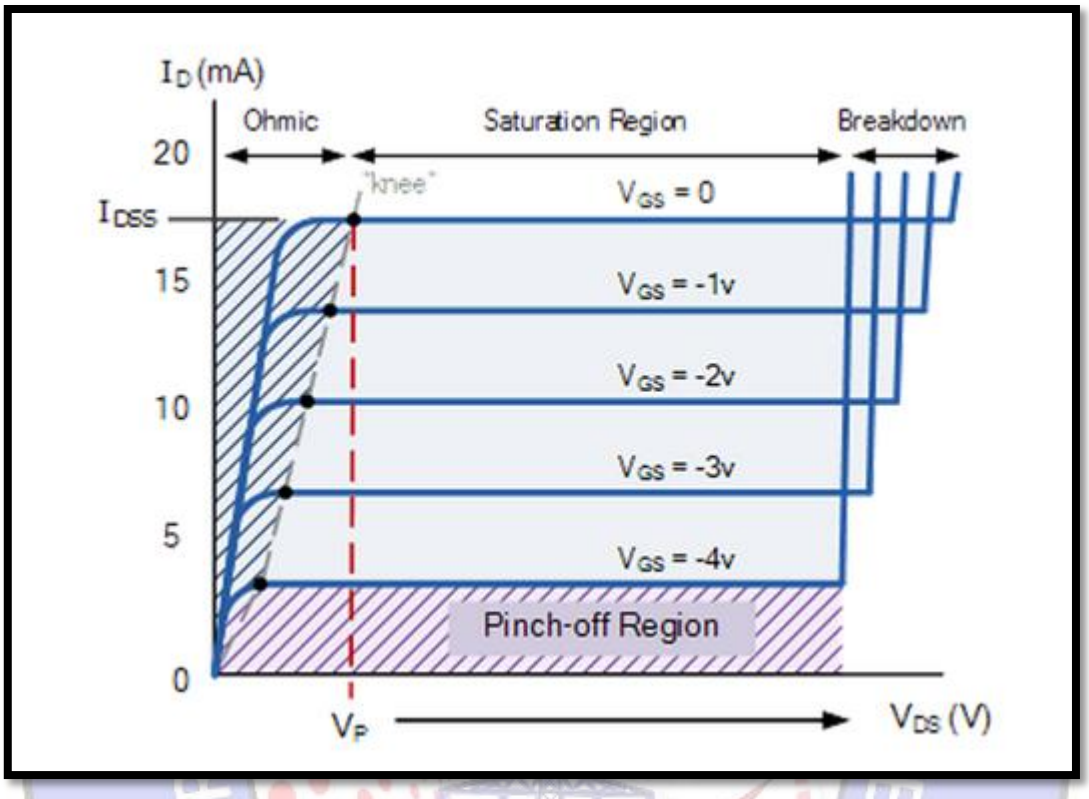


Figure 3: A Test Circuit for Getting JFET Characteristics

On the other hand, to sketch the drain characteristic, the gate-source voltage V_{GS} must be kept at a certain level while varying V_{DS} in several steps and recording I_D in each step. Figure 4 shows the drain (or output) characteristics of the JFET.



As shown from Fig.4, for small values of V_{DS} ($V_{DS} < |V_P|$) the drain current increases linearly with V_{DS}. This region is called the linear or Ohmic region in which the JFET behaves as a voltage-controlled resistor. For larger values of V_{DS} ($V_{DS} > |V_P|$), the drain current (I_D) is approximately constant and enters the saturation region.

The transconductance of the JFET (g_m) is defined as the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage (V_{DS}) kept constant. It has the unit of siemens (S).

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{.....(2)}$$

Because the transfer characteristic curve for a JFET is nonlinear, gm varies in value depending on the location on the curve as depicted in Fig.5. A datasheet normally gives the value of g_m measured at $V_{GS} = 0$, which is referred as g_{mo}.

Theoretically, g_m can be calculated at any point on the transfer characteristic curve from the following equation:

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{.....(3)}$$

Where g_{mo} is found from:

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \quad \text{.....(4)}$$

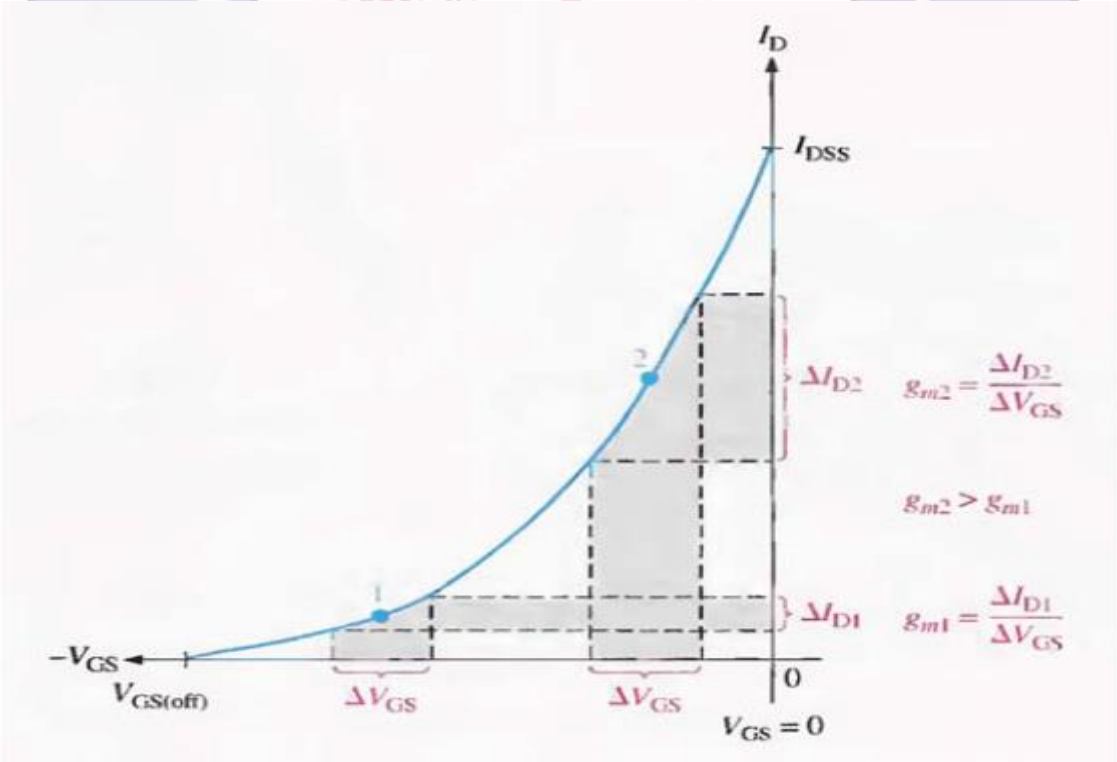


Figure 5: Graphical Determination of the JFET Transconductance

Procedure

1. Connect the circuit shown in Fig.6.

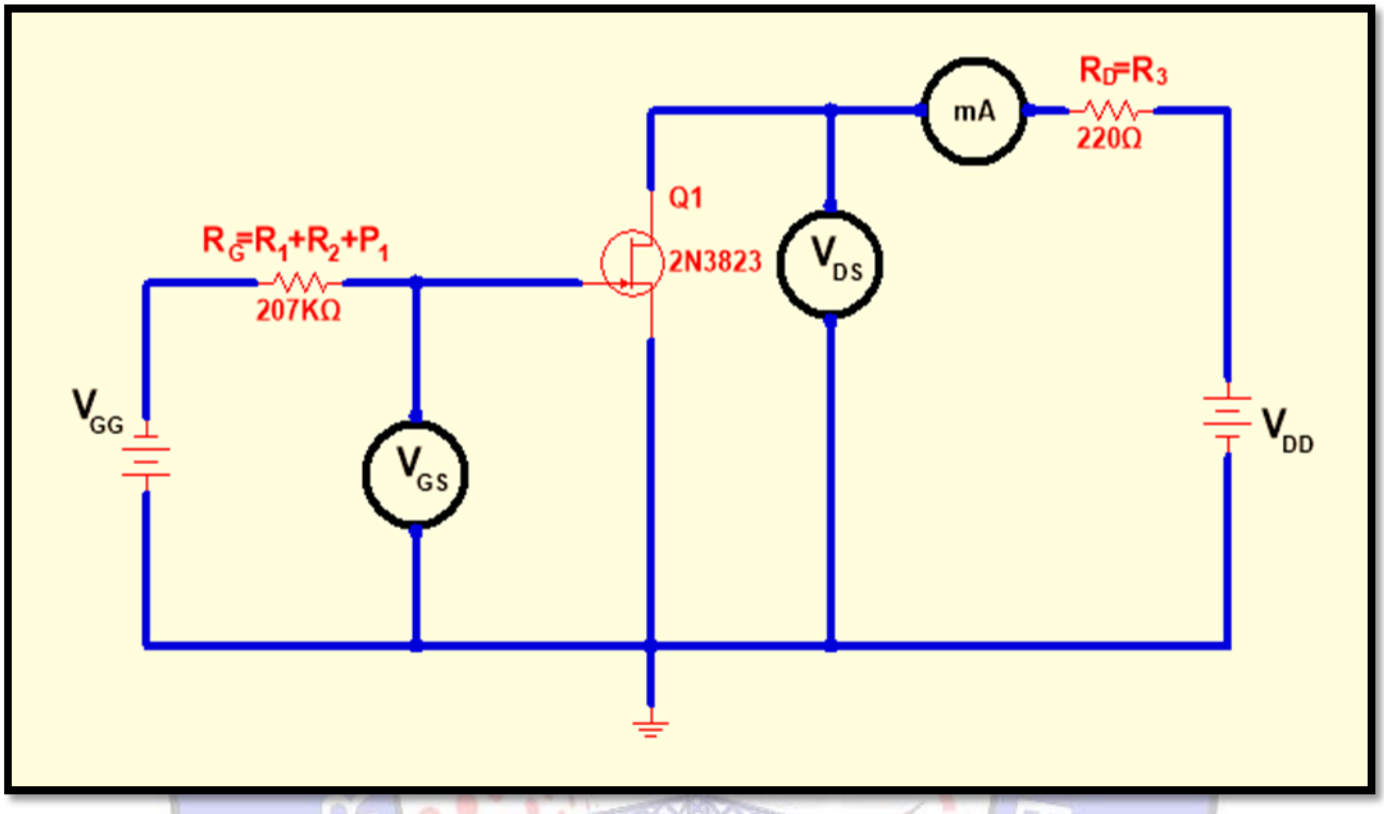


Figure 6: The Test Circuit for Getting JFET Characteristics

2. Adjust V_{DD} so that V_{DS} = 5V, and vary V_{GG} to change V_{GS} from 0V to -3V in different steps recording I_D for each step. Repeat with V_{DS} = 10V. Tabulate your results as shown in Table-1.
3. Set V_{GG} to 0V so that V_{GS} = 0V and vary V_{DD} so that V_{DS} changes in several steps recording I_D in each step. Repeat with V_{GS} = -1V. Tabulate your results as illustrated in Table 2.

Table 1: Recorded Data for the JFET Transfer Characteristics

VDS = 5V		VDS = 10V	
VGS(V)	ID (mA)	VGS(V)	ID (mA)
0		0	
-0.25		-0.25	
-0.5		-0.5	
-0.75		-0.75	
-1		-1	
-1.25		-1.25	
-1.5		-1.5	
-1.75		-1.75	
-2		-2	
-2.25		-2.25	
-2.5		-2.5	
-2.75		-2.75	
-3		-3	

Table 2: Recorded Data for the JFET Drain Characteristics

VDS = 0V		VDS = -1V	
VGS(V)	ID (mA)	VGS(V)	ID (mA)
0		0	
0.5		0.5	
1		1	
1.5		1.5	
2		2	
2.5		2.5	
3		3	
4		4	
5		5	
6		6	
7		7	
8		8	
9		9	
10		10	

Discussion

1. From the obtained data, sketch the transfer characteristics of the JFET.
2. Determine the values of V_P and I_{DSS} from the plot.
3. Calculate theoretically the value of g_m at V_{GS} = -1V and V_{GS} = -2V when V_{DS} = 10V and compare them with the measured quantities.
4. Sketch the drain characteristics of the JFET from the obtained data.
5. From the linear region of the drain characteristic, determine the value of the drain to source resistance r_{ds} when V_{GS} = 0V.
6. Compare between the JFET and the BJT.

Experiment No.7

The FET Common Source Amplifier

Object

The purpose of this experiment is to test the performance of the common source amplifier using the self-bias circuit.

Required Parts and Equipment's

1. Electronic Test Board. (M110)
2. Dual Polarity Variable DC Power Supply
3. Digital Multimeters.
4. Dual-Channel Oscilloscope.
5. Function Generator.
6. N-Channel JFET 2N3823
7. Resistors, R_5=100KΩ, R_6=10KΩ, R_8=1KΩ, R_7=2.2KΩ

Theory

The common source amplifier configuration is widely used amongst other JFET configurations and can provide both high voltages gain and large input impedance. In this configuration, the input signal is applied to the gate and the output signal is taken from the drain, while the source terminal being the reference or common. In order to work as an amplifier, the JFET should be properly biased by setting the gate-source voltage which results in the required drain current.

The N-channel JFET requires that the gate-source voltage always be less negative than the pinch-off voltage, but less than zero. Since virtually no gate current flows due to the JFET's high input impedance, the gate voltage is essentially at ground level. Consequently, using only a drain-supply voltage, the required negative quiescent gate-source voltage is developed by the voltage drop across the source resistor of the self-bias circuit shown in Fig.1. This circuit is one of the simplest and practical bias circuits for JFET amplifiers in which a single power supply is used.

In this circuit, the gate voltage is zero.

$$V_G = 0 \quad \text{.....(1)}$$

Thus, the gate-source voltage is given by:

$$V_{GS} = -I_D R_S \quad \text{.....(2)}$$

Where the drain current is given by:

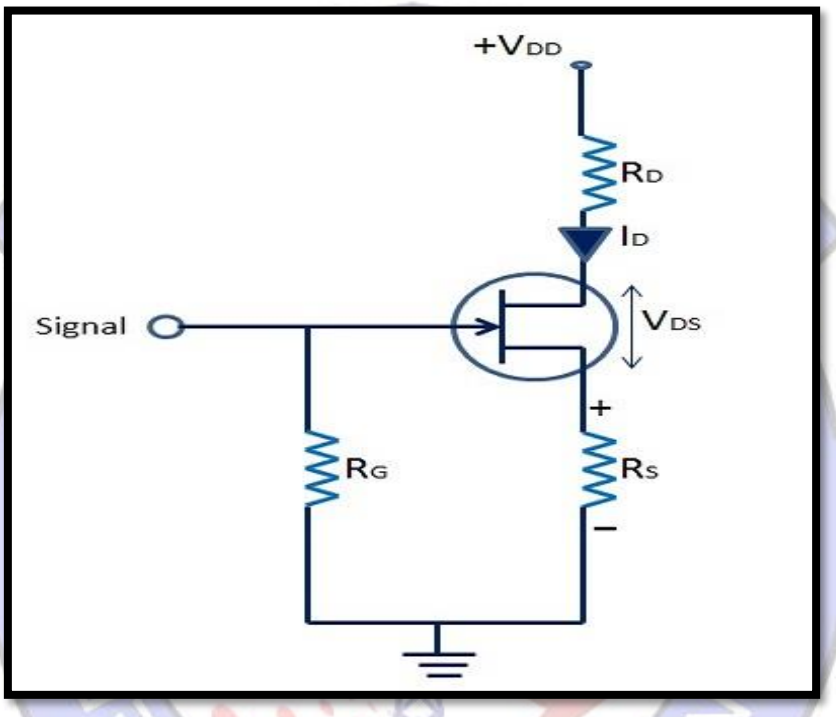


Figure 1: The Self-Bias JFET Circuit

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....(3)}$$

Solving equations (2) and (3) simultaneously will give both I_{DQ} and V_{GSQ}.

The drain-source voltage is given by:

$$V_{DS} = V_{DD} - I_D.(R_D + R_S) \quad \text{.....(4)}$$

A typical common-source amplifier circuit is shown in Fig.2. In this circuit, capacitors C_{c1} and C_{c2} are DC blocking capacitors, while C_S is a bypass capacitor for the source resistor R_S.

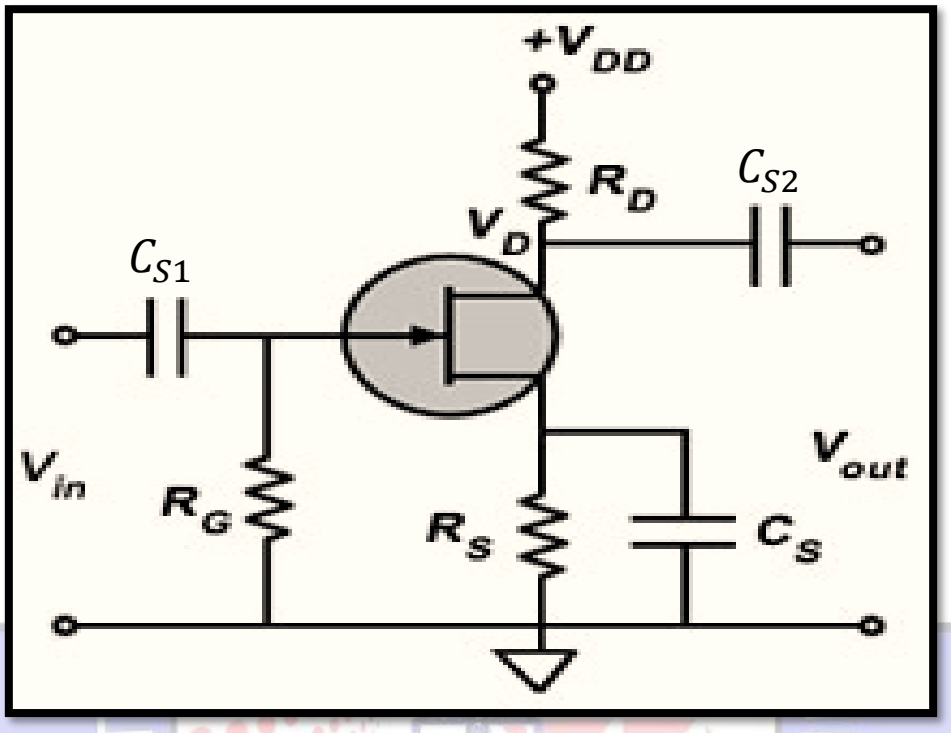


Figure 2: A Typical Common Source Amplifier

The small-signal approximate equivalent circuit for the amplifier of Fig.2 is presented in Fig.3.

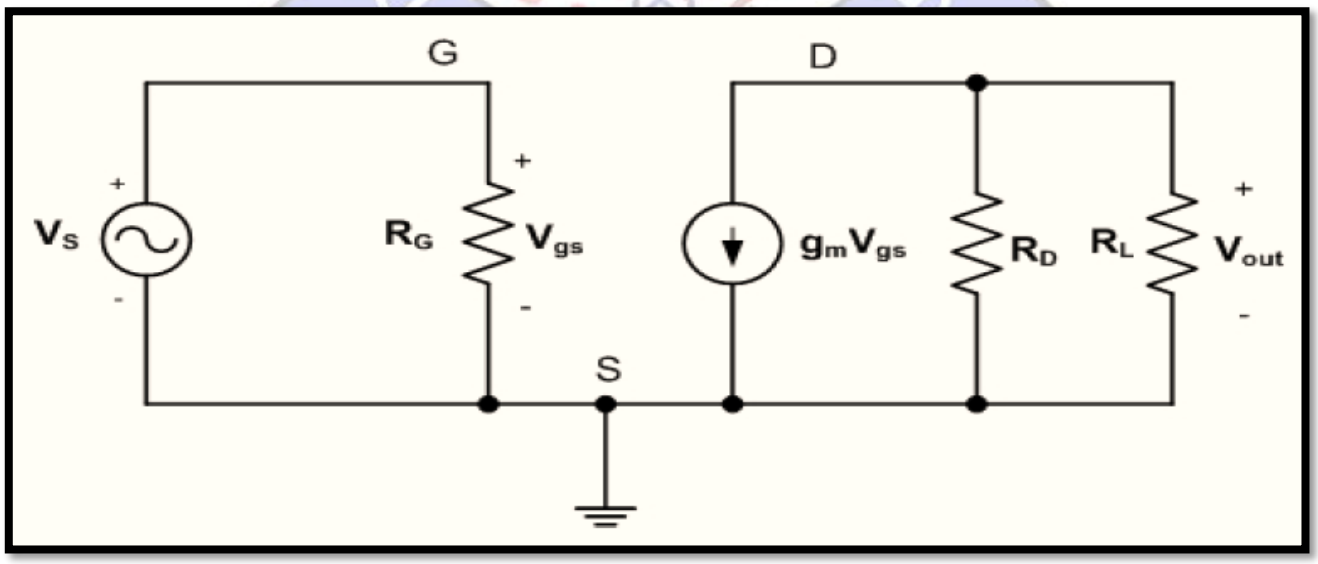


Figure 3: The Simplified Small-Signal Equivalent Circuit of the Amplifier

The transconductance of the JFET at the Q-point is derived as:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q-point} = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{.....(5)}$$

Where g_{mo} is given by:

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \quad \text{.....(6)}$$

The voltage gain of the amplifier can be derived from the equivalent circuit of Fig.4:

$$A_v = \frac{V_{out}}{V_S} = -g_m.(R_D \parallel R_L) \quad \text{.....(7)}$$

It can be shown that when the source bypass capacitor CS is removed, the voltage gain will become:

$$A_v = \frac{-g_m.(R_D \parallel R_L)}{1 + g_m.R_S} \quad \text{.....(8)}$$

The input impedance of the amplifier seen from the gate terminal is:

$$Z_{in} = R_G \quad \text{.....(9)}$$

And the output impedance seen from the output terminals is:

$$Z_{out} = R_D \quad \text{.....(10)}$$

Procedure

1. Connect the test circuit shown in Fig.4 to measure I_{DSS}. Increase the supply voltage until I_D no longer increases. This level of drain current is recorded as I_{DSS}.

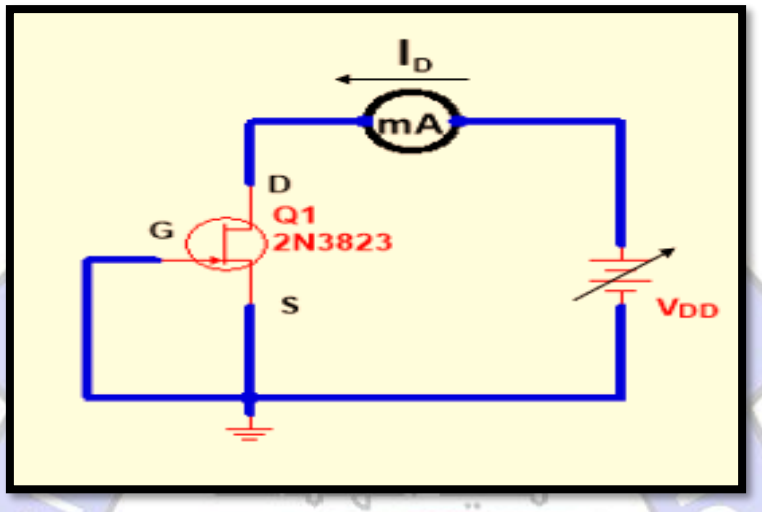


Figure 4: Test Circuit for Measuring I_{DSS}

2. Connect the test circuit shown in Fig.5 to measure V_P. The gate supply voltage V_{GG} is adjusted from 0 to larger negative values until the drain current I_D just reaches 0. The voltage V_{GS} to just cause the drain current to reach 0 is the measured value of V_P. Tabulate your results as shown in Table-1.

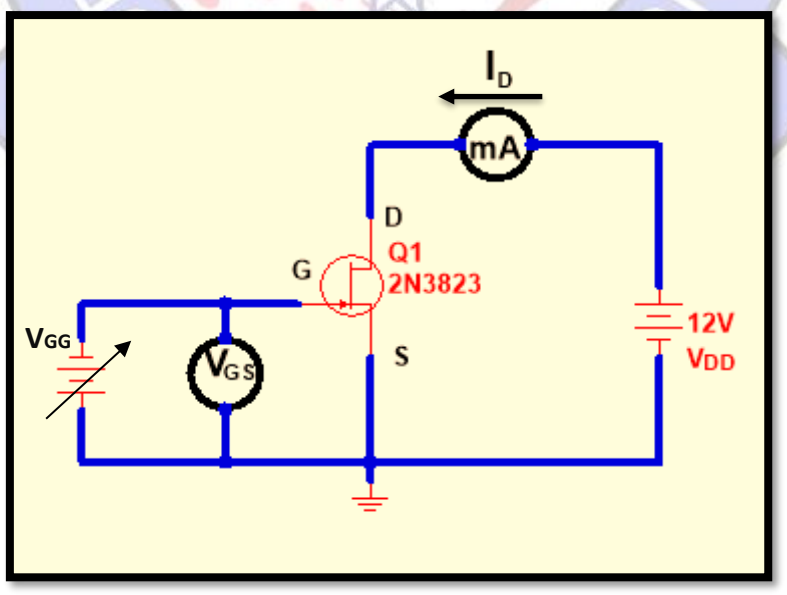


Figure 5: Test Circuit for Measuring V_P

Table-1: Measured JFET Parameters

Device Parameter	Value
I_{DSS}	
V_P	

3. Connect the JFET self-bias circuit shown in Fig.6 and measure the DC voltages V_G, V_S, and V_D with the aid of a digital multi-meter. Determine V_{GSQ}, I_{DQ}, V_{DSQ}, and g_m at the Q-point. Tabulate your results as illustrated in Table-2.

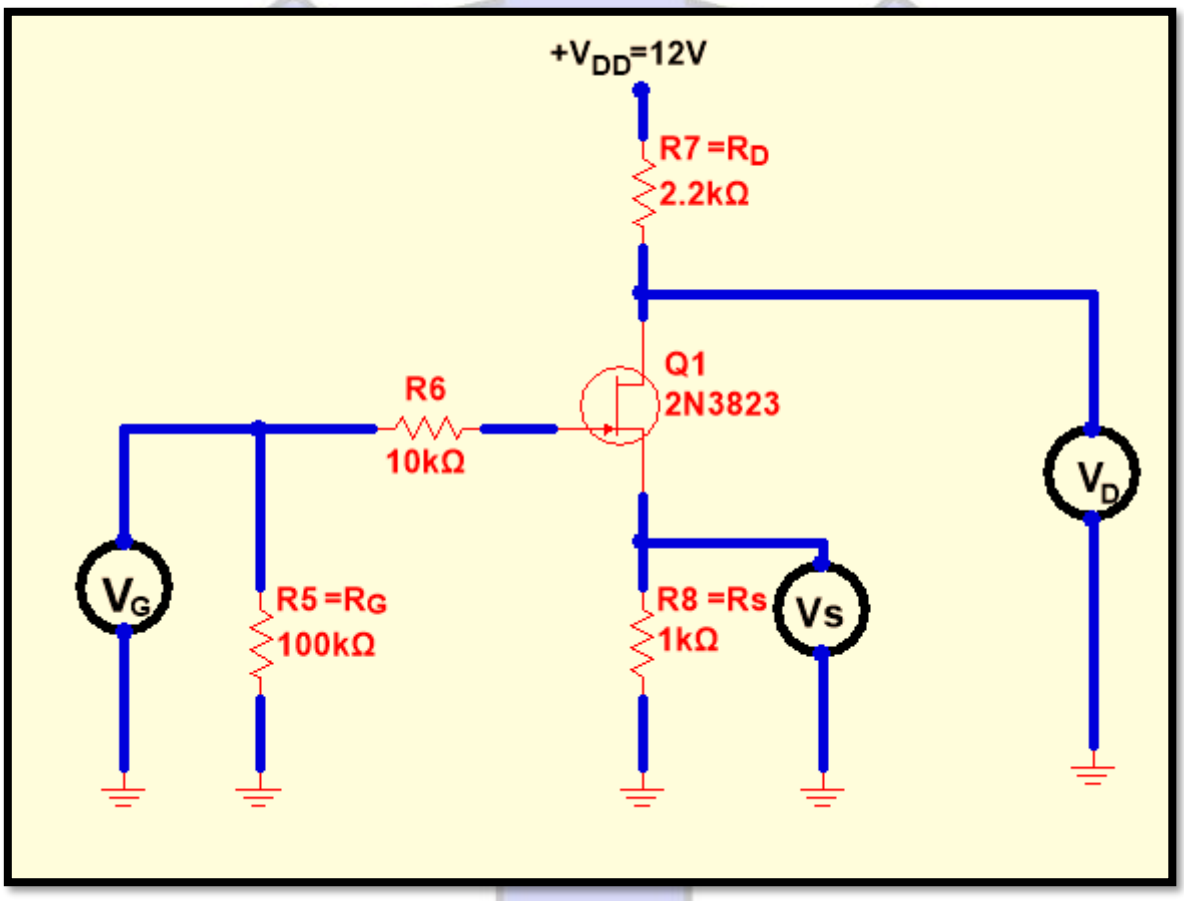


Figure 6: The Practical Bias Circuit of the Amplifier

4. Connect the amplifier circuit shown in Fig.7. Sketch the input (V_S) and output (V_D) signals and determine the voltage gain of the circuit in three cases as illustrated in Table-3.

Table-2: Measured Bias Circuit Parameters

Quantity	Value
V_G	
V_S	
V_D	
V_{GS}	
I_D	
V_{DS}	
g_m	

Table-3: Measured Voltage Gain Conditions

V_{in}	V_{out}	Voltage Gain (V_{out}/V_{in})
$0.1V_{PP}$		
$0.15V_{PP}$		
$0.2V_{PP}$		

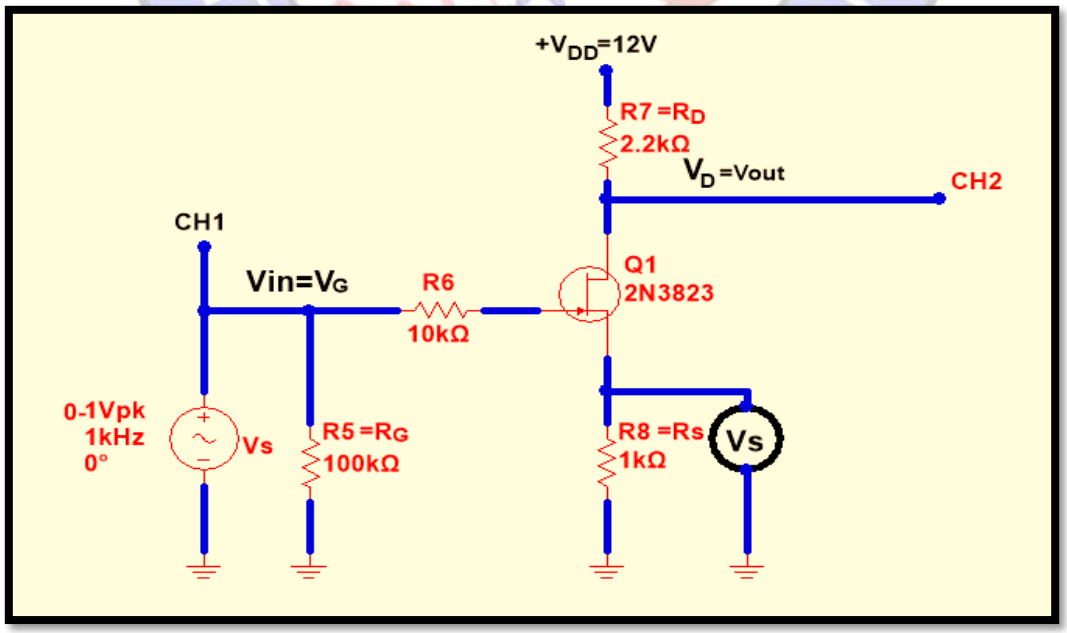


Figure 7: The Practical Common-Source Amplifier Circuit

Discussion

1. Using the measured device parameters I_{DSS} and V_P, calculate the theoretical Q-point values of I_{DQ} and V_{GSQ} and compare them with the measured quantities.
2. Indicate graphically the effect of increasing the source resistor R_S on the Q-point of the JFET.
3. Determine the DC power dissipation in the JFET connected in the amplifier circuit of Fig.7.
4. What is the effect of increasing the source resistance RS on the voltage gain of the amplifier circuit?