Experiment No.3

Logic Gate Circuits

Object

The purpose of this experiment is to implement the basic logic gate circuits and verify them.

Required Parts and Equipment's

1. Electronic Test Board. (M60, M90)
2. 5V DC Power Supply.
3. Digital Voltmeter.
4. Two BC 337 NPN silicon Transistors.
5. Resistors.M90 (10kΩand 1KΩ)
6. Two 1N4001 Silicon Diodes.

Theory

A logic gate is a switching circuit with two or more inputs and whose output will be either a high voltage or a low voltage, depending on the voltages on the various inputs. Logic gates are widely used in computers and in all types of digital circuits and systems.

Digital circuits are characterized by the fact that they contain voltages that exist at either of two levels, for example 0V and 5V. In other words, at any instant of time each circuit input and output voltage will either be at some LOW voltage (V_L) or some HIGH voltage (V_H). In practice, the LOW level is actually a range of voltages, as is the HIGH level. For example, between 0V and 0.8V might be the low level, and between 2V and 5V might be the HIGH level. The range of voltages between 0.8V and 2V is not allowed except during transitions between V_H and V_L. This concept is illustrated in Fig.1.

There are several types of logic gates, and many different ways to construct each type using discrete components. The basic logic gates are the OR gate, AND Gate, NOT gate, NOR gate, and NAND gate.

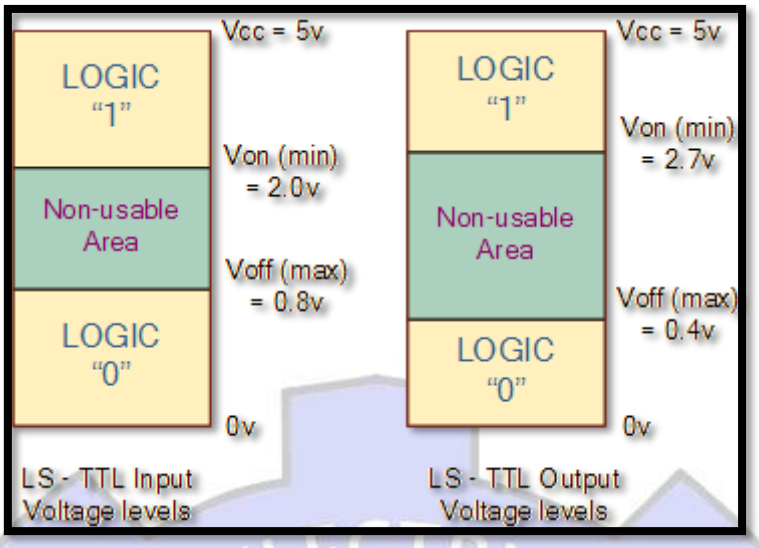


Figure1: Typical Voltage Levels in a Digital System

- **Diode OR Gate**

An OR gate is a circuit that has two or more inputs and whose output is equal to the OR sum (Logical Addition) of the inputs. Fig.2 shows the logic symbol and truth table of a two input OR gate.

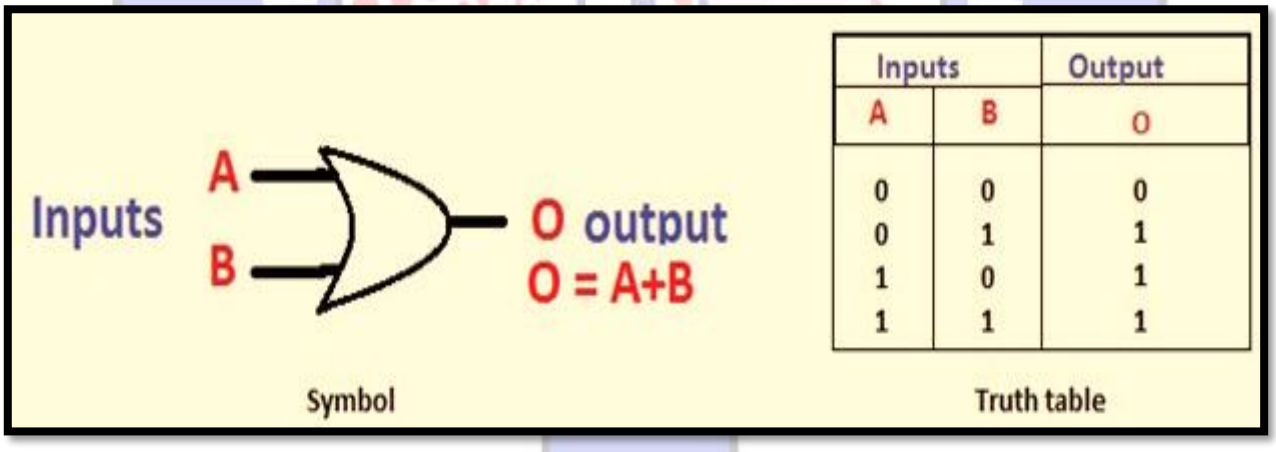
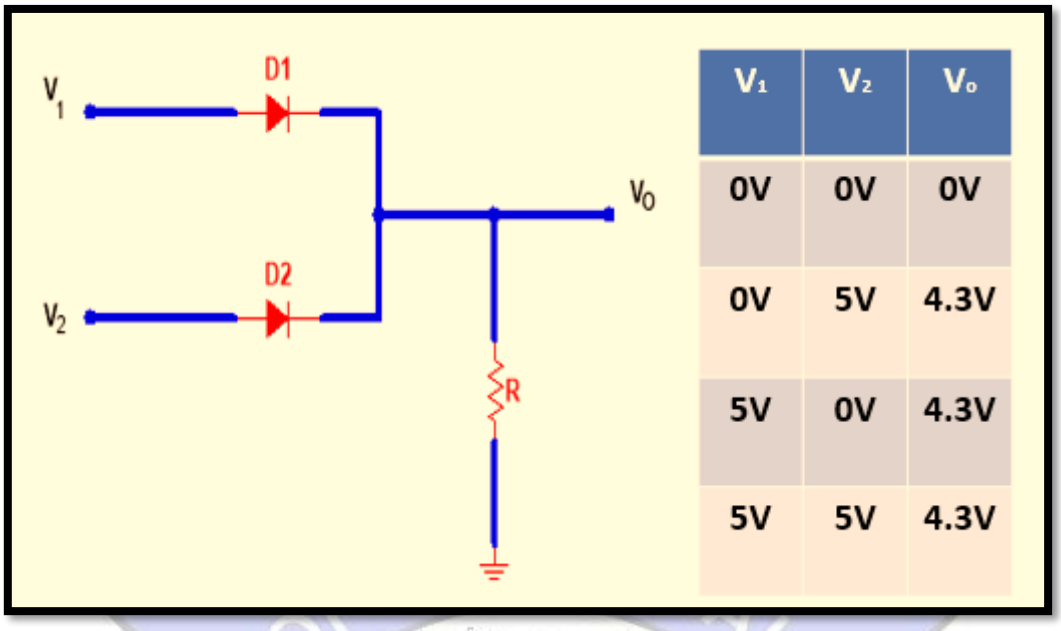


Figure 2: The Logic Symbol and Truth Table of the OR Gate

The OR gate operates such that its output is HIGH (Logic 1) if either input A or B or both are at a logic -1 level. The OR gate output will be LOW (logic 0) only if all its inputs are at logic- 0. Fig.3 presents a discrete circuit for the OR gate using two diodes and a resistor. Each input can be at either 0V or 5V, so there are four possible input combinations.



V_1	V_2	V_o
0V	0V	0V
0V	5V	4.3V
5V	0V	4.3V
5V	5V	4.3V

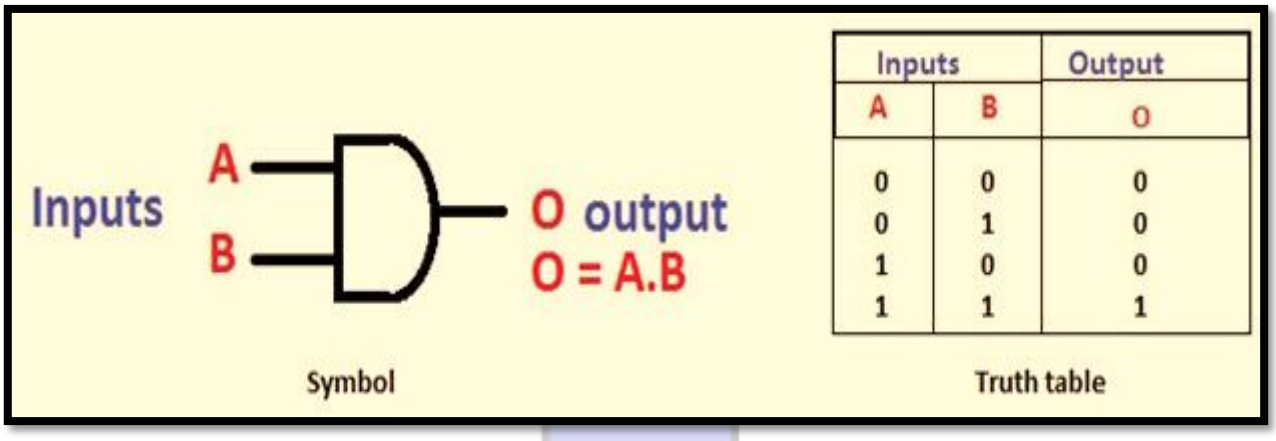
Figure 3: Two-input OR Gate Circuit

Examination of the truth table shows that the output will be at a HIHG level when either V_1 or V_2 or both are at a HIHG level. The value of V_o is LOW only when both inputs are at a LOW level.

Consider first the case where $V_1 = V_2 = 0V$. In this case neither diode will conduct; thus, no current flows in the circuit, and the output voltage is zero. When $V_1 = 0V$ and $V_2 = 5V$ then diode D_2 will be forward biased because its anode is made positive relative to its cathode. Thus, current will flow through D_2 and R. If the diodes are assumed to be silicon, the forward voltage drop across D_2 will be 0.7V, so V_0 must equal 5V - 0.7V = 4.3V. Diode D1 is reverse biased because its cathode is at +4.3 V relative to ground, and its anode is at 0V. The third case, where V1 = 5V and $V_2 = 0V$, will obviously be the same as the second case except that D1 will be ON, and D_2 will be OFF. In the final case, where both V_1 and V_2 are 5V, both diodes are ON, so each will have a 0.7V drop. Again, the output will be 4.3V.

- **Diode AND Gate**

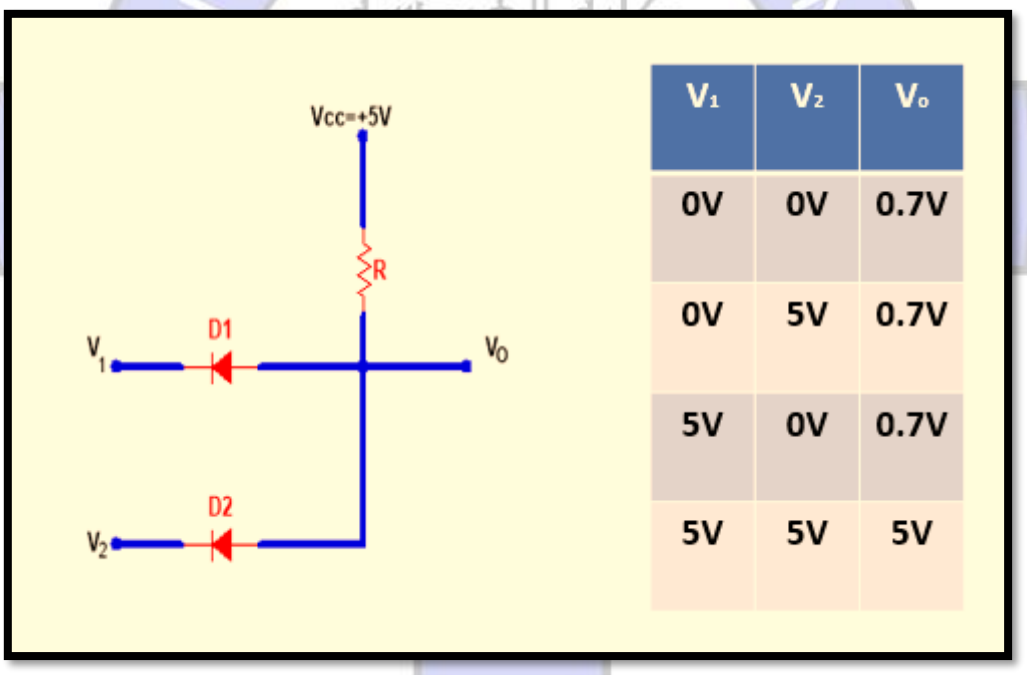
The second logic gate is the AND gate. Its symbol and truth table are presented in Fig.4. The output is equal to the AND product of the logic inputs (Logical Multiplication). The AND gate operates such that its output is HIGH only when all its inputs are HIGH. For all other cases the AND gate output is LOW.



Inputs		Output
A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4: The Logic Symbol and Truth Table of the AND Gate

The electronic circuit for the AND gate is shown in Fig.5. Consider the first case when $V_1 = V_2 = 0V$. In this case both diodes will be forward-biased and conduct current.



V_1	V_2	V_o
0V	0V	0.7V
0V	5V	0.7V
5V	0V	0.7V
5V	5V	5V

Figure 5: Two-input AND Gate Circuit

The output voltage in this case will equal the voltage drop across the diodes, which is 0.7V. When $V_1 = 0V$ and $V_2 = 5V$, diode D_1 will have its cathode at 0V, and thus will be forward - biased. So, current will flow from the 5V supply through R and D_1. Diode D_2 is OFF, since its cathode is at +5V. The output voltage V0 will be 0.7V, which is the voltage drop across D_1. In the third case when $V_1 = 5V$ and V_2

= 0V, diode D_1 will be OFF and D_2 will be ON and V0 will equal the voltage drop across D_2 which is 0.7V. Finally, when $V_1 = V_2 = 5V$, both diodes will be OFF and thus no current will flow through resistor R resulting in a zero voltage across R and 5V across the output ($V_0 = V_{CC} - V_R = 5V - 0 = 5V$).

- **The NOT Gate Circuit**

The NOT gate has a single input and output. The output equals the inverse of the input or the complement of the input. Fig.6 shows the symbol for the NOT gate, which is also called an inverter.

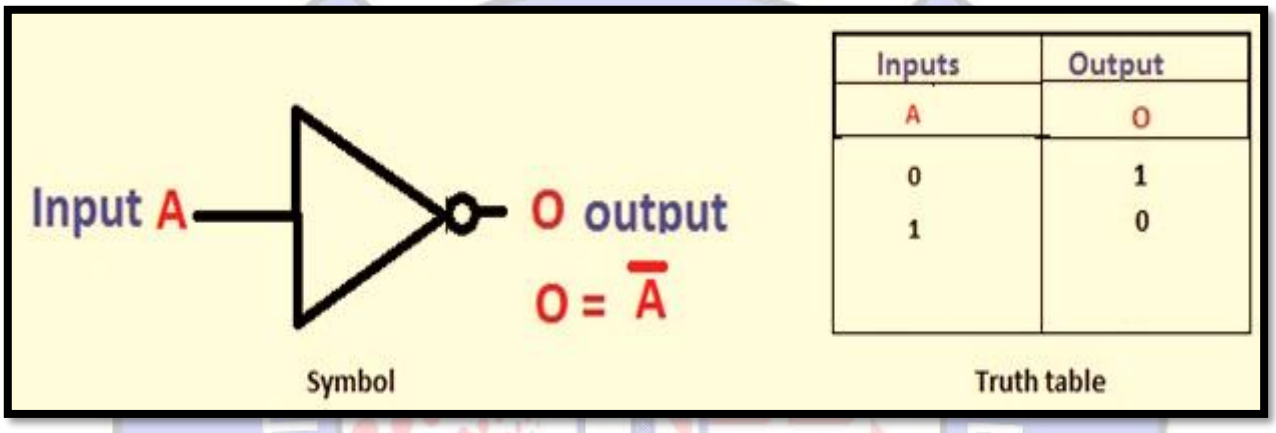


Figure 6: The Logic Symbol and Truth Table for the NOT Gate

The most widely used inverter circuit uses a bipolar transistor in the common-emitter configuration as shown in Fig.7. The input signal is applied to the base and the output is taken from the collector.

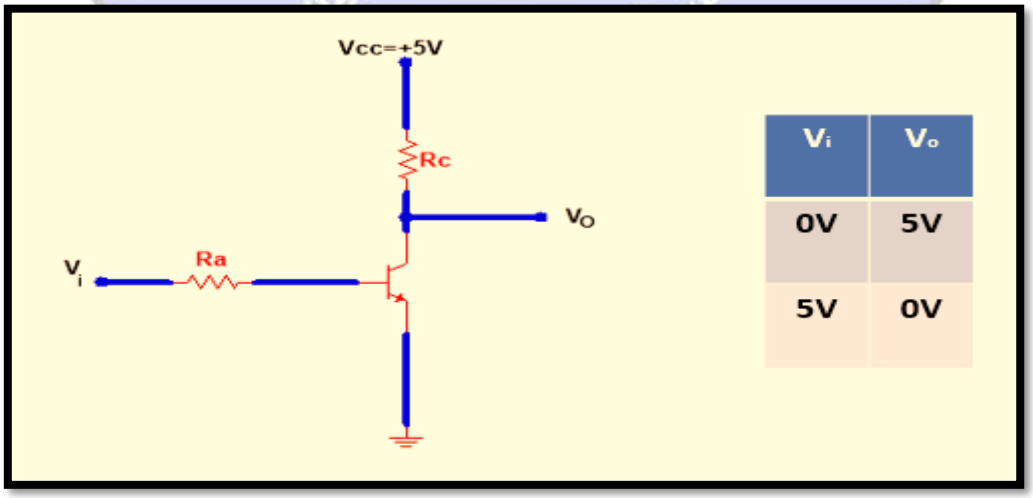


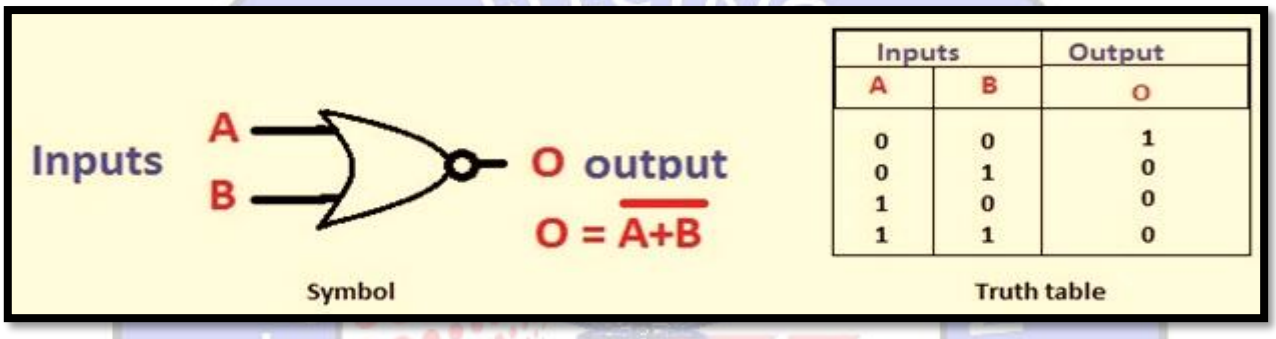
Figure 7: Transistor Inverter Circuit

The circuit operates so that when V_i = 0V, the transistor is OFF. Therefore, I_C is zero and no current flows through R_C. This means that the voltage drop across R_C is zero and the collector is at +5V above ground, producing V_0 = 5V.

When V_i = 5V, the transistor becomes ON and enters the saturation region when I_B is large enough. So, the collector voltage will be $V_{CE\,(sat)}$, and this produces $V_0 = V_{CE\,(sat)} \approx 0V$.

- **The NOR Gate Circuit**

Figure 8 shows the logic symbol for a two-input NOR gate. The operation of the NOR gate is equivalent to the OR gate followed by an inverter.

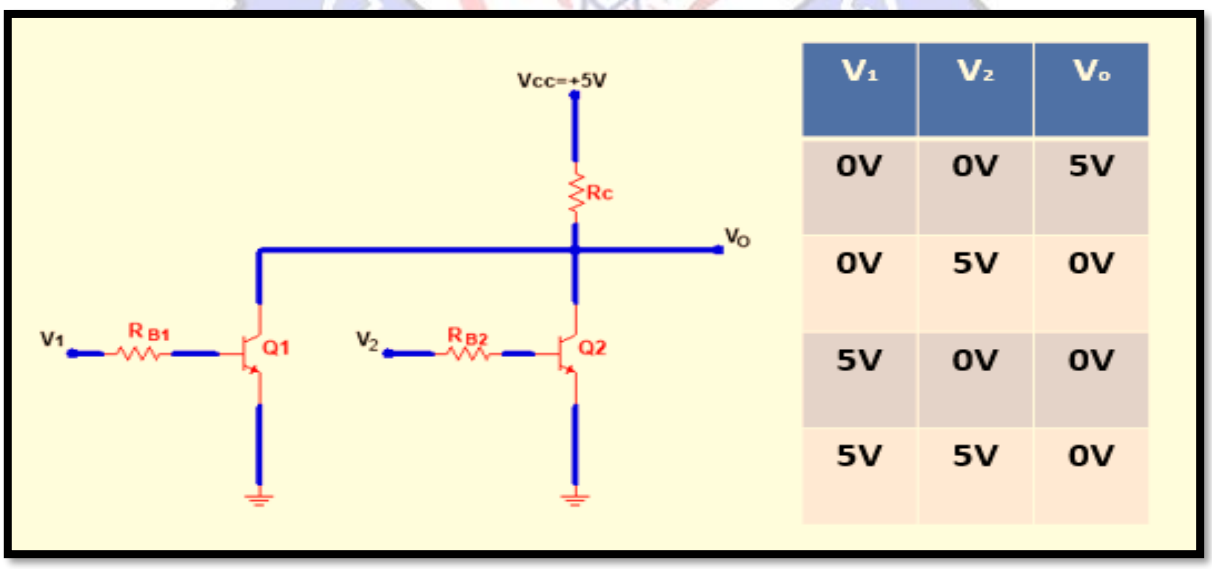


Inputs		Output
A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

Figure 8: The Logic Symbol and Truth Table for the NOR Gate

Figure 9 shows a practical electronic circuit for implementing the NOR gate. It consists of two transistors connected in parallel.



V_1	V_2	V_o
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

Figure 9: The NOR Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are in the cut-off region (OFF), and hence no current flows in resistor R_C. Therefore, the output voltage V_0 equals V_{CC} and is +5V.When $V_1=0$ and $V_2=5V$, transistor Q_1 will be OFF and transistor Q_2 will now be ON and enters the saturation

region. In this case, the current will flow in R_C through transistor Q_2. The output voltage will equal the saturation voltage of Q_2 and is approximately 0V ($V_o = V_{CE2(sat)} \approx 0V$).

When $V_1 = 5V$ and $V_2 = 0V$, the situation will be opposite to the previous case and $V_o = V_{CE2(sat)} \approx 0V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will conduct, and the output voltage will equal the saturation voltage of the transistors and hence is approximately 0V ($V_o = V_{CE\,(sat)} \approx 0V$).

- **The NAND Gate Circuit**

Figure 10 shows the logic symbol and the truth table of a two-input NAND gate. The operation of the NAND gate can be understood as being constituted from an AND gate followed by an inverter.

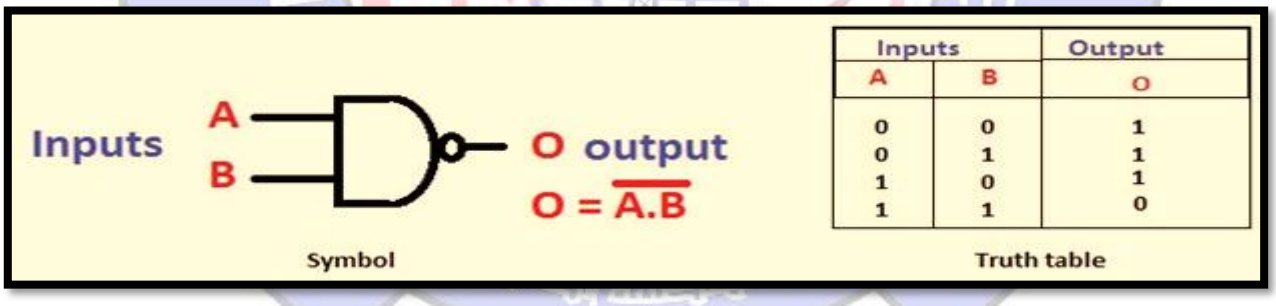
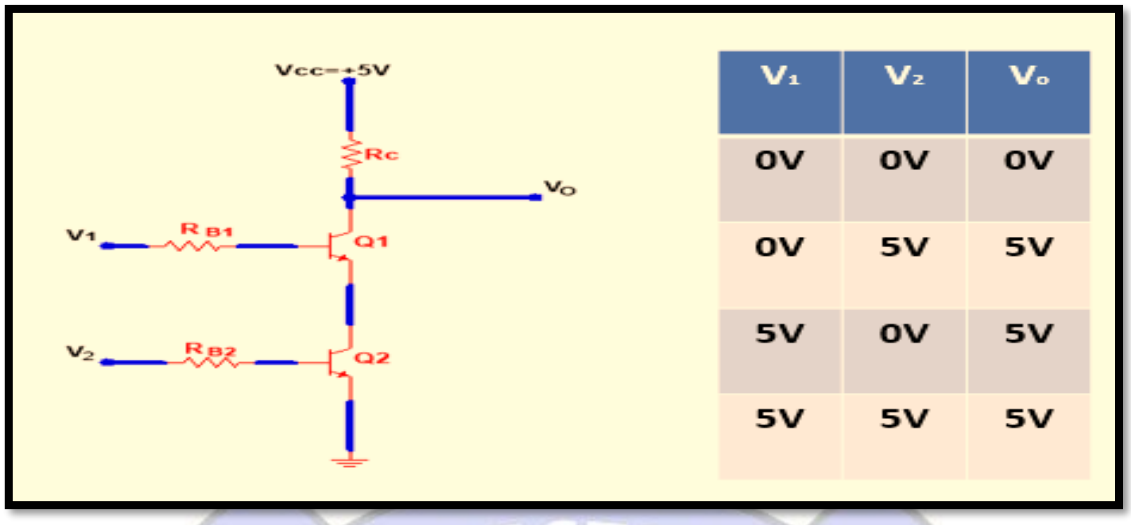


Figure 10: The Logic Symbol and Truth Table for the NAND Gate



V_1	V_2	V_o
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

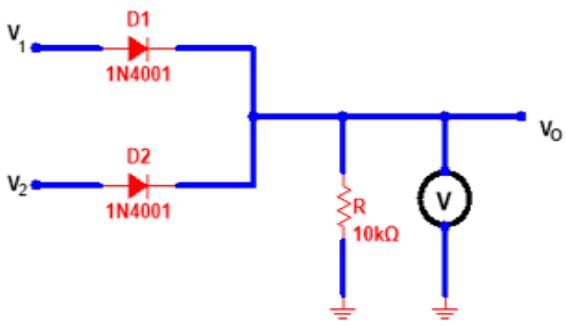
Figure 11: The NAND Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are OFF and no-current flows through RC and therefore $V_o = V_{CC} = 5V$. When $V_1=0$, and $V_2=5V$ transistor Q_2 will be ON, but Q_1 is OFF, and therefore no-current will flow through resistor R_C and V_0 is HIGH and equals 5V. In the third case, when $V_1 = 5V$, and $V_2= 0V$, transistor Q_1 becomes ON and Q_2 will be OFF and no current flows through R_C, and hence $V_0 = V_{CC} = 5V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will be ON and enter the saturation region. So, $V_0 = 2V_{sat} \approx 0V$ and will be LOW.

Procedure

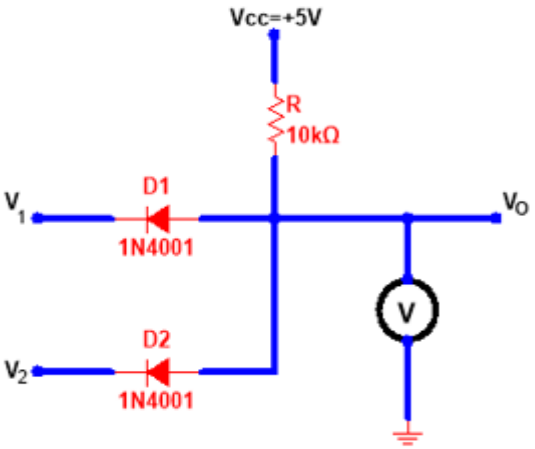
1. Connect the OR gate circuit shown in Fig.12 and verify its operation.



V_1	V_2	V_o
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 12: Practical OR Gate circuit

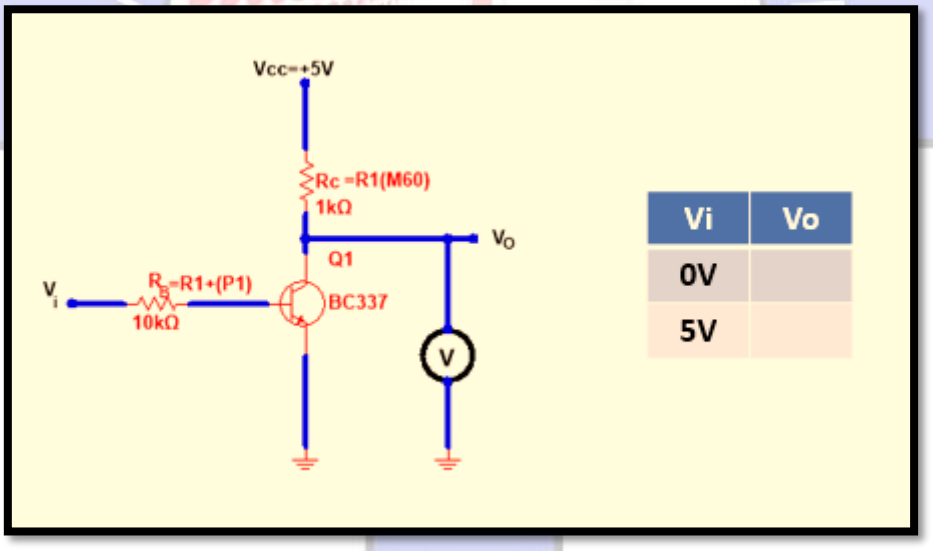
2. Connect the AND gate circuit shown in Fig.13 and verify its truth table.



V_1	V_2	V_o
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 13: Practical AND Gate Circuit

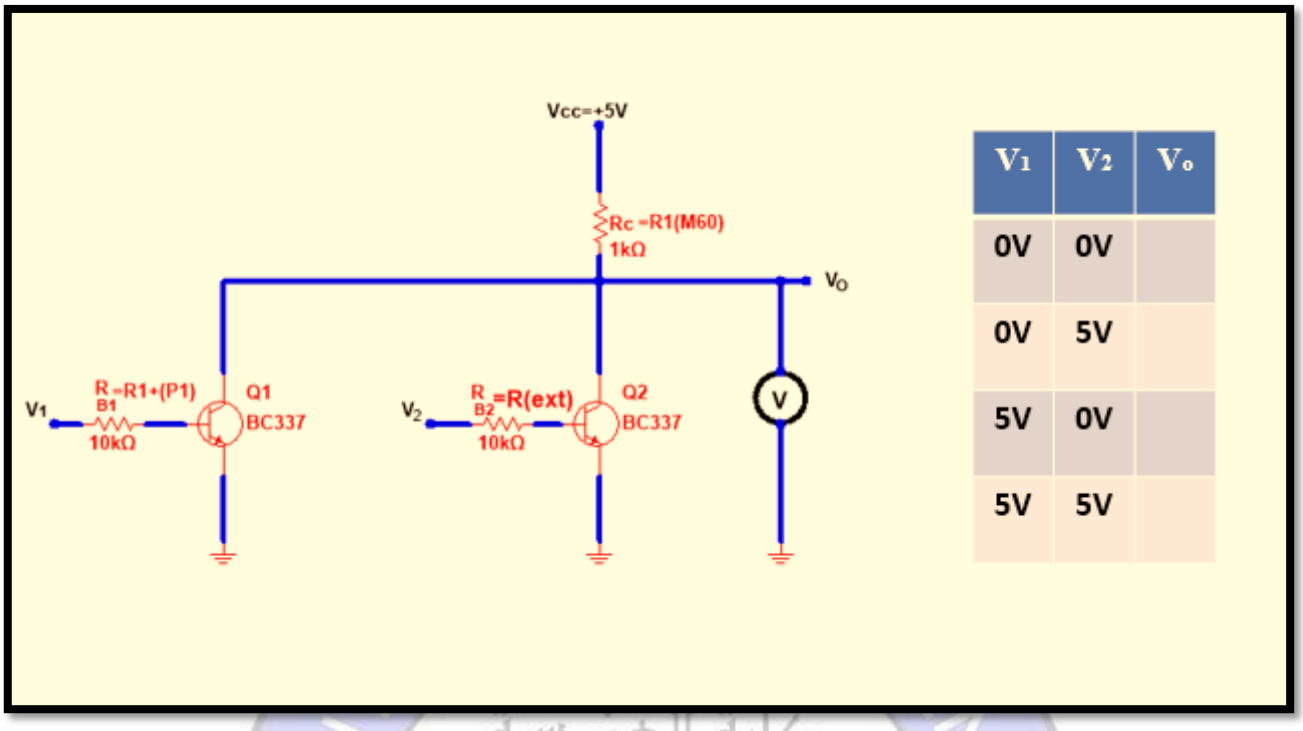
3. Connect the inverter circuit shown in Fig.14 and verify its operation. When Vi = 5V (HIGH), try to measure V_{BE} and V_{CE} of the transistor at saturation.



Vi	Vo
0V	
5V	

Figure 14: Practical Inverter Circuit

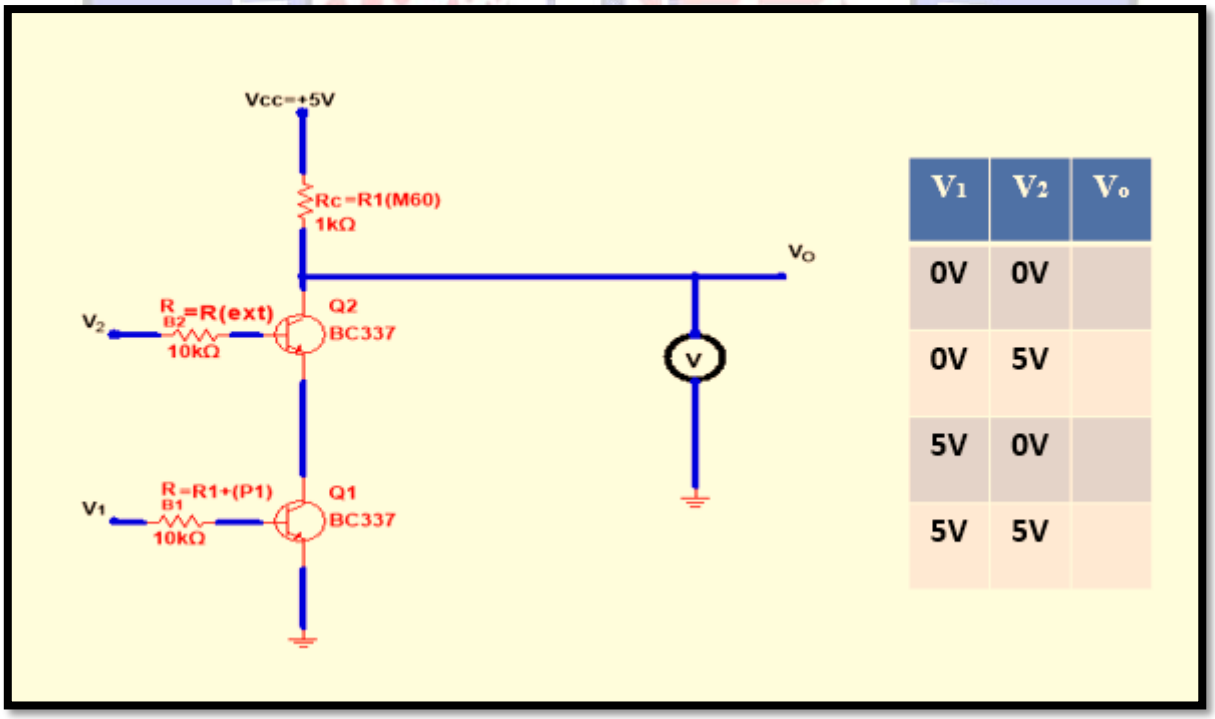
4. Connect the NOR gate circuit shown in Fig.15 and verify its truth table.



V1	V2	Vo
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Figure 15: Practical NOR Gate Circuit

5. Connect the NAND gate circuit shown in Fig.16 and verify its truth table.

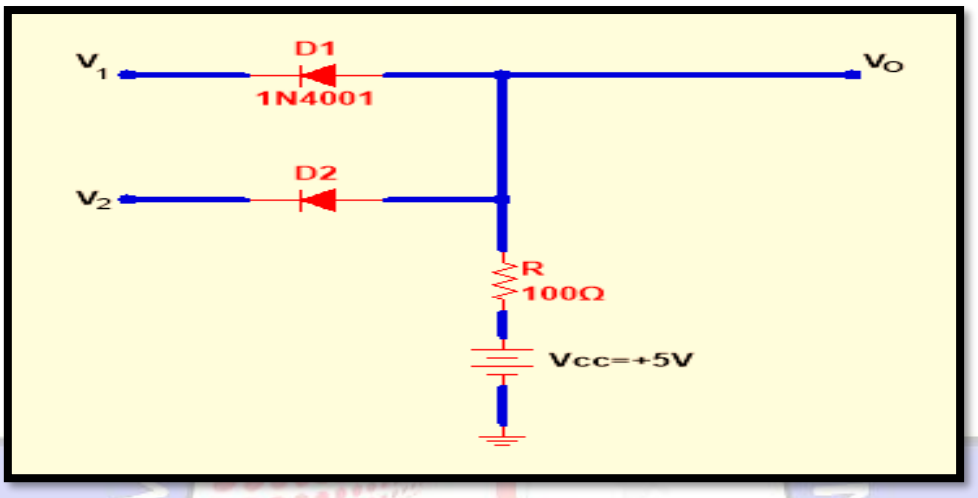


V1	V2	Vo
0V	0V	
0V	5V	
5V	0V	
5V	5V	

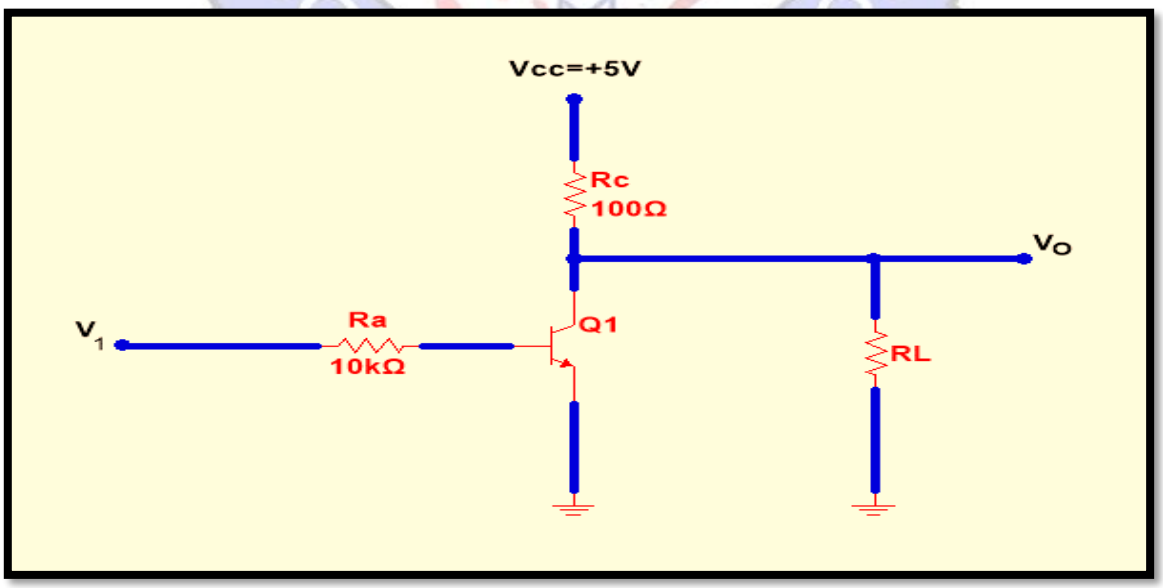
Figure 16: Practical NAND Gate Circuit

Discussion

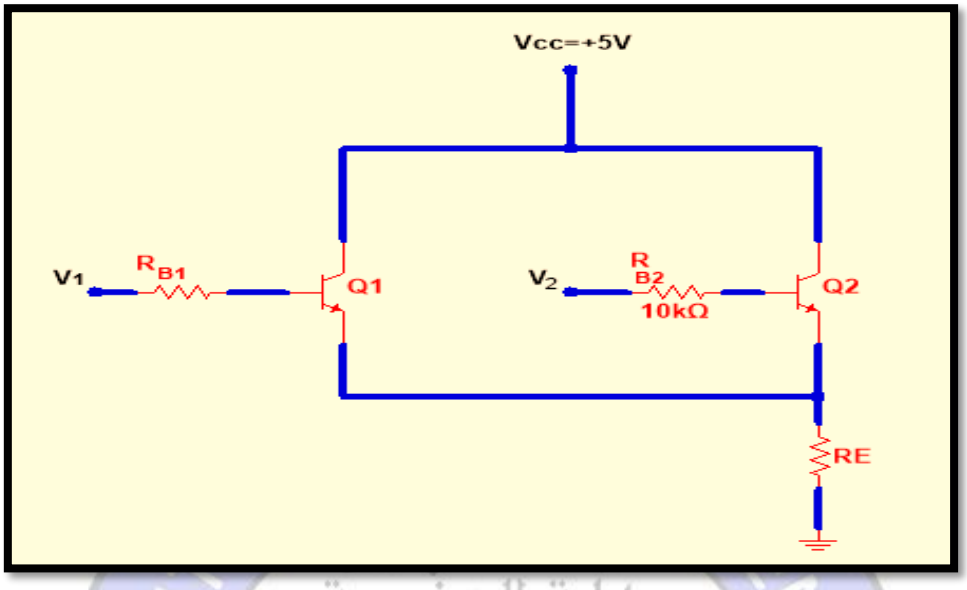
1. Determine the current flowing in each diode in the practical OR logic circuit of Fig.12 when both inputs are HIGH (5V).
2. What is the maximum current rating that each diode should have in the logic circuit shown below? Assume that the voltage drop across the silicon diode is 0.7V when it conducts.



3. For the inverter circuit of Fig.14, prove that the transistor is working deeply in saturation when Vi = 5V. Assume that β = 150 for the BC107 NPN transistor.
4. In the logic circuit shown below, what is the minimum RL that the inverter can drive without causing the output to drop below 4V when Vi = 0V?



5. What is the function of the digital circuit shown below? Describe its operation briefly and find its truth table.



6. Design a NAND Gate digital circuit using an AND gate and an inverter. Describe the operation of the circuit.
7. Design a NOR gate circuit using an OR gate circuit and an inverter. Describe briefly the operation of the circuit.
8. Determine the truth table of the digital circuit shown in the figure below and explain its operation.