Experiment No.7

The FET Common Source Amplifier

Object

The purpose of this experiment is to test the performance of the common source amplifier using the self-bias circuit.

Required Parts and Equipment's

1. Electronic Test Board. (M110)
2. Dual Polarity Variable DC Power Supply
3. Digital Multimeters.
4. Dual-Channel Oscilloscope.
5. Function Generator.
6. N-Channel JFET 2N3823
7. Resistors, R_5=100KΩ, R_6=10KΩ, R_8=1KΩ, R_7=2.2KΩ

Theory

The common source amplifier configuration is widely used amongst other JFET configurations and can provide both high voltages gain and large input impedance. In this configuration, the input signal is applied to the gate and the output signal is taken from the drain, while the source terminal being the reference or common. In order to work as an amplifier, the JFET should be properly biased by setting the gate-source voltage which results in the required drain current.

The N-channel JFET requires that the gate-source voltage always be less negative than the pinch-off voltage, but less than zero. Since virtually no gate current flows due to the JFET's high input impedance, the gate voltage is essentially at ground level. Consequently, using only a drain-supply voltage, the required negative quiescent gate-source voltage is developed by the voltage drop across the source resistor of the self-bias circuit shown in Fig.1. This circuit is one of the simplest and practical bias circuits for JFET amplifiers in which a single power supply is used.

In this circuit, the gate voltage is zero.

$$V_G = 0 \quad \text{.....(1)}$$

Thus, the gate-source voltage is given by:

$$V_{GS} = -I_D R_S \quad \text{.....(2)}$$

Where the drain current is given by:

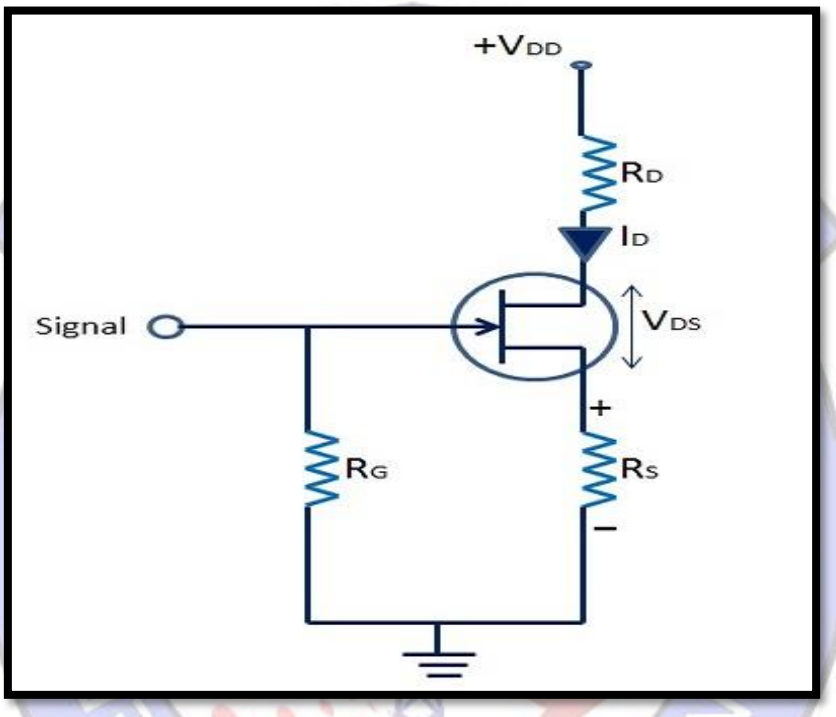

Figure 1: The Self-Bias JFET Circuit

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....(3)}$$

Solving equations (2) and (3) simultaneously will give both I_{DQ} and V_{GSQ}.

The drain-source voltage is given by:

$$V_{DS} = V_{DD} - I_D.(R_D + R_S) \quad \text{.....(4)}$$

A typical common-source amplifier circuit is shown in Fig.2. In this circuit, capacitors C_{c1} and C_{c2} are DC blocking capacitors, while C_S is a bypass capacitor for the source resistor R_S.

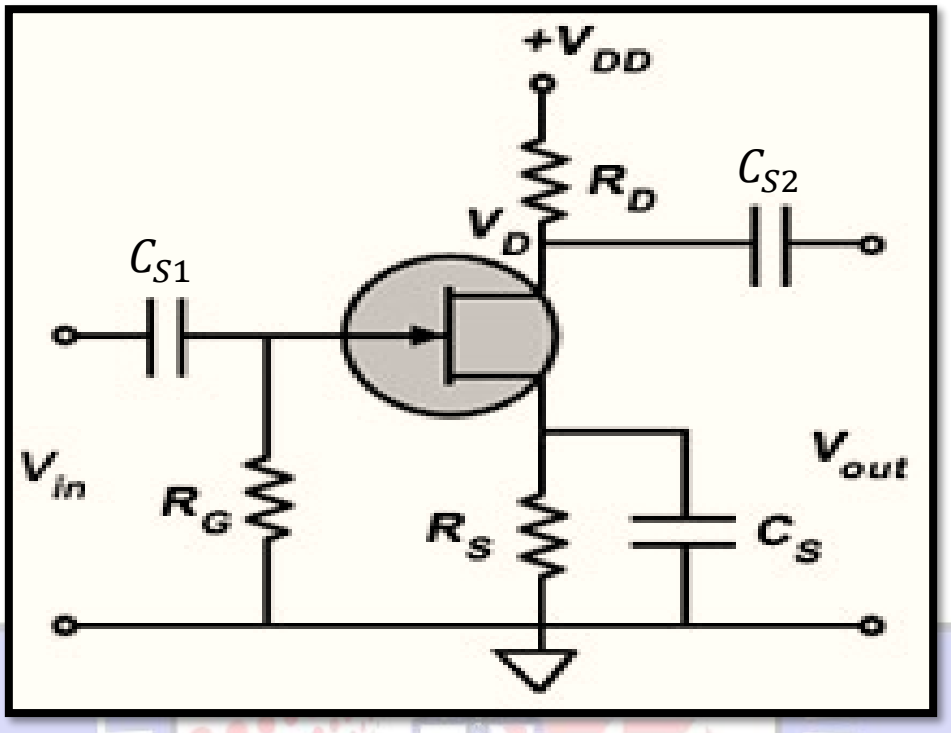

Figure 2: A Typical Common Source Amplifier

The small-signal approximate equivalent circuit for the amplifier of Fig.2 is presented in Fig.3.

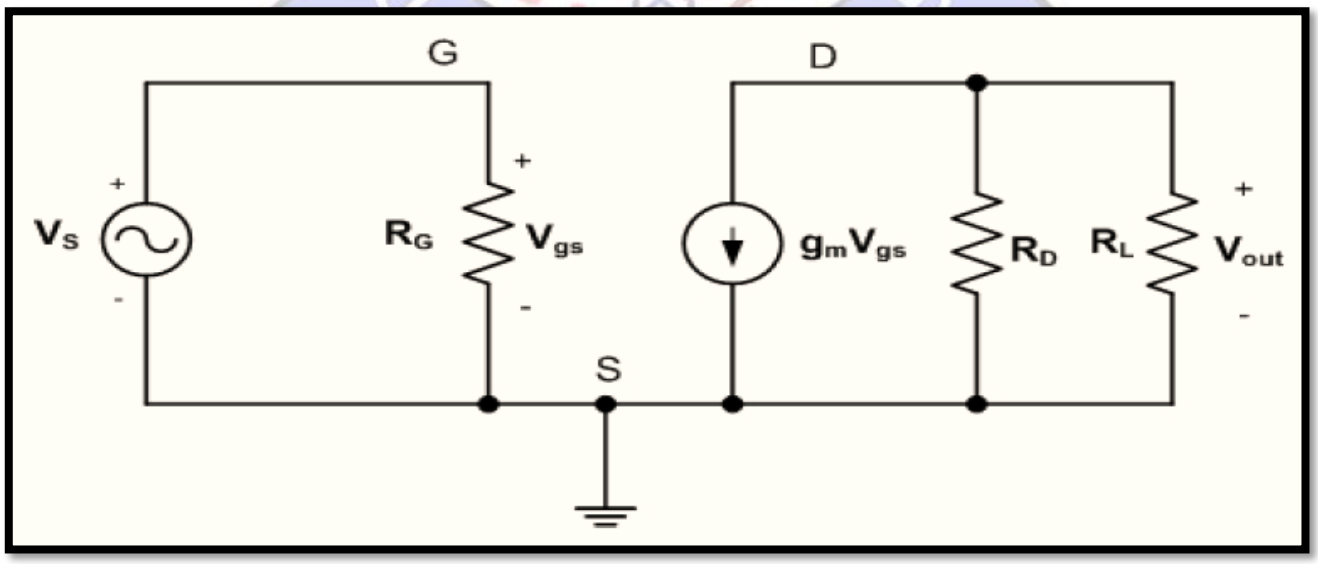

Figure 3: The Simplified Small-Signal Equivalent Circuit of the Amplifier

The transconductance of the JFET at the Q-point is derived as:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q-point} = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{.....(5)}$$

Where g_{mo} is given by:

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \quad \text{.....(6)}$$

The voltage gain of the amplifier can be derived from the equivalent circuit of Fig.4:

$$A_v = \frac{V_{out}}{V_S} = -g_m.(R_D \parallel R_L) \quad \text{.....(7)}$$

It can be shown that when the source bypass capacitor CS is removed, the voltage gain will become:

$$A_v = \frac{-g_m.(R_D \parallel R_L)}{1 + g_m.R_S} \quad \text{.....(8)}$$

The input impedance of the amplifier seen from the gate terminal is:

$$Z_{in} = R_G \quad \text{.....(9)}$$

And the output impedance seen from the output terminals is:

$$Z_{out} = R_D \quad \text{.....(10)}$$

Procedure

1. Connect the test circuit shown in Fig.4 to measure I_{DSS}. Increase the supply voltage until I_D no longer increases. This level of drain current is recorded as I_{DSS}.

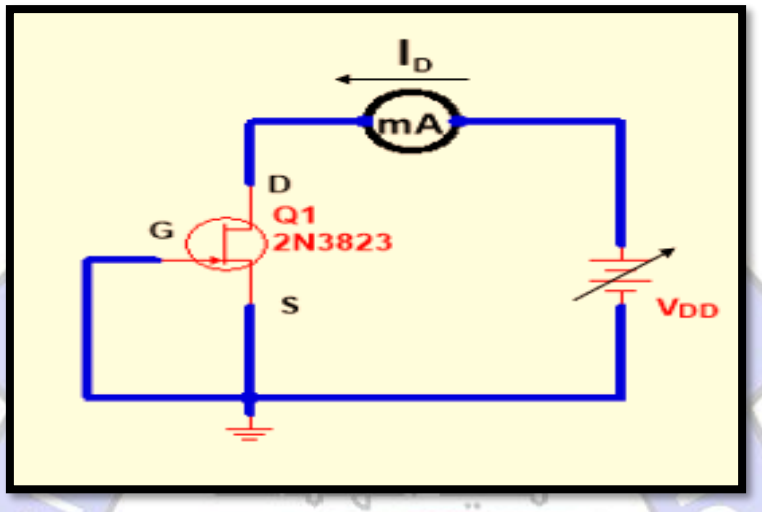

Figure 4: Test Circuit for Measuring I_{DSS}

2. Connect the test circuit shown in Fig.5 to measure V_P. The gate supply voltage V_{GG} is adjusted from 0 to larger negative values until the drain current I_D just reaches 0. The voltage V_{GS} to just cause the drain current to reach 0 is the measured value of V_P. Tabulate your results as shown in Table-1.

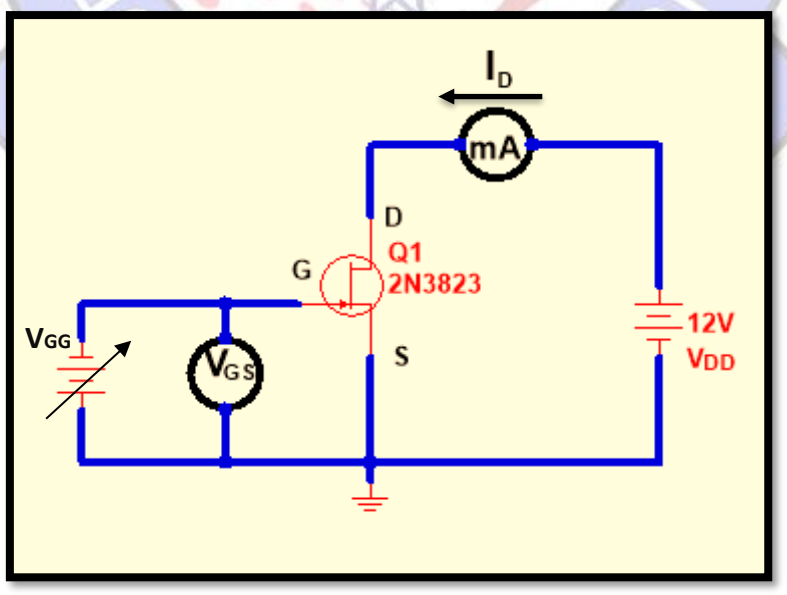

Figure 5: Test Circuit for Measuring V_P

Table-1: Measured JFET Parameters

Device Parameter	Value
I_{DSS}	
V_P	

3. Connect the JFET self-bias circuit shown in Fig.6 and measure the DC voltages V_G, V_S, and V_D with the aid of a digital multi-meter. Determine V_{GSQ}, I_{DQ}, V_{DSQ}, and g_m at the Q-point. Tabulate your results as illustrated in Table-2.

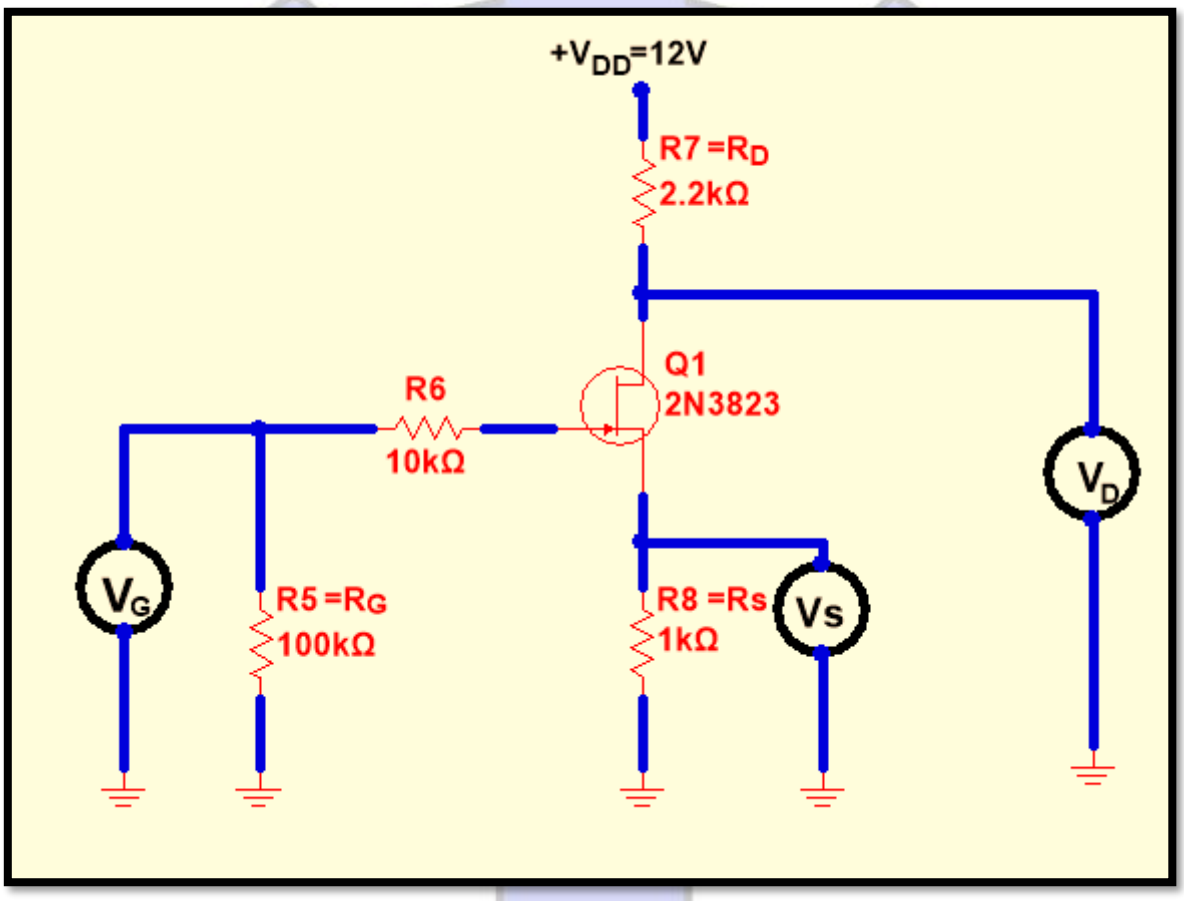

Figure 6: The Practical Bias Circuit of the Amplifier

4. Connect the amplifier circuit shown in Fig.7. Sketch the input (V_S) and output (V_D) signals and determine the voltage gain of the circuit in three cases as illustrated in Table-3.

Table-2: Measured Bias Circuit Parameters

Quantity	Value
V_G	
V_S	
V_D	
V_{GS}	
I_D	
V_{DS}	
g_m	

Table-3: Measured Voltage Gain Conditions

V_{in}	V_{out}	Voltage Gain (V_{out}/V_{in})
$0.1V_{PP}$		
$0.15V_{PP}$		
$0.2V_{PP}$		

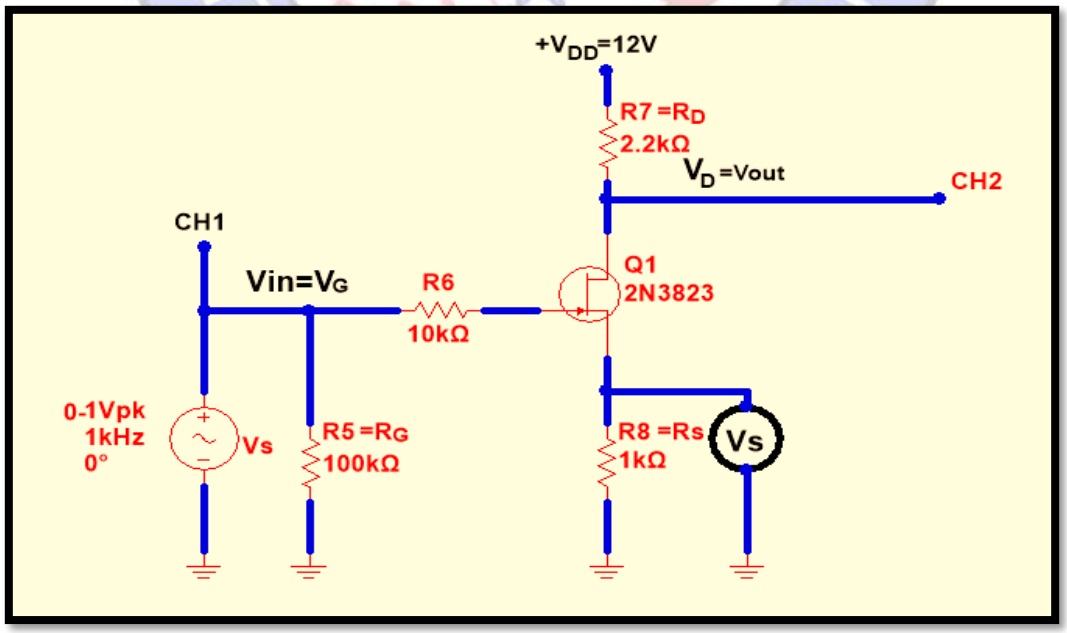

Figure 7: The Practical Common-Source Amplifier Circuit

Discussion

1. Using the measured device parameters I_{DSS} and V_P, calculate the theoretical Q-point values of I_{DQ} and V_{GSQ} and compare them with the measured quantities.
2. Indicate graphically the effect of increasing the source resistor R_S on the Q-point of the JFET.
3. Determine the DC power dissipation in the JFET connected in the amplifier circuit of Fig.7.
4. What is the effect of increasing the source resistance RS on the voltage gain of the amplifier circuit?