Fundumantal of Electronic II

Second Class

Chapter 7 : FET Biasing
Lec07_p2

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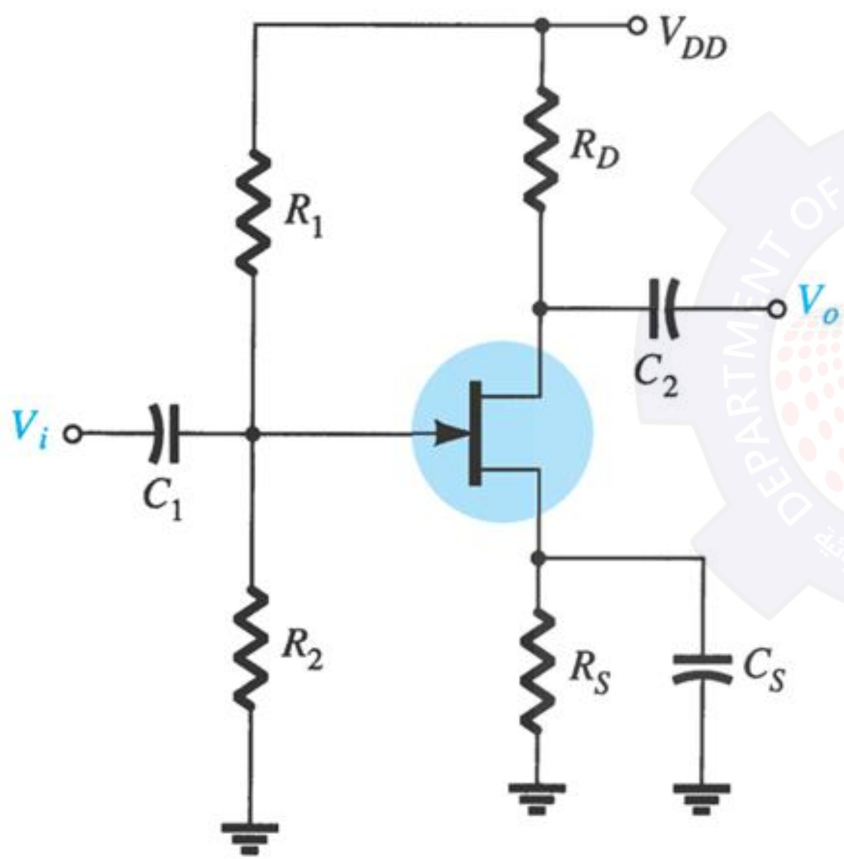
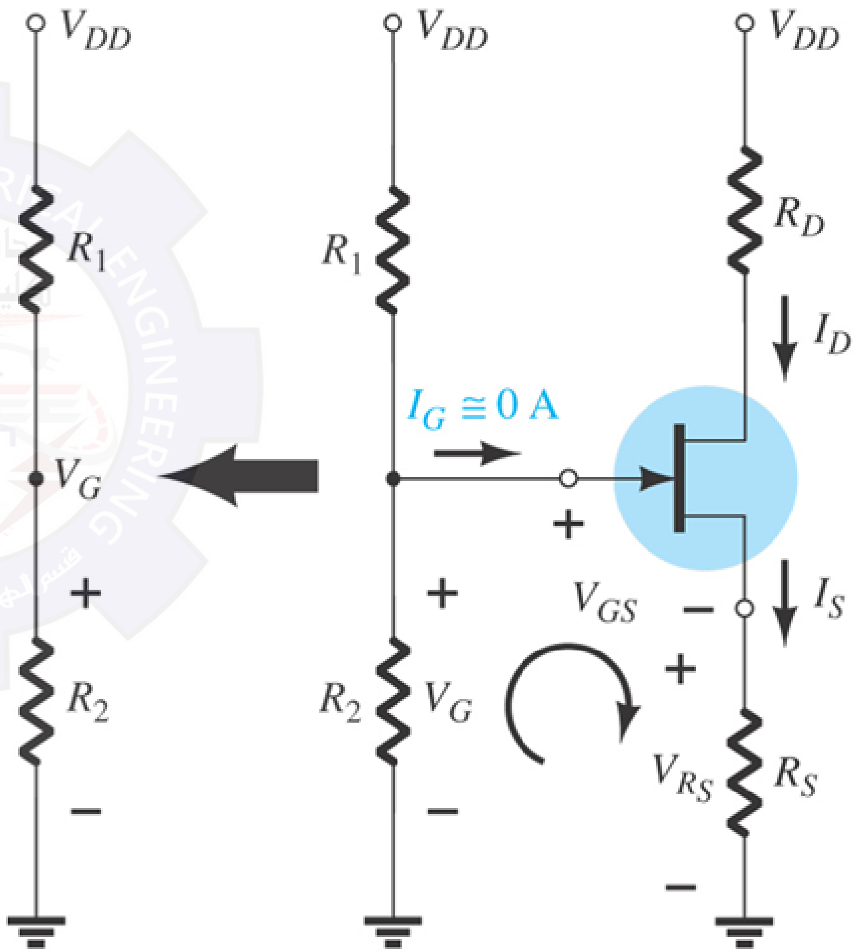
Voltage-Divider Bias





$I_G = 0\ A$

$I_{R1} = I_{R2}$

Redrawn network for dc analysis.

Voltage-Divider Bias

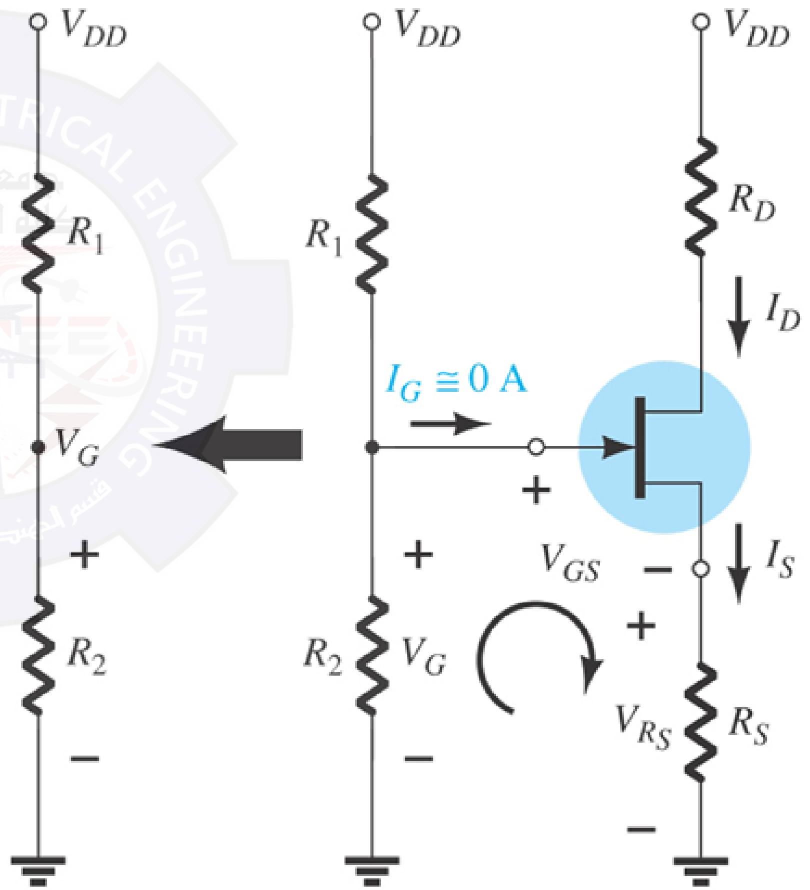
V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.



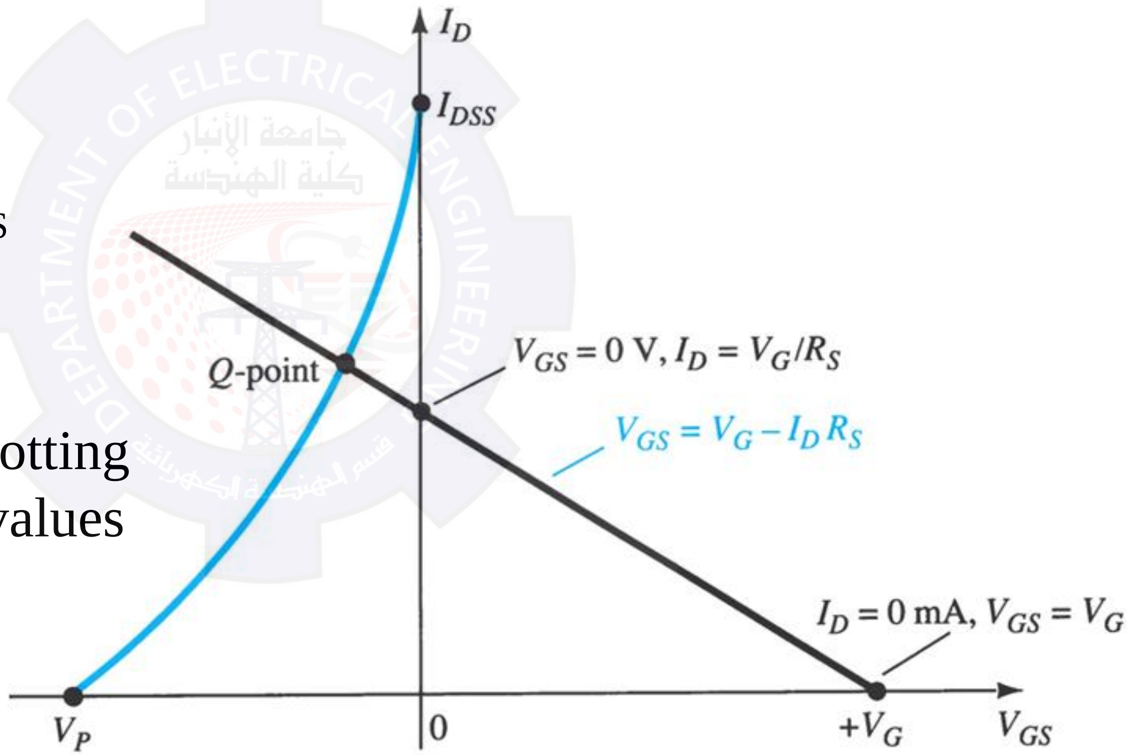
Voltage-Divider Bias

Step 1

$$V_{GS} = V_G - I_D R_S$$

Plot the line by plotting two points:

- $V_{GS} = V_G$, $I_D = 0$ A
- $V_{GS} = 0$ V, $I_D = V_G / R_S$



Step 2

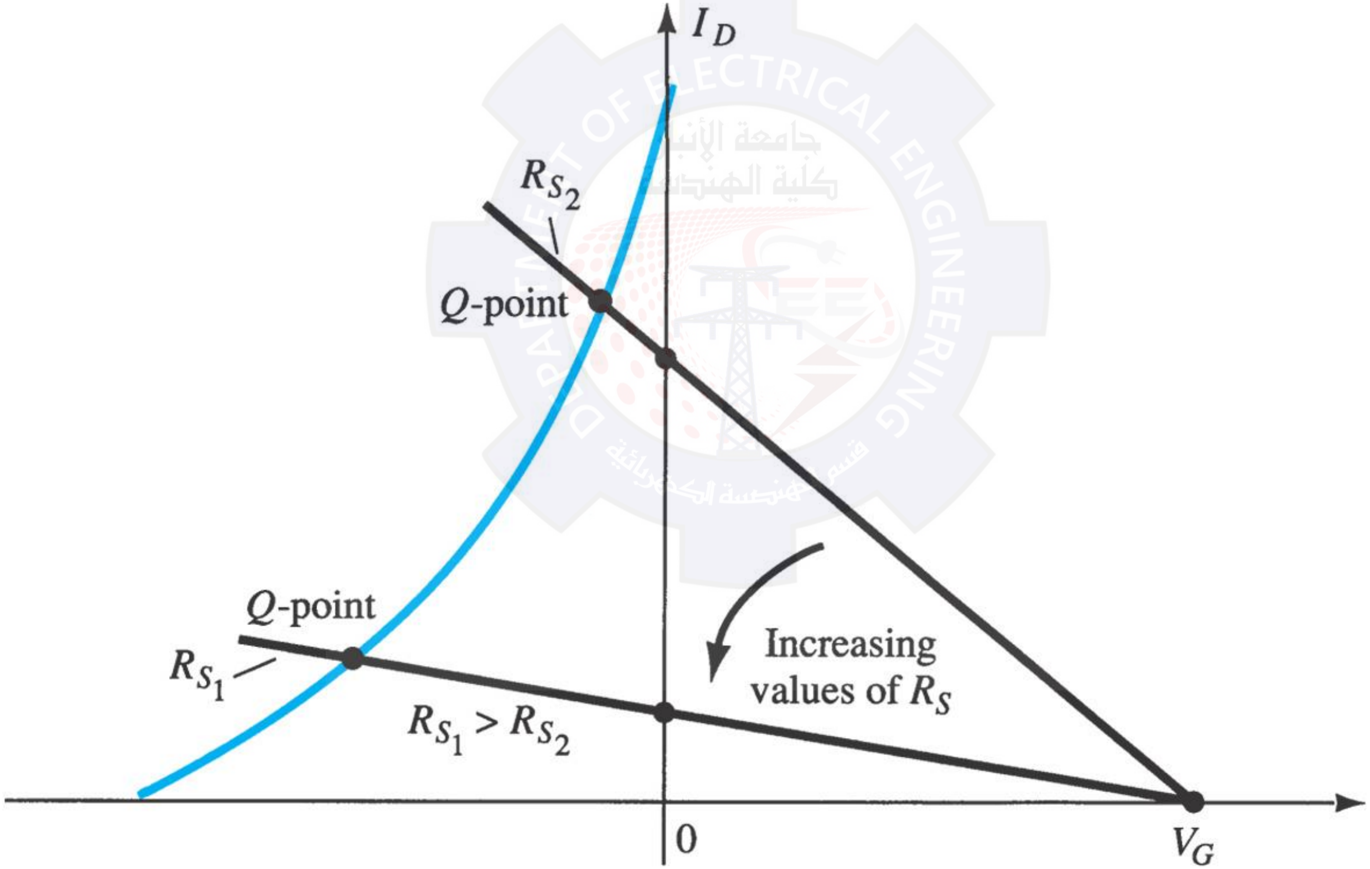
Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve

Voltage-Divider Bias

$$V_{GS} = V_G - I_D R_S$$



Effect of R_S on the resulting Q-point.

Voltage-Divider Bias

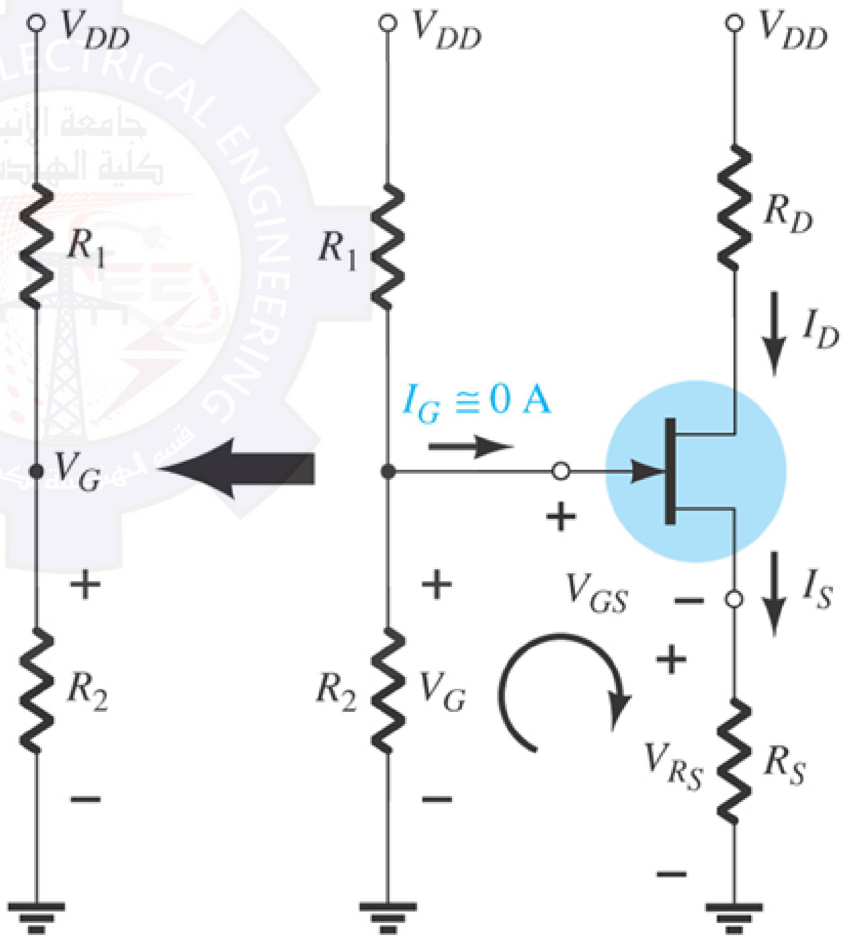
Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

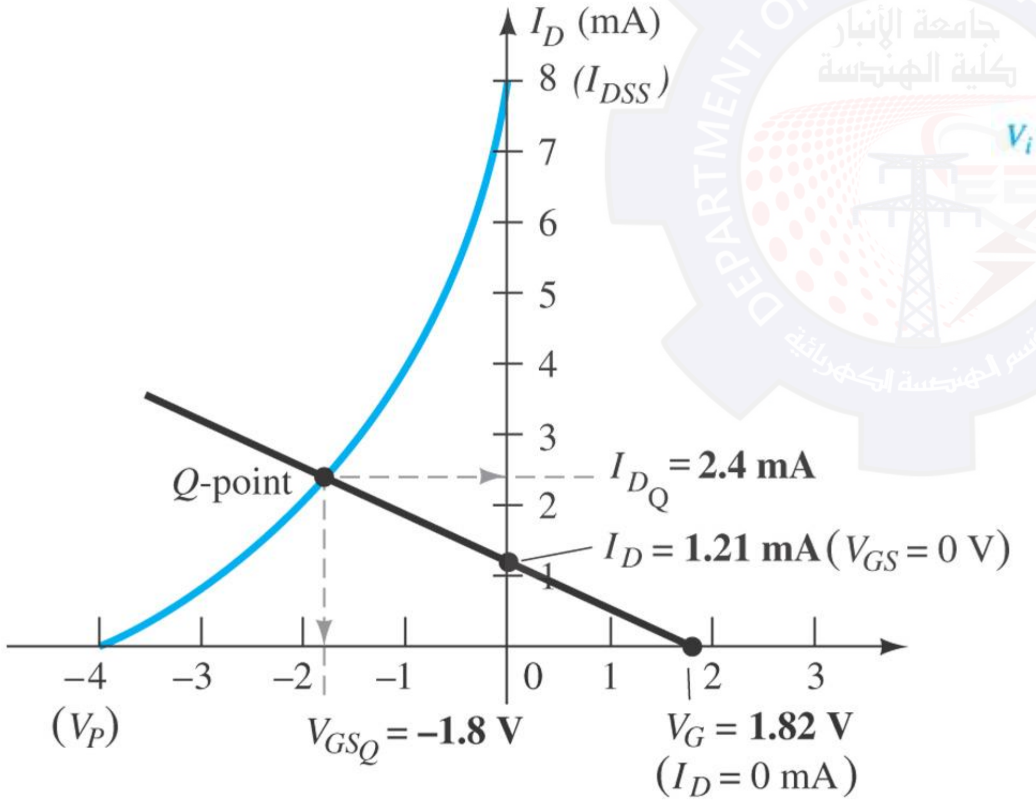
$$V_S = I_D R_S$$

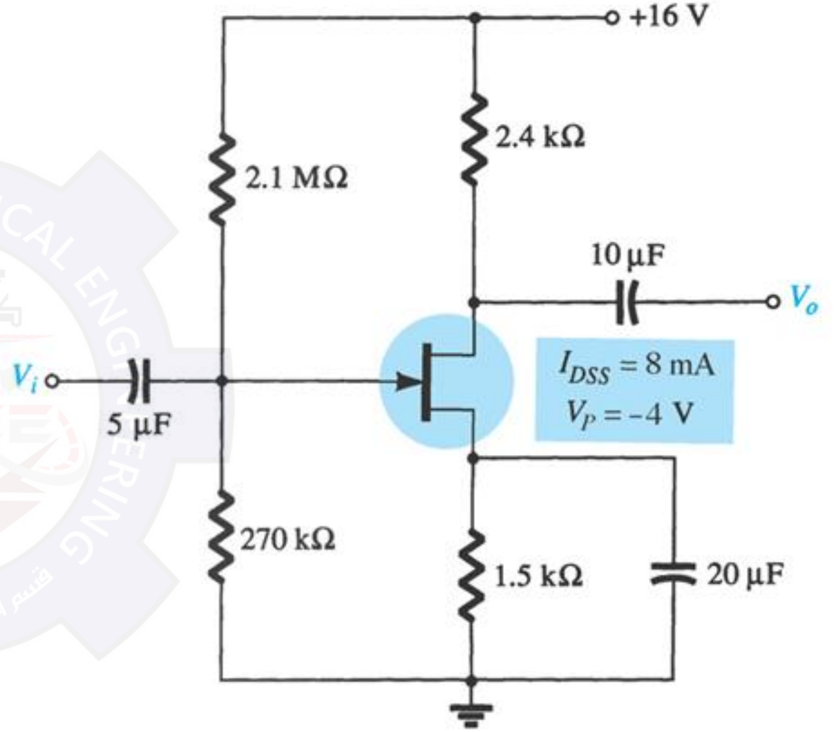
$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$



Example 7.5

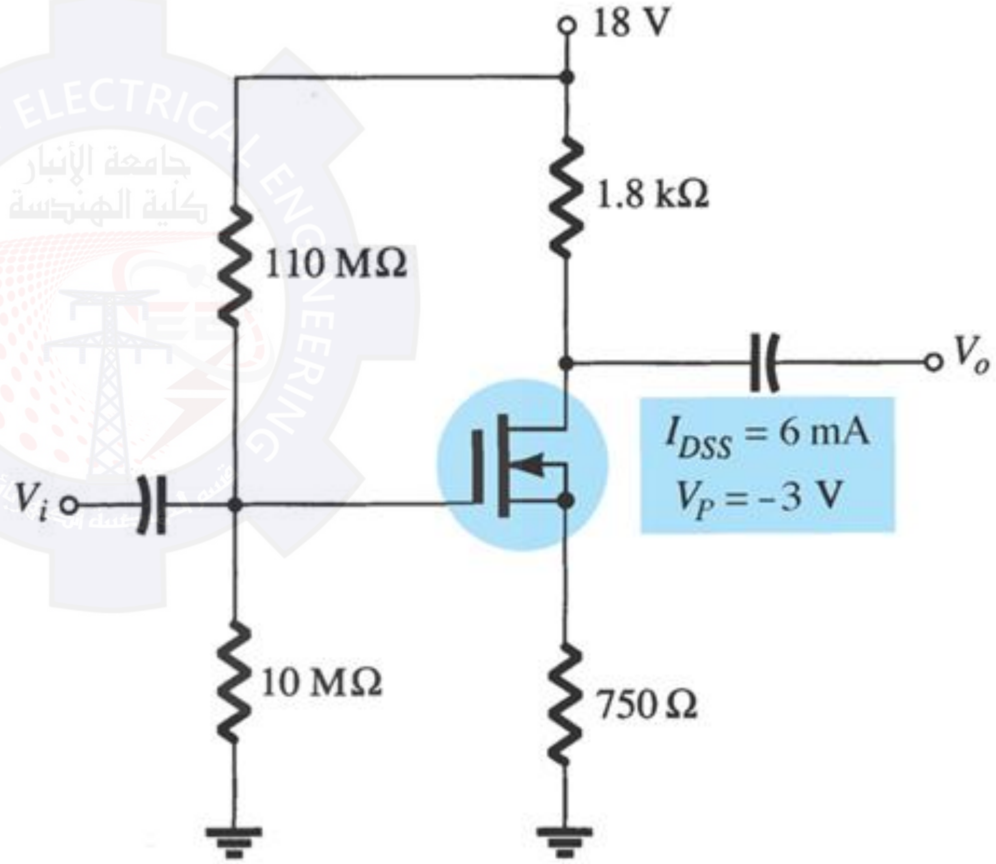
Find V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S.



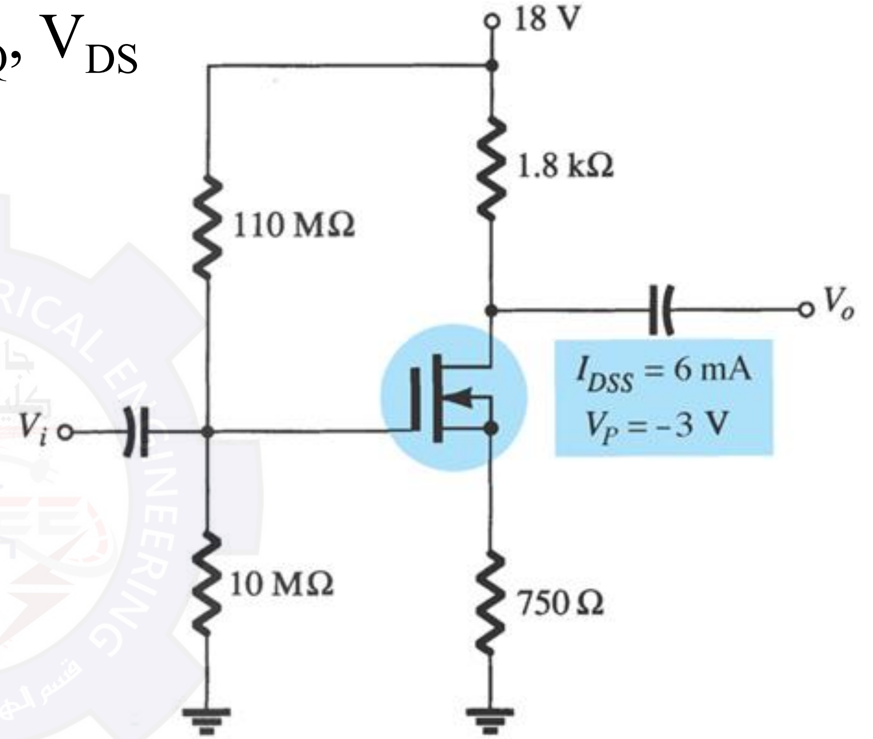


D-Type MOSFET Bias Circuits

Depletion-type MOSFET bias circuits are similar to those used to bias JFETs.
The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.



Example 7.7 Find V_{GSQ}, I_{DQ}, V_{DS}



Step 1

Plot the line for

- $V_{GS} = V_G$, $I_D = 0$ A
- $I_D = V_G/R_S$, $V_{GS} = 0$ V

Step 2

Plot the transfer curve using I_{DSS}, V_P and calculated values of I_D.

Step 3

The Q-point is located where the line intersects the transfer curve is. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

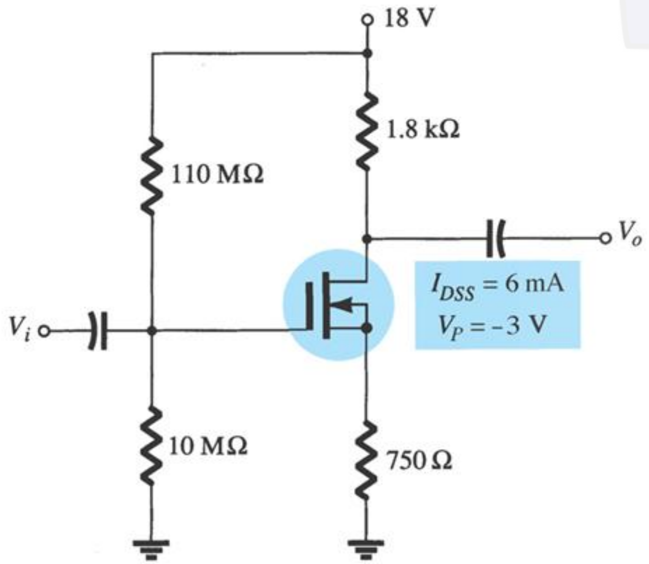
These are the same steps used to analyze JFET voltage-divider bias circuits.

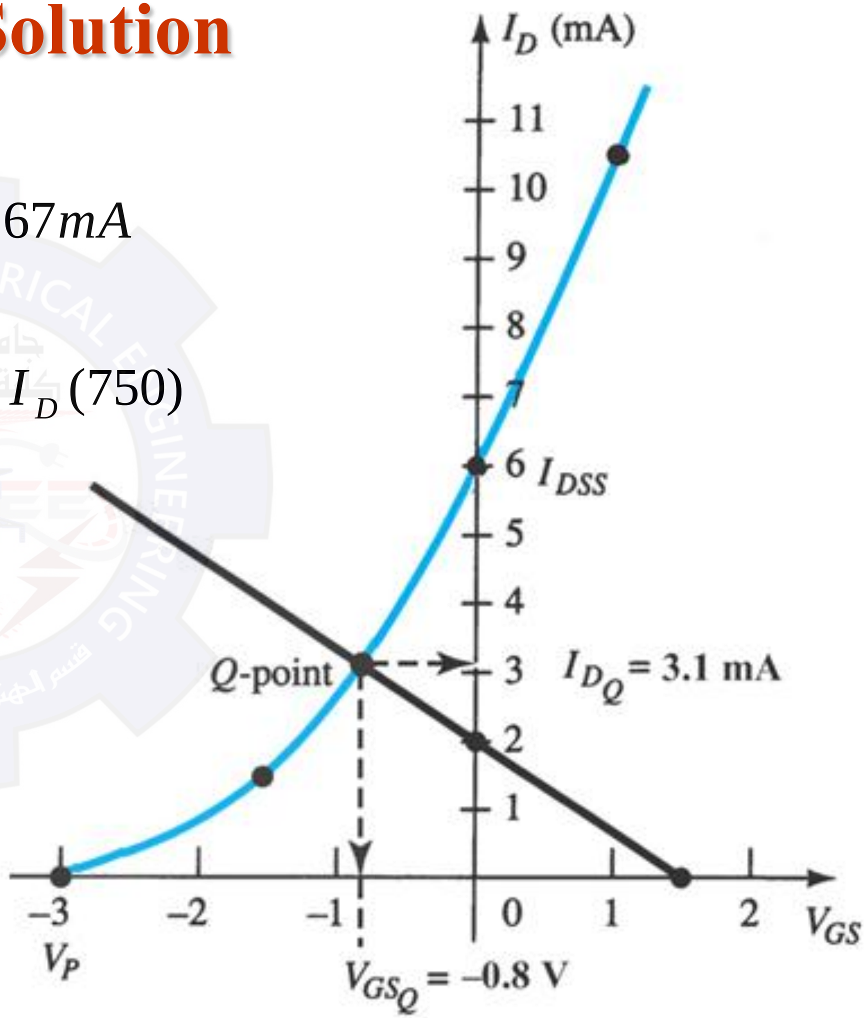
Example 7.7 - Solution

$For \ V_{GS} = +1V$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 = 6\text{mA}\left(1-\frac{+1}{-3}\right)^2 = 10.67mA$$

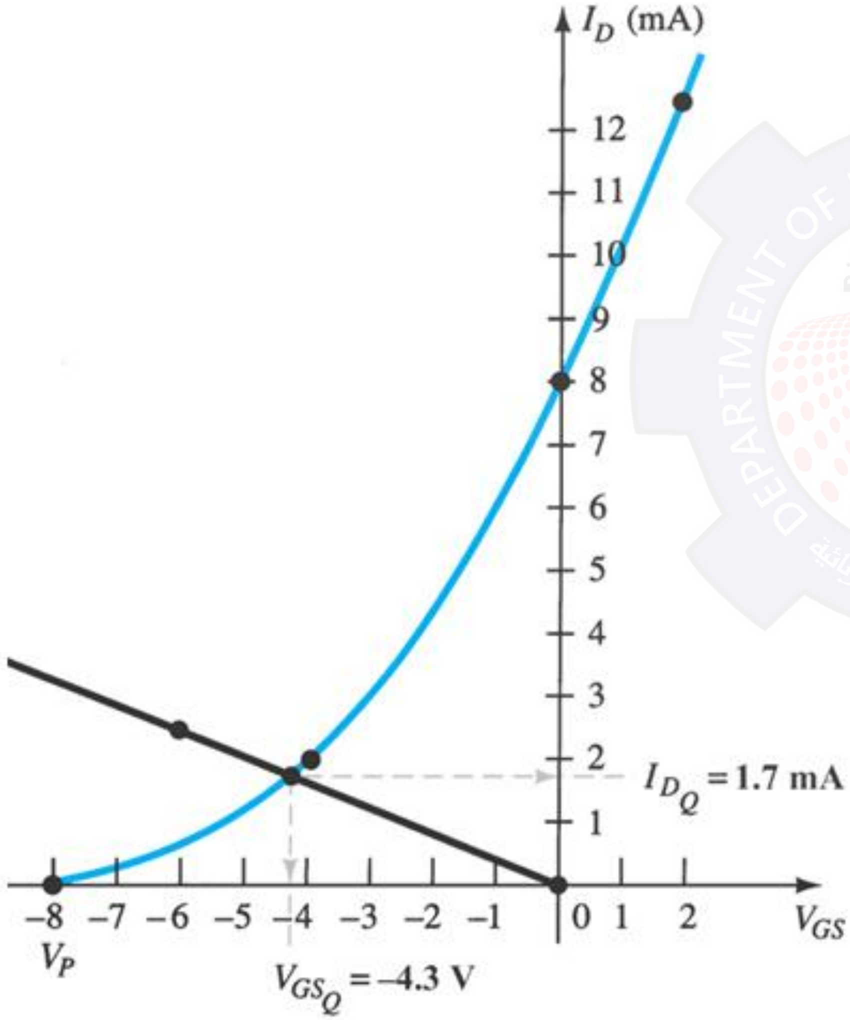
$$V_G = \frac{10M\,(18V)}{10M + 110M} = 1.5V \rightarrow V_{GS} = 1.5V - I_D(750)$$

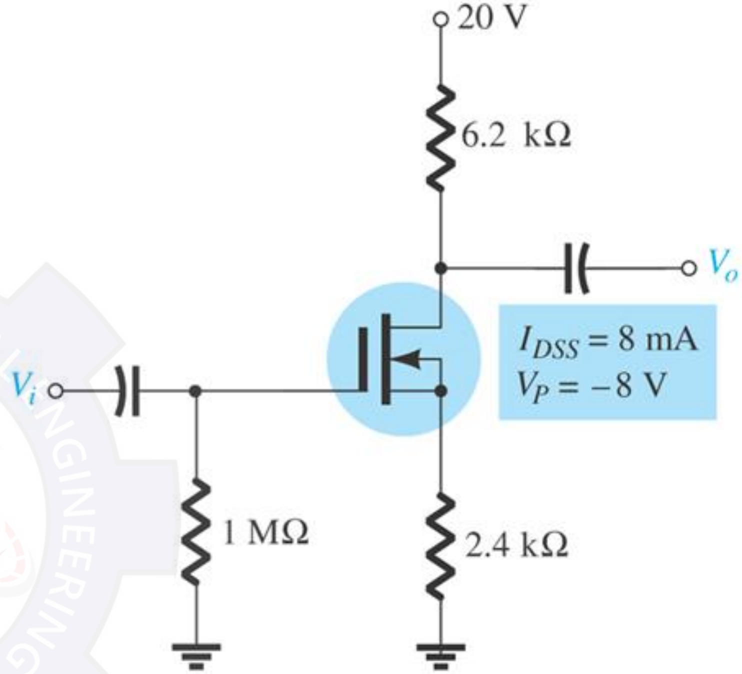




$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad V_{GS} = V_G - I_D R_S$$

Example 7.9 Find V_{GSQ}, I_{DQ}, V_D





To plot line $V_{GS} = -I_D R_S$:

$$I_D = -V_{GS} / R_S$$

$$For\ V_{GS} = -6,\ I_D = -(-6)/2.4k = 2.5mA$$

To plot transfer curve for V_{GS}=+2V:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 8m\left(1 - \frac{+2}{-8}\right)^2 = 12.5mA$$