



Experiment #2- Part#1

Transistor DC Biasing Circuits

Object

The purpose of this experiment is to determine the DC operating point (Q-point) for the transistor fixed-bias circuit, and the voltage divider bias circuit, and also to compare between their bias stabilities against changes in the transistor beta.

Required Parts and Equipment's

1. Electronic Test Board. (M90, M100)
2. DC Power Supply.
3. Digital Multi-meters.
4. NPN Transistors (BC337).
5. Resistors.M90 (470k Ω , 1.74K Ω), M100(39K Ω ,3.3K Ω ,4.7K Ω ,470 Ω)
6. Leads and Wires.

Theory

The analysis or design of a transistor amplifier requires knowledge of both the DC and the AC response. The analysis or design of any amplifier therefore has two components: the DC portion and the AC portion. In fact, the improved output AC power level is the result of a transfer of energy from the applied DC supplies.

The term biasing refers to the application of DC voltages to establish a fixed level of current and voltage. For transistor amplifier, the resulting DC current and voltage establish an operating point on the characteristics that define the region that will be employed for the amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (Q-point). The biasing circuit should be designed to set the device operation at a Q-point within the active region. For the BJT to be biased in the active region, the following must be verified:

1. The base-emitter junction must be forward-biased, with a resulting forward-bias voltage of about 0.6 to 0.7V.

2. The base-collector junction must be reverse-biased, with the reverse-bias voltage being any value within the maximum limits of the device.

▪ The Fixed-Bias Circuit

The Fixed-Bias circuit of Fig.1 is the simplest DC bias configuration.

In the base-emitter loop, applying KVL yields:

$$V_{CC} = I_B \cdot R_B + V_{BE}$$

Solving for I_B , we have:

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

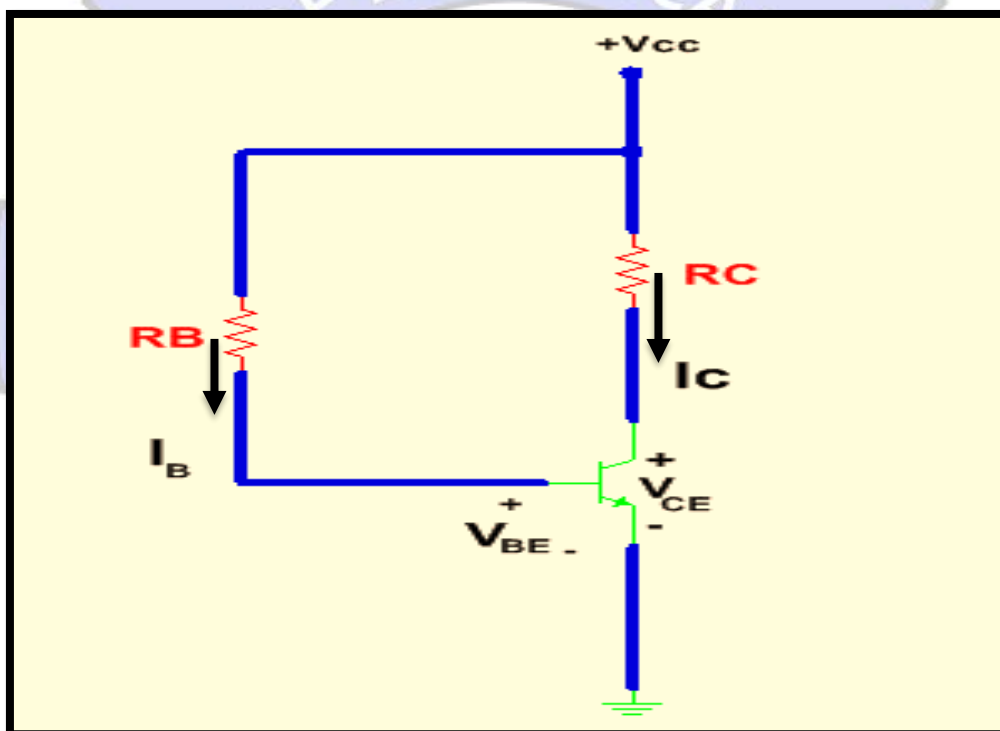


Figure 1: The Fixed -Bias Transistor Circuit

The collector current is related to base current by:

$$I_{CQ} = \beta \cdot I_{BQ}$$

Therefore,

$$I_{CQ} = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$



In the collector-emitter loop, we have:

$$V_{CC} = V_{CEQ} + I_{CQ} \cdot R_C$$

Solving for V_{CE} yields:

$$V_{CEQ} = V_{CC} - I_{CQ} \cdot R_C$$

The transistor operating point is I_{CQ} , V_{CEQ} .

To sketch the DC load line, the saturation and cut-off limits should be obtained.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE(off)} = V_{CC}$$

Although the fixed-bias circuit is very simple in construction, it has poor stability, and the Q-point may change or shift considerably if the transistor parameters (β and V_{BE}) change with temperature. This will result in change in the characteristics of the amplifier circuit.

The value of V_{BE} can be taken as 0.7V theoretically for silicon transistors. However, the measured practical value may be slightly different from the theoretical value.

▪ The Voltage-Divider Bias Circuit

In the fixed bias circuit, the bias current I_{CQ} and voltage V_{CEQ} are functions of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, this may result in change in bias current and voltage. Therefore, it would be desirable to develop a bias circuit that is independent of the transistor beta. The voltage divider circuit shown in Fig.2 is such a circuit. Voltage-Divider bias circuit is often used because the base current is made small compared to the currents through the two base (voltage-divider) resistors. Consequently, the base voltage and therefore the collector current are stabilized against changes in the transistor beta.

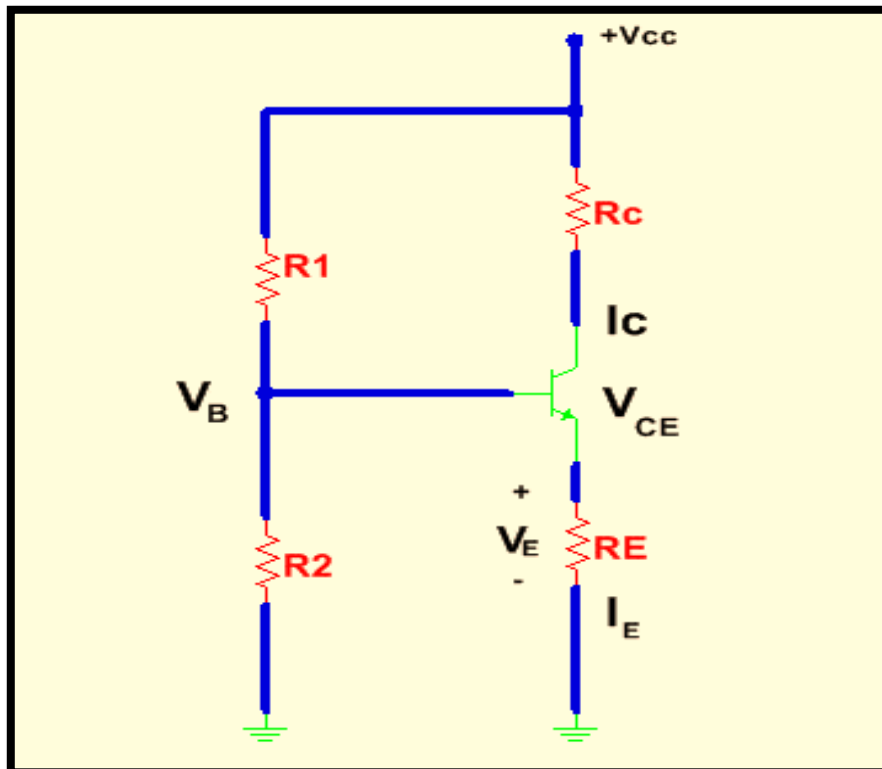


Figure 2: The Voltage-Divider Bias Circuit

The approximate analysis of the voltage divider bias circuit can be established by neglecting the base current I_B when compared to the current flowing in resistor R_2 . This is justified by assuming that the input resistance seen from the base is much greater than R_2 ($R_i = \beta \cdot R_E \gg R_2$). Thus, the necessary condition for the approximate analysis of the circuit is:

$$\beta \cdot R_E \geq 10R_2$$

In this case, the base voltage is given by:

$$V_B = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

The DC emitter voltage is given by:

$$V_E = V_B - V_{BE}$$

Quiescent DC collector current can be found from:

$$I_{CQ} \cong I_{EQ} = \frac{V_E}{R_E}$$



Collector voltage is found as:

$$V_C = V_{CC} - I_{CQ} \cdot R_C$$

The quiescent DC collector-to-emitter voltage is calculated from:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

The collector saturation current in this case is given by:

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C + R_E}$$

$V_{CE(sat)}$ is approximately equal to 0.2V for silicon transistors. The collector-emitter voltage at cut-off is:

$$V_{CE(off)} = V_{CC}$$

