University of Anbar
College of Engineering
Dept. of Electrical Engineering

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Experiment no.: 2
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Experiment #2- Part#2

Transistor DC Biasing Circuits

Procedure

1. Connect the circuit shown in Fig.3. Use the NPN transistor BC337 in (M90).

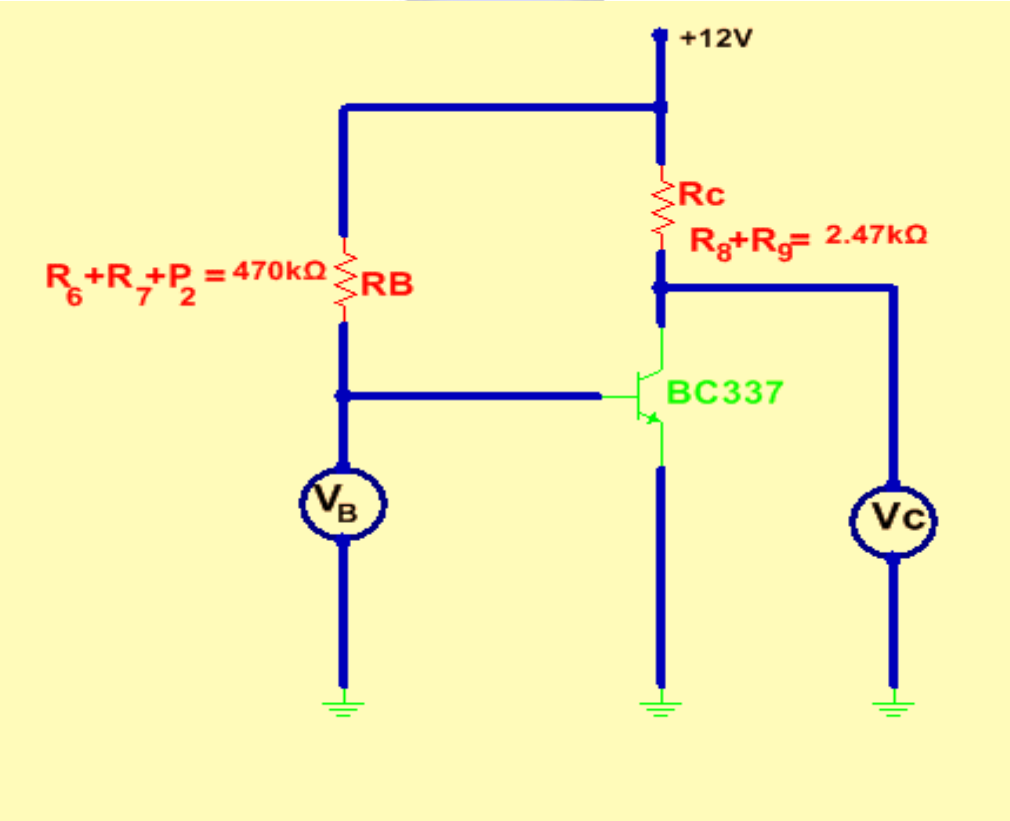

Figure 3: Practical Fixed Bias Transistor Circuit

2. Measure the DC voltages V_C and V_B using digital multi-meters. Determine the quiescent base current, collector current, and collector- emitter voltage, where:

$$I_{BQ} = \frac{V_{CC} - V_B}{R_B}$$

$$I_{CQ} = \frac{V_{CC} - V_C}{R_C}$$

$$V_{CEQ} = V_C$$

$$V_{BEQ} = V_B$$

3. Measure the transistor current gain as follows:

$$\beta_{dc} = \frac{I_{CQ}}{I_{BQ}}$$

4. Calculate the expected values of I_{BQ}, I_{CQ}, and V_{CEQ}. Use the value of β determined in step 3 above. Assume that V_{BE} = 0.7 theoretically. Tabulate you results as shown in Table 1.

Transistor 1 BC337		
Quantity	Measured	Calculated
V_B		
V_C		
V_{BEQ}		
V_{CEQ}		
I_{BQ}		
I_{CQ}		
V_{CEQ}		
β_{dc}		

Table 1: Measured and Calculated Transistor Parameters for the Fixed Bias Circuit

5. Connect the voltage-divider bias circuit shown in Fig.4. (use npn transistor in (M100)).

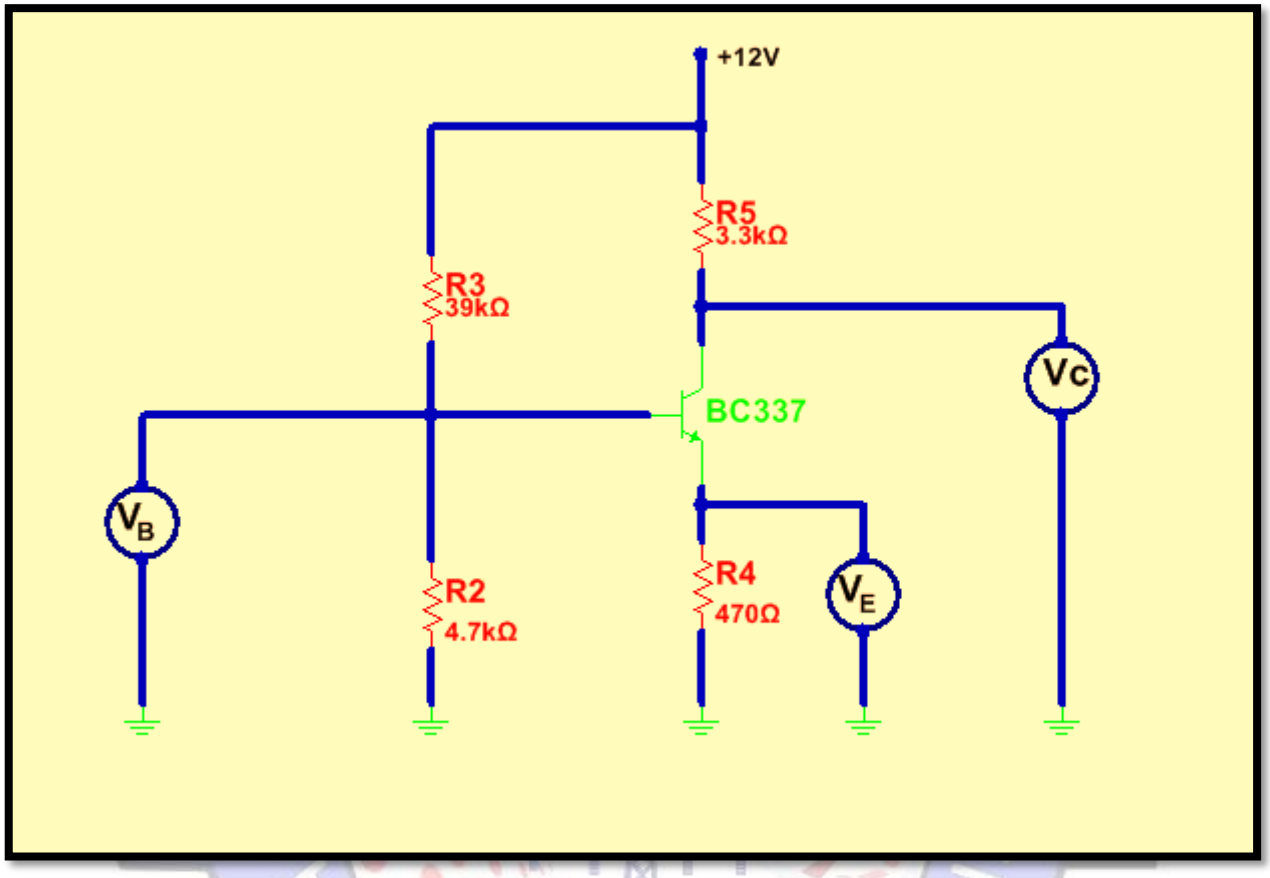

Figure 4: Practical Voltage-Divider Transistor Bias Circuit

6. Measure the DC voltages V_B, V_E, and V_C using digital multi-meters. Determine the quiescent point of the transistor as follows:

$$I_{CQ} \cong I_{EQ} = \frac{V_E}{R_E}$$

$$V_{CC} = V_{CEQ} + I_{CQ}.R_C$$

$$V_{CEQ} = V_{CC} - I_{CQ}.R_C$$

Discussion

1. Perform the theoretical calculations to determine the Q-point for both circuits and for each transistor, and compare them with the measured values.
2. Determine the drift in the Q-point for the two biasing circuits and therefore compare their bias stabilities.
3. Sketch the DC load line for the fixed bias circuit for each transistor case and place the Q-point on it.
4. Sketch the DC load line for the voltage divider bias circuit for each transistor case and place the Q-point on it. Is there a difference between the load lines in this case?
5. What is the effect of increasing resistor R_2 in the voltage-divider bias circuit on I_{CQ}? How should we select its practical value for better stability considerations?
6. What is the effect of decreasing resistor R_B on I_{CQ} for the fixed – bias circuit? What is its minimum value to ensure that the transistor is working in the active region?
7. For the fixed bias circuit of Fig.3, if the minimum β of the transistor is specified in the datasheet as 50, and the maximum value is 250, then determine the range of the Q-point of the transistor.
8. Sketch the circuit diagram of the collector-feedback bias circuit and compare its stability with that of the voltage-divider bias circuit.