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Experiment #3- Part#2

Logic Gate Circuits

- **The NOT Gate Circuit**

The NOT gate has a single input and output. The output equals the inverse of the input or the complement of the input. Fig.6 shows the symbol for the NOT gate, which is also called an inverter.

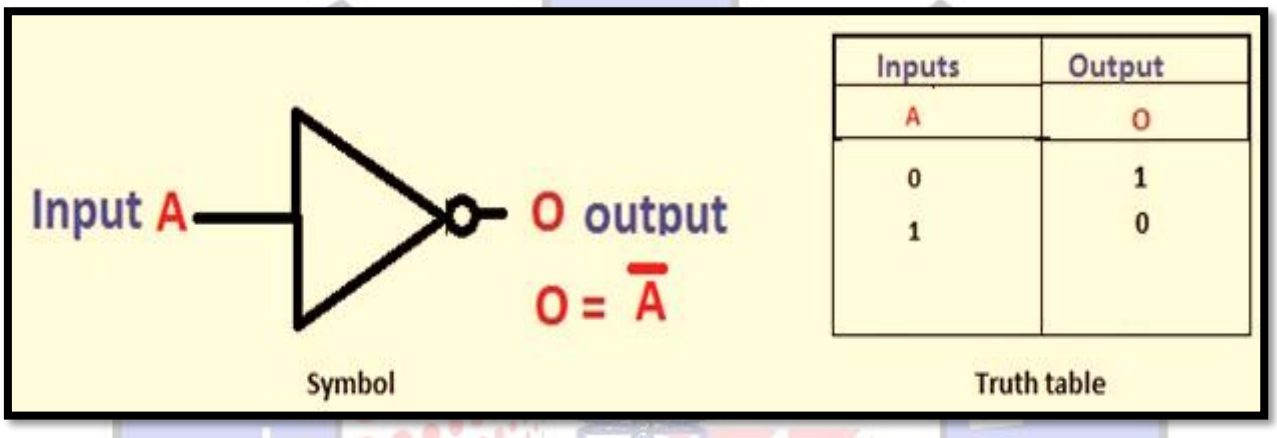


Figure 6: The Logic Symbol and Truth Table for the NOT Gate

The most widely used inverter circuit uses a bipolar transistor in the common-emitter configuration as shown in Fig.7. The input signal is applied to the base and the output is taken from the collector.

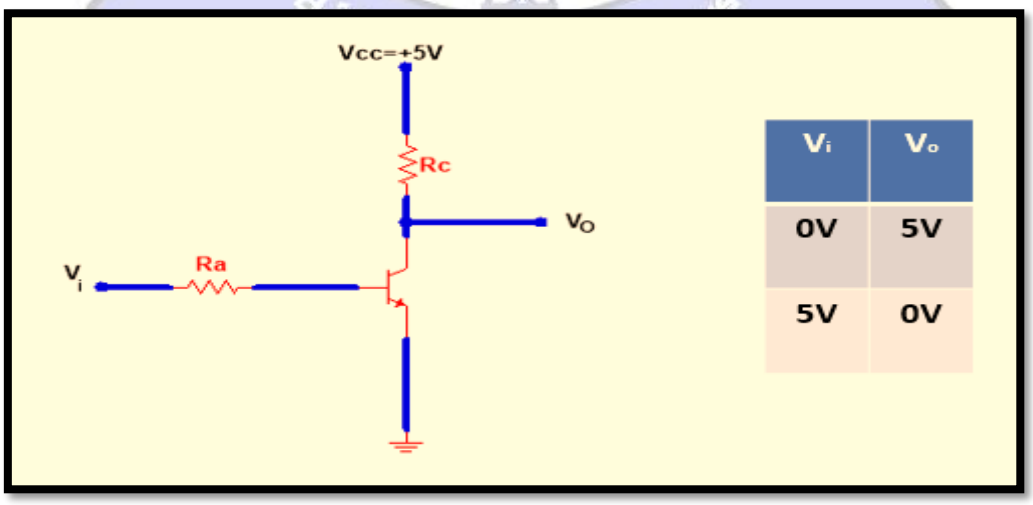


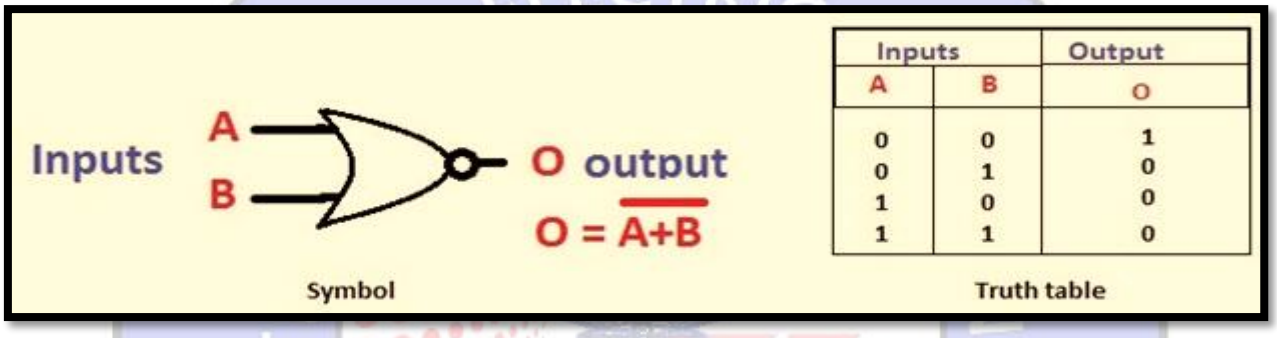
Figure 7: Transistor Inverter Circuit

The circuit operates so that when V_i = 0V, the transistor is OFF. Therefore, I_C is zero and no current flows through R_C. This means that the voltage drop across R_C is zero and the collector is at +5V above ground, producing V_0 = 5V.

When V_i = 5V, the transistor becomes ON and enters the saturation region when I_B is large enough. So, the collector voltage will be $V_{CE\,(sat)}$, and this produces $V_0 = V_{CE\,(sat)} \approx 0V$.

- **The NOR Gate Circuit**

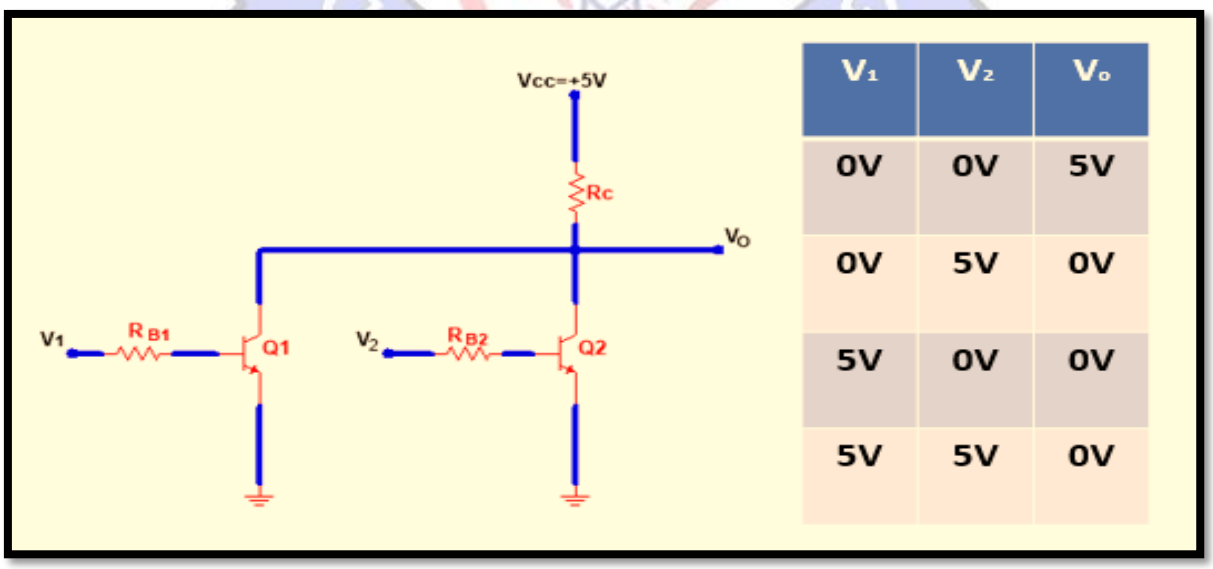
Figure 8 shows the logic symbol for a two-input NOR gate. The operation of the NOR gate is equivalent to the OR gate followed by an inverter.



Inputs		Output
A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

Figure 8: The Logic Symbol and Truth Table for the NOR Gate

Figure 9 shows a practical electronic circuit for implementing the NOR gate. It consists of two transistors connected in parallel.



V_1	V_2	V_o
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

Figure 9: The NOR Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are in the cut-off region (OFF), and hence no current flows in resistor R_C. Therefore, the output voltage V_0 equals V_{CC} and is +5V.When $V_1=0$ and $V_2=5V$, transistor Q_1 will be OFF and transistor Q_2 will now be ON and enters the saturation

region. In this case, the current will flow in R_C through transistor Q_2. The output voltage will equal the saturation voltage of Q_2 and is approximately 0V ($V_o = V_{CE2(sat)} \approx 0V$).

When $V_1 = 5V$ and $V_2 = 0V$, the situation will be opposite to the previous case and $V_o = V_{CE2(sat)} \approx 0V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will conduct, and the output voltage will equal the saturation voltage of the transistors and hence is approximately 0V ($V_o = V_{CE\,(sat)} \approx 0V$).

- **The NAND Gate Circuit**

Figure 10 shows the logic symbol and the truth table of a two-input NAND gate. The operation of the NAND gate can be understood as being constituted from an AND gate followed by an inverter.

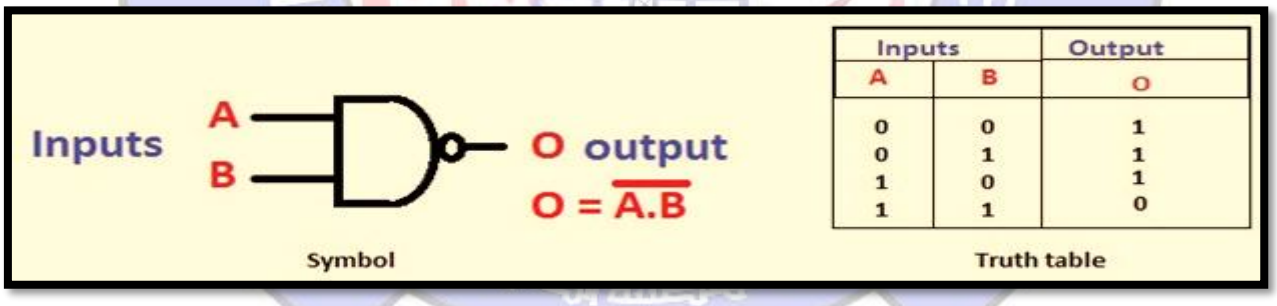
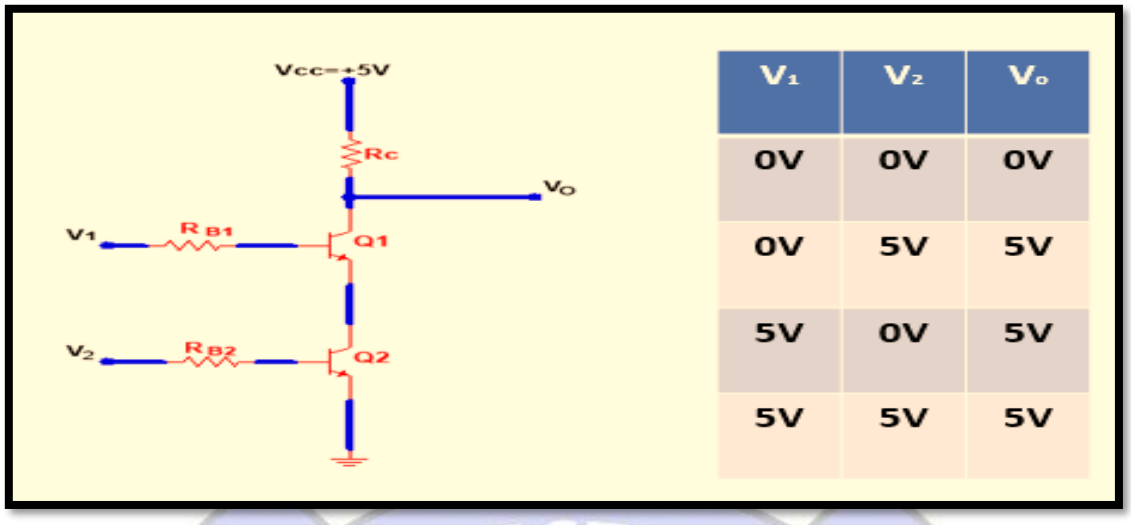


Figure 10: The Logic Symbol and Truth Table for the NAND Gate



V_1	V_2	V_o
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

Figure 11: The NAND Gate Circuit

When $V_1 = V_2 = 0V$, both transistors are OFF and no-current flows through RC and therefore $V_o = V_{CC} = 5V$. When $V_1=0$, and $V_2=5V$ transistor Q_2 will be ON, but Q_1 is OFF, and therefore no-current will flow through resistor R_C and V_0 is HIGH and equals 5V. In the third case, when $V_1 = 5V$, and $V_2= 0V$, transistor Q_1 becomes ON and Q_2 will be OFF and no current flows through R_C, and hence $V_0 = V_{CC} = 5V$.

Finally, when $V_1 = V_2 = 5V$, both transistors will be ON and enter the saturation region. So, $V_0 = 2Vsat \approx 0V$ and will be LOW.