



## Experiment #4- part#1

### Small Signal BJT Amplifier

#### Object

The purpose of this experiment is to demonstrate the operation of the small signal common emitter amplifier and investigate the factors influencing the voltage gain as well as to determine the input and output impedances.

#### Required Parts and Equipment's

1. Electronic Test Board. (M100)
2. Function Generator
3. DC Power Supply.
4. Two-channel Oscilloscope
5. DC Multimeter
6. BC 337 NPN silicon Transistors.
7. Resistors  $R_L=10K\Omega$ ,  $R_2=4.7K\Omega$ ,  $R_3=39K\Omega$ ,  $R_C= R_5=3.3K\Omega$ ,  $R_{test}=(P_2)$   
 $P_2=R_{E2}=1K\Omega$ ,  $R_{E1}=R_4=470\Omega, 120\Omega$
8. Capacitors  $2.2 \mu F$  and  $10 \mu F$ .  $C_1=100nf$ ,  $C_2=C_E=1\mu f$ ,  $C_3=100nf$

#### Theory

The common-emitter amplifier is characterized by the application of the input signal to the base lead of the transistor while taking the output from the collector, which always gives  $180^\circ$  phase shift between the input and output signals. Figure 1 presents a schematic diagram for a typical common-emitter amplifier using the voltage-divider bias configuration.

The DC coupling capacitors  $C_{in}$  and  $C_{out}$  are used to block the DC current and thus to prevent the source internal resistance and the load resistance  $R_L$  from changing the DC bias voltages at the base and collector. Capacitor  $C_E$  is a bypass capacitor for the emitter resistor  $R_E$ . Resistor  $R_{E2}$  is used for bias stability, while  $R_E$  is used to minimize the change in the emitter internal AC resistance  $r_e$  due to temperature effects, and thereby to obtain a stable voltage gain.

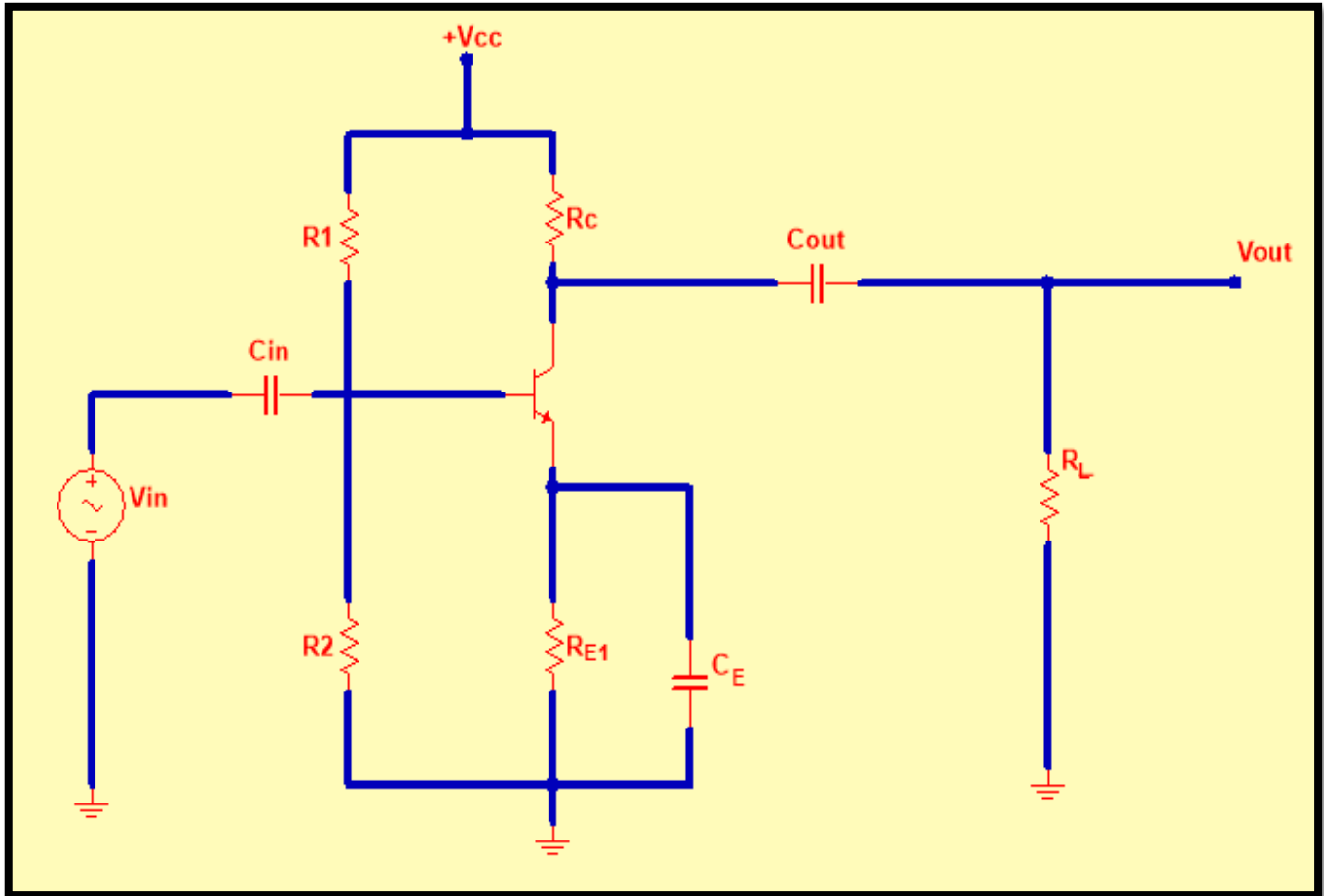


Figure 1: Schematic Diagram for a Typical Common Emitter Amplifier Circuit

The base DC voltage can be calculated approximately from the following equation assuming that  $\beta \cdot (R_{E1}) \gg R_2$ :

$$V_B = \frac{R_2 + V_{CC}}{R_1 + R_2} \quad (1)$$

The emitter DC voltage is therefore:

$$V_E = V_B - V_{BE} \quad (2)$$

The emitter DC bias current can be obtained as:

$$I_{EQ} = \frac{V_E}{R_E} \cong I_{CQ} \quad (3)$$

Transistor AC emitter resistance is obtained from:

$$r_e = \frac{V_T}{I_{EQ}} \quad (4)$$

Where  $V_T = 26 \text{ mV}$  at room temperature.

The quiescent DC collector-emitter voltage is calculated from:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) \quad (5)$$

### • Voltage Gain Analysis

Figure 2 presents the AC small-signal equivalent circuit for the common emitter amplifier. From this circuit, the amplifier voltage gain can be found as:

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{R_C \parallel R_L}{R_E + r_e} \quad (6)$$

If the load resistor  $R_L$  is removed then the voltage gain will become:

$$A_v = -\frac{R_C}{R_E + r_e} \quad (7)$$

On the other hand, if the bypass capacitor  $C_E$  is removed, then the voltage gain will be modified as:

$$A_v = -\frac{R_C \parallel R_L}{R_E + r_e} \quad (8)$$

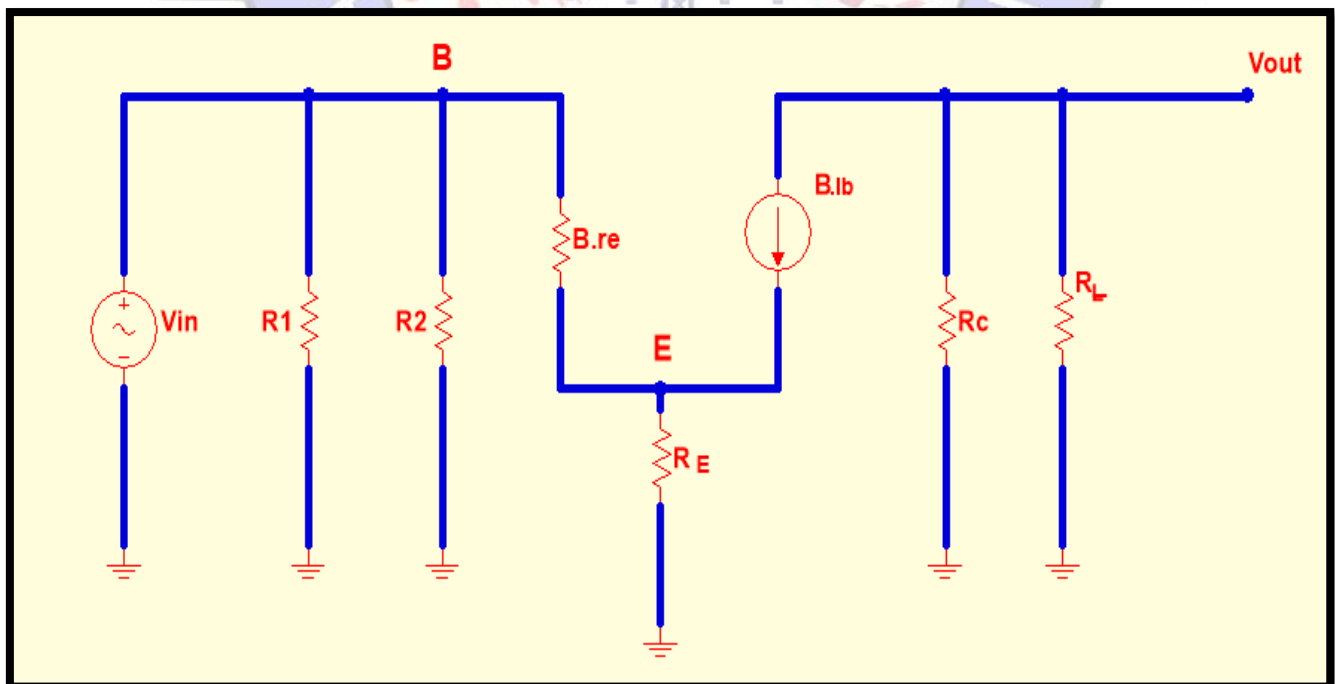


Figure 2: The Small-Signal AC Equivalent Circuit for the Common Emitter Amplifier

• **AC Load Line and Maximum Symmetrical Swing**

The AC load line of the amplifier circuit can be sketched to predict the swing of the output voltage and collector current. Figure 2 shows the AC and DC load lines of the circuit.

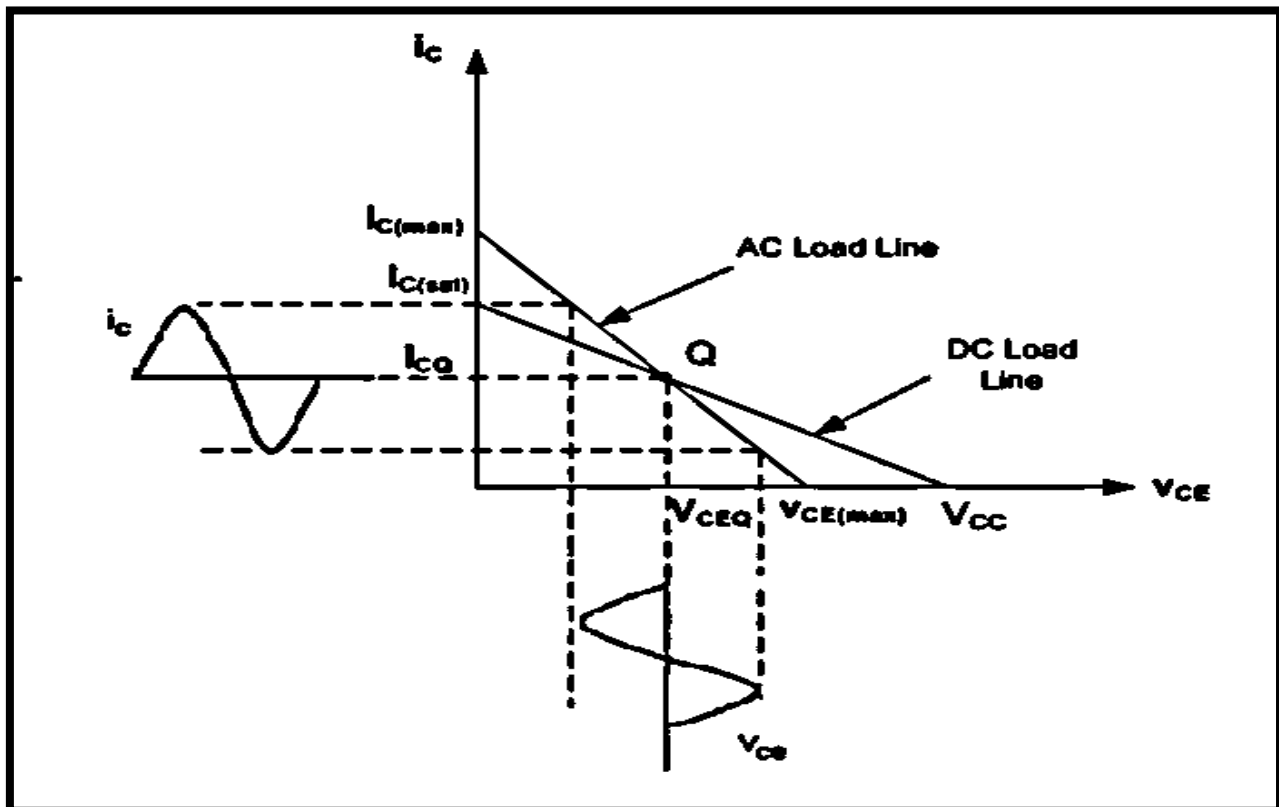


Figure 3: DC and AC Load Lines and Collector Current and Voltage Swing

As shown in Fig.2, both load lines intersect at the Q-point of the transistor. The slope of the AC load line is equal to  $-1/R_{ac}$ , where  $R_{ac}$  is the AC equivalent resistance seen between the collector and emitter terminals.  $R_{ac}$  can be obtained from the amplifier's small signal equivalent circuit of Fig.2. The total collector current and voltage can be expressed as the sum of the quiescent values and the AC signal quantities as shown below:

$$i_c = I_{CQ} + i_c \tag{9}$$

$$v_{ce} = V_{CEQ} + v_{ce} \tag{10}$$

It can be shown that  $i_{C(max)}$  and  $v_{CE(max)}$  in Fig.3 are given by:



$$i_{C(\max)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \quad (11)$$

$$v_{CE(\max)} = V_{CEQ} + I_{CQ} \cdot R_{ac} \quad (12)$$

Where:

$$R_{ac} = R_E + R_C \parallel R_L \quad (13)$$

Maximum symmetrical swing in the output signal can be obtained if the Q-point bisects the AC load line. The AC load line concept can be used to predict the maximum amplitude in the output signal before clipping.

### • Input and Output Impedances

The input and output impedances of the amplifier can be found theoretically as the Thevenin equivalent impedances at the input and output terminals respectively. For the equivalent circuit of Fig.2, the input impedance ( $Z_{in}$ ) of the amplifier seen by the source is:

$$Z_{in} = R_1 \parallel R_2 \parallel \beta(r_e + R_E) \quad (14)$$

Similarly, the output impedance ( $Z_{out}$ ) seen from the output terminals is:

$$Z_{out} = R_C$$

The amplifier circuit can be represented as a two-port network as illustrated in Fig.4. In this figure,  $A_{vo}$  represents the no-load voltage gain of the amplifier,  $Z_{in}$  is the amplifier's input impedance, and  $Z_{out}$  is the amplifier's output impedance. Resistor  $R_s$  is the internal resistance of the signal source, while  $R_L$  is the load resistance.

The overall voltage gains of the amplifier taking the effects of  $R_s$  and  $R_L$  into account can be expressed as:

$$A_v = \frac{v_{in}}{v_s} \cdot \frac{v_{out}}{v_{in}}$$

$$A_v = \frac{Z_{in}}{Z_{in} + R_s} \cdot \frac{A_{vo} \cdot R_L}{R_L + Z_{out}} \quad (16)$$

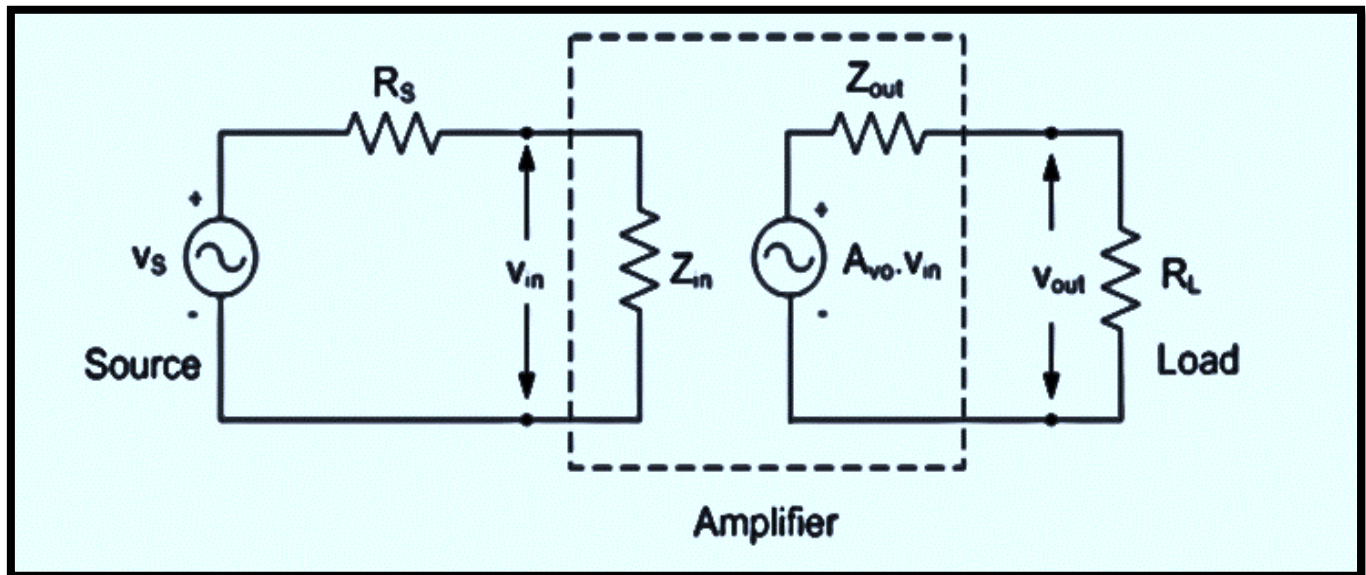


Figure 4: The Amplifier as a Two-Port Network

For the input port, when  $R_s = Z_{in}$ , we have:

$$v_{in} = \frac{Z_{in}}{Z_{in} + R_s} v_s = \frac{1}{2} v_s$$

Assuming that the amplifier is connected with no-load, we have:

$$A_v = \frac{v_{in}}{v_s} \cdot \frac{v_{out}}{v_{in}} = \frac{1}{2} A_{vo}$$

Thus, the input impedance can be estimated practically by inserting a variable source resistor  $R_s$  in series with the source and varying it until the voltage gain of the amplifier equals half the no-load gain  $A_{vo}$ . This value of  $R_s$  represents the input impedance  $Z_{in}$ .

For the output port, when  $R_L = Z_{out}$ , and assuming that  $R_s = 0$ , then we have:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{A_{vo} \cdot R_L}{R_L + Z_{out}} = \frac{1}{2} A_{vo}$$

So that the output impedance can be estimated practically by connecting a variable load resistor  $R_L$  and varying it until the voltage gain becomes equal to half the value of the no-load gain with  $R_s = 0$ . This value of  $R_L$  represents the output impedance  $Z_{out}$ .