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Experiment no.: 7
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Experiment #6- Part-1

The FET Common Source Amplifier

Object

The purpose of this experiment is to test the performance of the common source amplifier using the self-bias circuit.

Required Parts and Equipment's

1. Electronic Test Board. (M110)
2. Dual Polarity Variable DC Power Supply
3. Digital Multimeters.
4. Dual-Channel Oscilloscope.
5. Function Generator.
6. N-Channel JFET 2N3823
7. Resistors, R_5=100KΩ, R_6=10KΩ, R_8=1KΩ, R_7=2.2KΩ

Theory

The common source amplifier configuration is widely used amongst other JFET configurations and can provide both high voltages gain and large input impedance. In this configuration, the input signal is applied to the gate and the output signal is taken from the drain, while the source terminal being the reference or common. In order to work as an amplifier, the JFET should be properly biased by setting the gate-source voltage which results in the required drain current.

The N-channel JFET requires that the gate-source voltage always be less negative than the pinch-off voltage, but less than zero. Since virtually no gate current flows due to the JFET's high input impedance, the gate voltage is essentially at ground level. Consequently, using only a drain-supply voltage, the required negative quiescent gate-source voltage is developed by the voltage drop across the source resistor of the self-bias circuit shown in Fig.1. This circuit is one of the simplest and practical bias circuits for JFET amplifiers in which a single power supply is used.

In this circuit, the gate voltage is zero.

$$V_G = 0 \quad \text{.....(1)}$$

Thus, the gate-source voltage is given by:

$$V_{GS} = -I_D R_S \quad \text{.....(2)}$$

Where the drain current is given by:

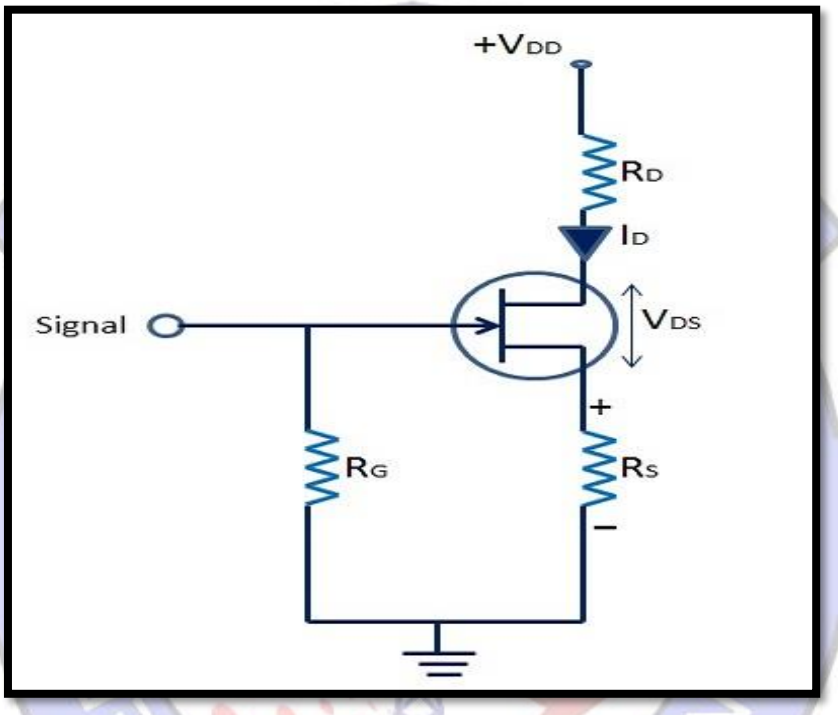

Figure 1: The Self-Bias JFET Circuit

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....(3)}$$

Solving equations (2) and (3) simultaneously will give both I_{DQ} and V_{GSQ}.

The drain-source voltage is given by:

$$V_{DS} = V_{DD} - I_D.(R_D + R_S) \quad \text{.....(4)}$$

A typical common-source amplifier circuit is shown in Fig.2. In this circuit, capacitors C_{c1} and C_{c2} are DC blocking capacitors, while C_S is a bypass capacitor for the source resistor R_S.

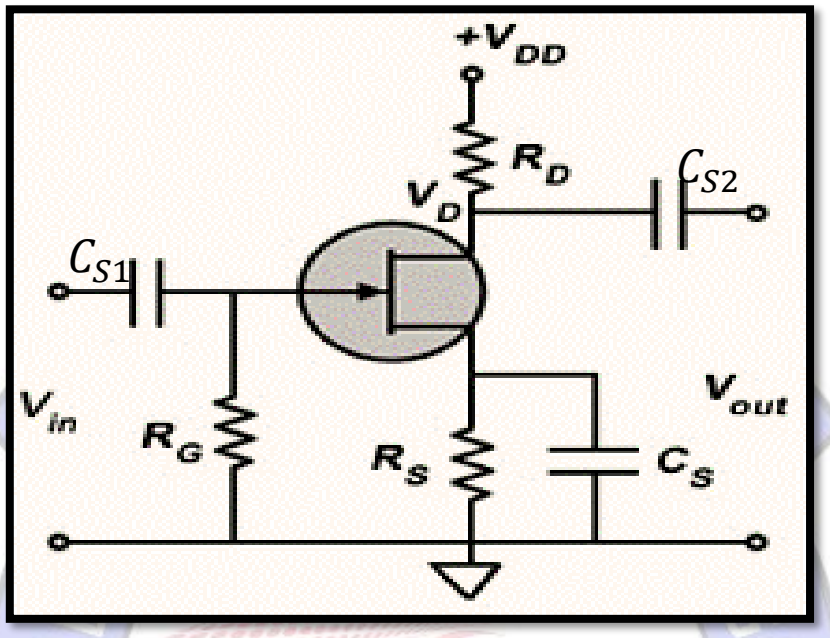

Figure 2: A Typical Common Source Amplifier

The small-signal approximate equivalent circuit for the amplifier of Fig.2 is presented in Fig.3.

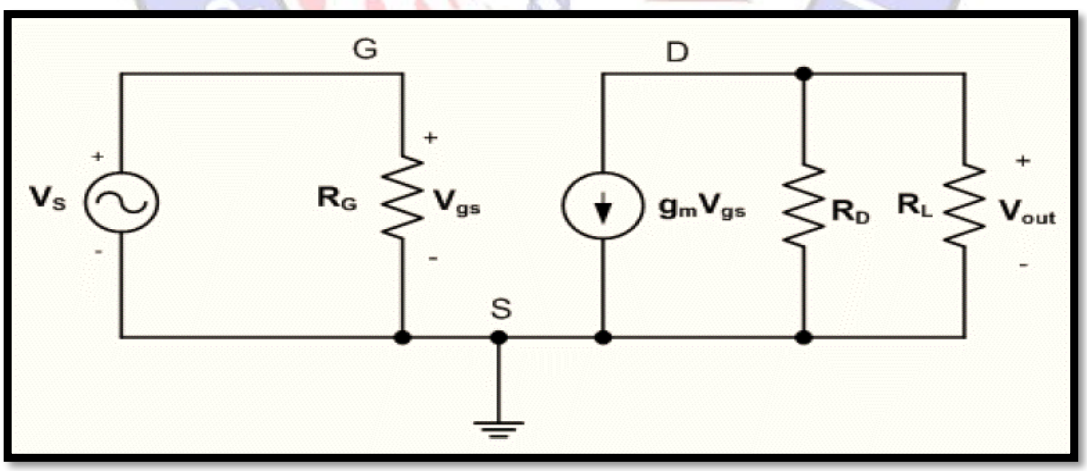

Figure 3: The Simplified Small-Signal Equivalent Circuit of the Amplifier

The transconductance of the JFET at the Q-point is derived as:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q-point} = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{.....(5)}$$

Where g_{mo} is given by:

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \quad \text{.....(6)}$$

The voltage gain of the amplifier can be derived from the equivalent circuit of Fig.4:

$$A_v = \frac{V_{out}}{V_S} = -g_m.(R_D \parallel R_L) \quad \text{.....(7)}$$

It can be shown that when the source bypass capacitor CS is removed, the voltage gain will become:

$$A_v = \frac{-g_m.(R_D \parallel R_L)}{1 + g_m.R_S} \quad \text{.....(8)}$$

The input impedance of the amplifier seen from the gate terminal is:

$$Z_{in} = R_G \quad \text{.....(9)}$$

And the output impedance seen from the output terminals is:

$$Z_{out} = R_D \quad \text{.....(10)}$$