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Experiment #6- Part#2

The FET Common Source Amplifier

Procedure

1. Connect the test circuit shown in Fig.4 to measure I_{DSS}. Increase the supply voltage until I_D no longer increases. This level of drain current is recorded as I_{DSS}.

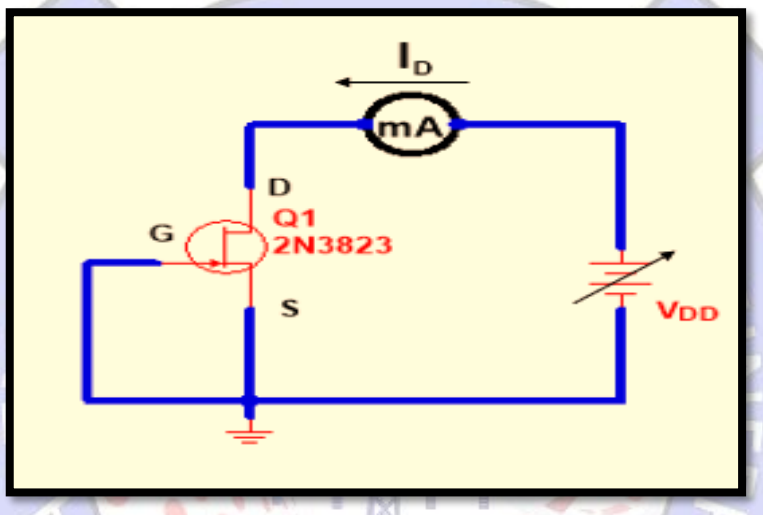

Figure 4: Test Circuit for Measuring I_{DSS}

2. Connect the test circuit shown in Fig.5 to measure V_P. The gate supply voltage V_{GG} is adjusted from 0 to larger negative values until the drain current I_D just reaches 0. The voltage V_{GS} to just cause the drain current to reach 0 is the measured value of V_P. Tabulate your results as shown in Table-1.

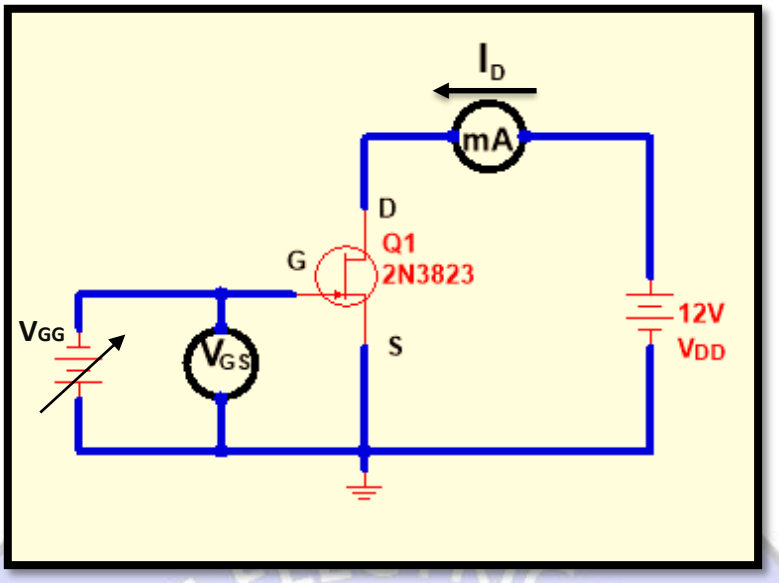

Figure 5: Test Circuit for Measuring V_P

Table-1: Measured JFET Parameters

Device Parameter	Value
I_{DSS}	
V_P	

3. Connect the JFET self-bias circuit shown in Fig.6 and measure the DC voltages V_G, V_S, and V_D with the aid of a digital multi-meter. Determine V_{GSQ}, I_{DQ}, V_{DSQ}, and g_m at the Q-point. Tabulate your results as illustrated in Table-2.

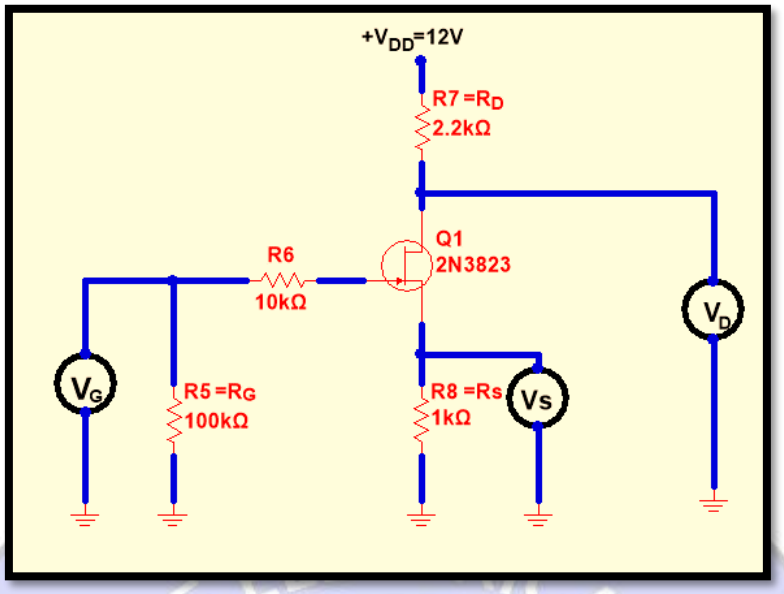

Figure 6: The Practical Bias Circuit of the Amplifier

4. Connect the amplifier circuit shown in Fig.7. Sketch the input (V_S) and output (V_D) signals and determine the voltage gain of the circuit in three cases as illustrated in Table-3.

Table-2: Measured Bias Circuit Parameters

Quantity	Value
V_G	
V_S	
V_D	
V_{GS}	
I_D	
V_{DS}	
g_m	

Table-3: Measured Voltage Gain Conditions

V_{in}	V_{out}	Voltage Gain (V_{out}/V_{in})
0.1V_{PP}		
0.15V_{PP}		
0.2V_{PP}		

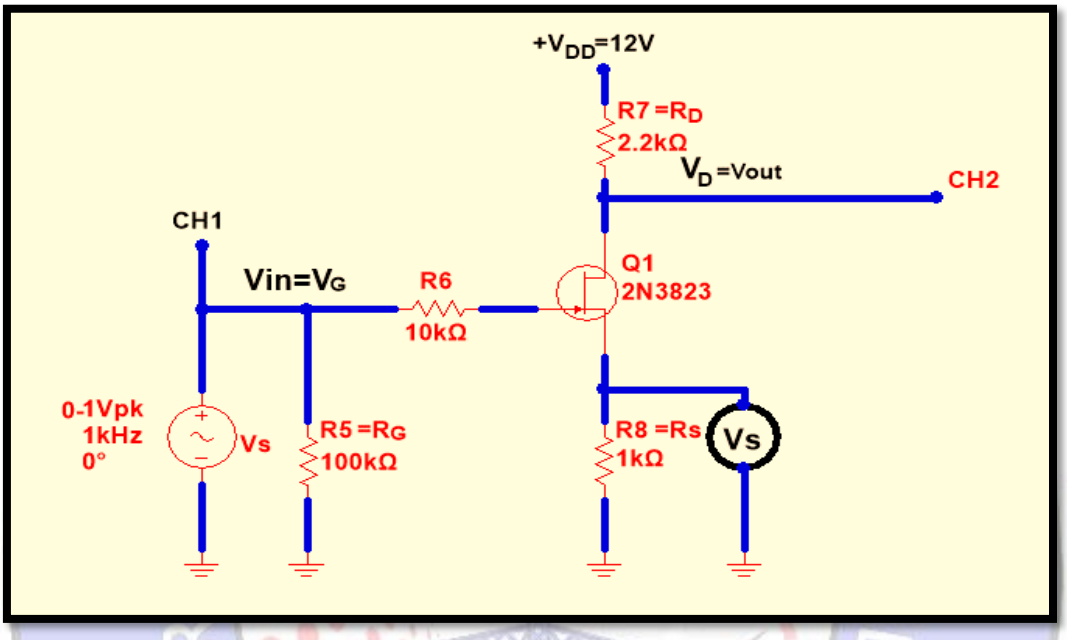

Figure 7: The Practical Common-Source Amplifier Circuit

Discussion

1. Using the measured device parameters I_{DSS} and V_P, calculate the theoretical Q-point values of I_{DQ} and V_{GSQ} and compare them with the measured quantities.
2. Indicate graphically the effect of increasing the source resistor R_S on the Q-point of the JFET.
3. Determine the DC power dissipation in the JFET connected in the amplifier circuit of Fig.7.
4. What is the effect of increasing the source resistance RS on the voltage gain of the amplifier circuit?