COMBINATIONAL LOGIC CIRCUITS EXPERIMENTS

Combinational logic circuits are constructed with basic logic gates. Its output will correspond only to the current input, previous inputs and outputs can't influence the current output. Therefore the output of any combinational logic circuits can be expressed by Boolean functions.

The major components of a combinational logic circuit includes Input Variables; Logic Gates and Output Variables. The input variable could be either higher or lower than the output variable but both are binary signals, or "0" and "1".

Assuming there are "n" input variables, there will be 2 possible input combinations, each with one corresponding output combination. Before designing and constructing a combinational logic circuit the following information should be taken into consideration:

1. Truth tables of logic gates
2. Boolean Function
3. Karnaugh Map
4. de Morgan's Theorem

The following combinational logic gates are used very often and they are discussed in this chapter, along with many other combinational logic gates.

1. Combinational logic circuits with NAND and NOR gates
2. AND-OR-INVERTER (A-O-I) gate
3. XOR gate
4. Open-collector gates
5. Tristate gate
6. Arithmetic circuits
7. Encoder and decoder circuits
8. Multiplexer and demultiplexer circuits
9. Comparator circuits

2-1 NOR Gate Circuit

OBJECTIVE

Understanding how to construct other combinational logic gates using NOR gates.

Summary

The symbol of a NOR gate is shown in Fig. 2-1. The Boolean expression for the NOR gate is F= $\overline{A+B}$; in de Morgan's theorem, F= $\overline{A+B}=\overline{A}\times\overline{B}$.

When A=B, F= $\overline{A+B}=\overline{A}$ +A= $\overline{A}$. When B=0, F= $\overline{A+B}=\overline{A+0}=\overline{A}$. Therefore, the NOR gate can be used to construct NOT; OR; AND; NAND; and XOR gates. We will attempt to construct various logic gates in this experiment by connecting NOR gates in different ways.

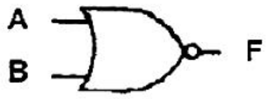


Fig. 2-1 Symbol of NOR gate

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Module KL-33002

PROCEDURES

1. U1a of Fig. 2-2 (a) will be used to construct a NOT gate.

2. Connect inputs A, B to Data Switches SW0, SW1 and output F1 to Logic Indicator L1. Set SW0 to "0", observe states of F1 at SW1="0" and SW1="1 ".

   Does the circuit act as a NOT gate? (as in Fig. 2-2 (b)?)

3. Insert a connection clip between A and B. Connect A to SW0 and F1 to L1. What is the state of F1 when SW0=0 and SW0=1?

   Does the circuit act as a NOT gate?

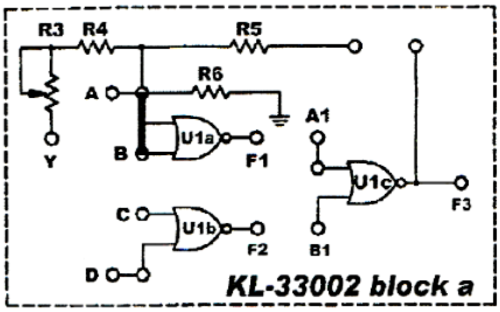


Fig. 2-2 (a)

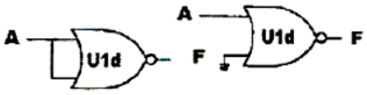


Fig. 2-2 (b) NOR gate used as NOT gate

4. Use U1a and U1c to construct a buffer shown on the left side of Fig. 2-2 (c). Insert connection clips between A～B; F1～A1; A1～B1. Connect input A to SW0 and output F3 to L1. What is the state of F3 when SW0=0 and SW0=1?

   Does the circuit act as a buffer?

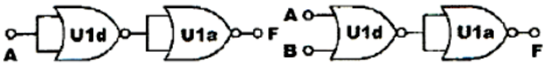


Fig. 2-2 (c) NOR gate use as Buffer and OR gate

5. Use U1a and U1c to construct an OR gate shown on the right side of Fig. 2-2 (c). Insert connection clips between F1～A1 and A1～B1. Connect inputs A to SW0, B to SW1; and output F3 to L1. Follow the input sequences shown below and record the output states in Table 2-1.

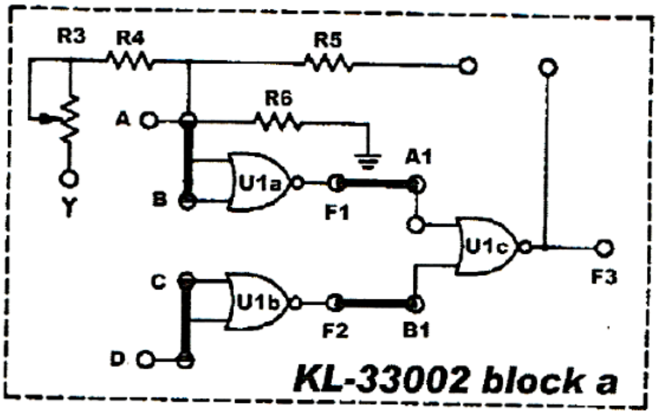
SW1(B)	SW0(A)	F
0	0	
0	1	
1	0	
1	1	

Table 2-1

6. Insert connection clips according to the figure below. The circuit will act as an AND gate.

(1) Connect A to SW0; D to SW1; F1 to A1; F2 to B1; F3 to L1.

(2) Follow the input sequences given below, record the output states in Table 2-2.



SW1(D)	SW0(A)	F3
0	0	
0	1	
1	0	
1	1	

Table 2-2

2-2 NAND Gate Circuit

OBJECTIVE

Understanding how to constructed various combinational logic gates with NAND gates.

Summary

The symbol of a NAND gate is shown in Fig. 2-4. The Boolean expression for a NAND gate is $F=\overline{A\times B}$; in de Morgan's theorem, $\overline{A\times B}=\overline{A}+\overline{B}$.

When A=B, $F=\overline{A\times B}=\overline{A}$. When B=1, $F=\overline{A\times B}=\overline{A\times 1}=\overline{A}$. Like the NOR gates, NAND gates can be used to construct just about any basic logic gates. We will attempt to construct various basic gates in this experiment by connecting NAND gates in different ways.

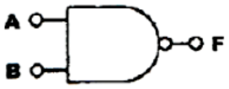


Fig. 2-4 Symbol of NAND gate

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Module KL-33002

PROCEDURES

1. Insert connection clips according to Fig. 2-5(a), using U2c and U2d to construct the NOT gate shown on left side of Fig. 2-5(b).

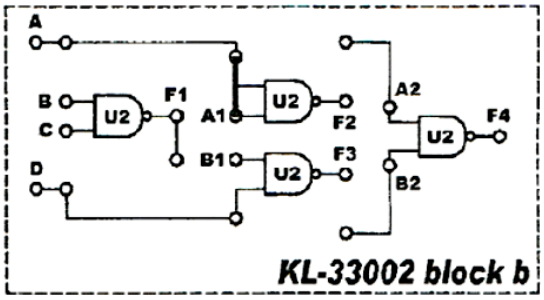
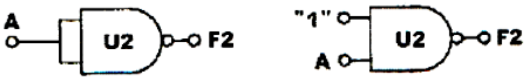


Fig. 2-5 (a)



(b) NOT gate constructed with NAND gate

(1) Connect input A to Data Switch SW1 and output F2 to A2 and Logic Indicator L1; connect B1 to Vcc ("1"). Observe the output states.

When SW1="0", F2=________
When SW1="1", F2=________

Does the circuit act as a NOT gate?

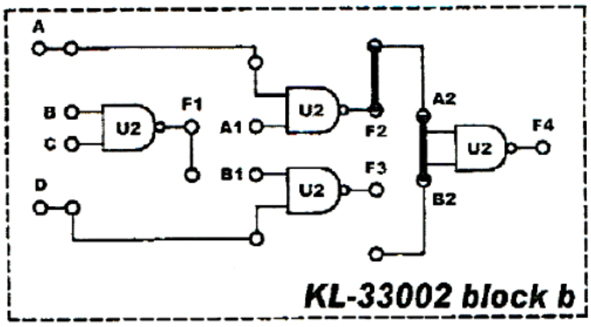
(2) Connect input A1 to Vcc ("1") and remove the connection clip between A and A1 to create the NOT gate shown on the right side of Fig. 2-5 (b). Other connections remain the same. Observe the output states.

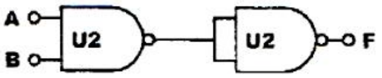
When SW1="0", F2=________
When SW1="1", F2=________

Does the circuit act as a NOT gate?

(3) Remove connection clips and insert them again according to Fig. 2-6 (a) to construct the AND gate shown in Fig. 2-6 (b). Connect A to SW1, A1 to SW2 and F4 to L1. Follow the input sequences given below and record the outputs in Table 2-4.

Does the circuit act as an AND gate (F=A × B)?





(b)

SW2(A1)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-4

2. Insert connection clips according to Fig. 2-7 (a) to construct the circuit of Fig. 2-7 (b). Connect A to A1 and SW1; F2 to A2; D to B1 and SW2; F3 to B2; F to L1. Follow the input sequences in Table 2-5 and record the outputs.

   Does the circuit act as an OR gate (F=A+B)?

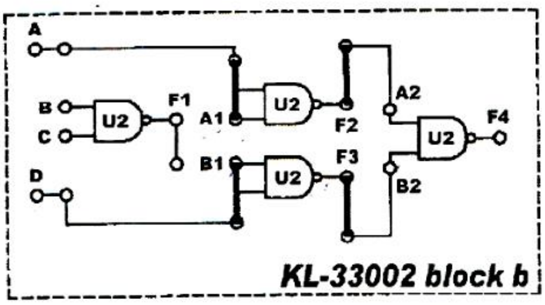
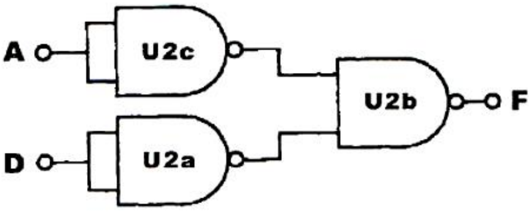


Fig 2-7 (a)



(b) OR gate constructed with NAND gate

SW2(D)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-5

2-3 XOR Gate Circuit

OBJECTIVE

Understanding the characteristics of XOR gates.

summary

The symbol of a XOR gate is shown in Fig. 2-8. The output F is equal to $\overline{A \oplus B} = \overline{A}B + A\overline{B}$. XOR gates can be constructed using NOT, OR, AND, NOR or NAND gates or by using four NAND gates, as shown in Fig. 2-9 (a) and (b).

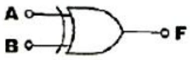
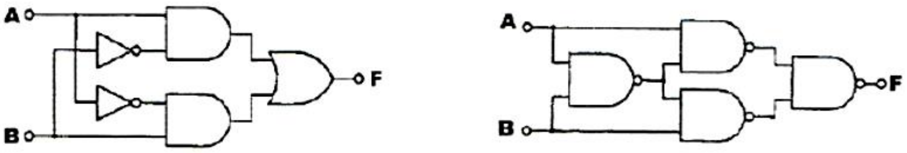


Fig. 2-8 Symbol of XOR gate



(a) with basic gates

(b) with NAND gates only

Fig. 2-9 XOR gate circuits

Since $F = \overline{A}B + A\overline{B}$, when B=0 $F = \overline{A} \times 0 + A \times \overline{0} = A \times 1 = 1$ and the circuit act as buffer. When B=1, $F = \overline{A} \times 1 + A \times \overline{1} = \overline{A} \times 1 = \overline{A}$, the circuit act as an inverter. In other words, the input state of a XOR gate determines whether it will act as a buffer or an inverter. In this experiment, we will use basic logic gates to construct XOR gates and study the relationship between the inputs and outputs.

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab, Module KL-33002

PROCEDURES

(a) Constructing XOR gate with NAND gate (Module KL-33002 block b)

1. Insert connection clips according to Fig. 2-10 (a) to construct the circuit of Fig. 2-10 (b). Connect inputs A to SW1, D to SW2; outputs F1 to L1, F2 to L2; F3 to L3 and F4 to L4.

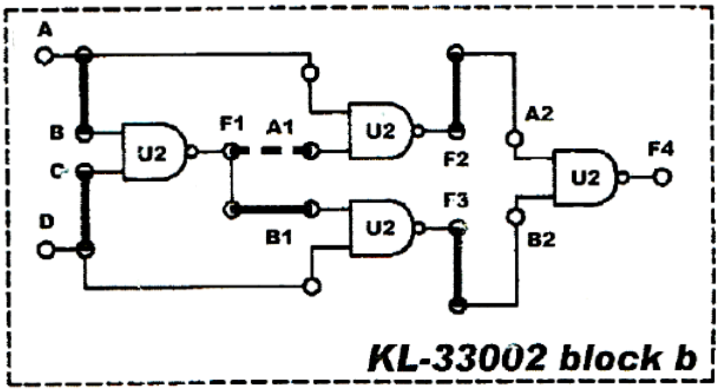
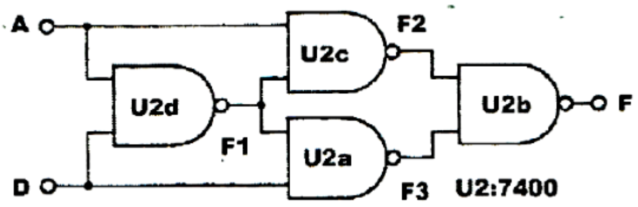


Fig. 2-10 (a)



(b) equivalent circuit

2. Follow the input sequences for A and D in Table 2-6 and record the outputs.

INPUT		OUTPUT			
D	A	F1	F2	F3	F4
0	0				
0	1				
1	0				
1	1				

Table 2-6

3. Determine the Boolean expression for F1, F2, F3, F4.

(b) Constructing XOR Gate with Basic Gate (Module KL-33002 block c)

1. Insert connection clips according to Fig. 2-11 (a) to construct the equivalent circuit of Fig. 2-11 (b).

2. Connect inputs A, B to SW1, SW2; outputs F1, F2, F3 to L1, L2, L3.

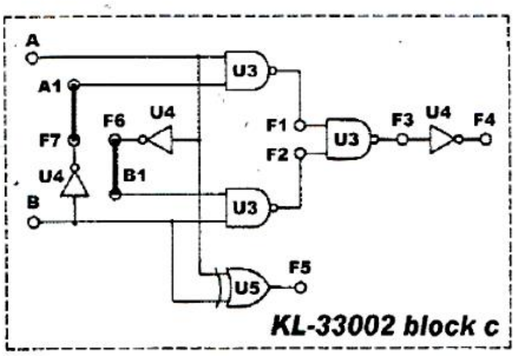
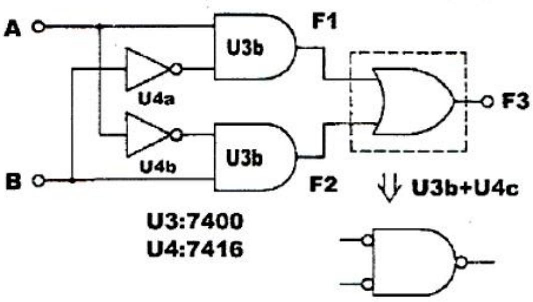


Fig. 2-11 (a)



(b) equivalent circuit

3. Follow the input sequences for A and B in Table 2-7 and record the outputs.

INPUT		OUTPUT		
SW2(B)	SW1(A)	F1	F2	F3
0	0			
0	1			
1	0			
1	1			

Table 2-7

2-4 AND-OR-INVERTER (A-O-I) Gate Circuits

OBJECTIVE

Understanding the basic principled of combined logic.

summary

AND-OR-INVERTER (A-O-I) gates consist of two AND gates, one OR gate and one INVERTER (NOT) gate. The symbol of an A-O-I gate is shown in Fig. 2-12. The Boolean expression for the output F is

$F=\overline{AB+CD}$ .... Equation (1)

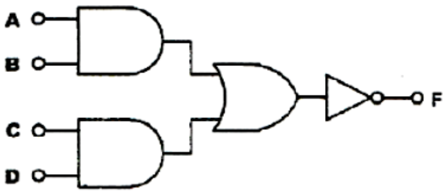


Fig. 2-12

Equation (1) can be converted into de Morgan's theorem as :

$F=(\overline{A}+\overline{B})\times(\overline{C}+\overline{D})$......... Equation (2)

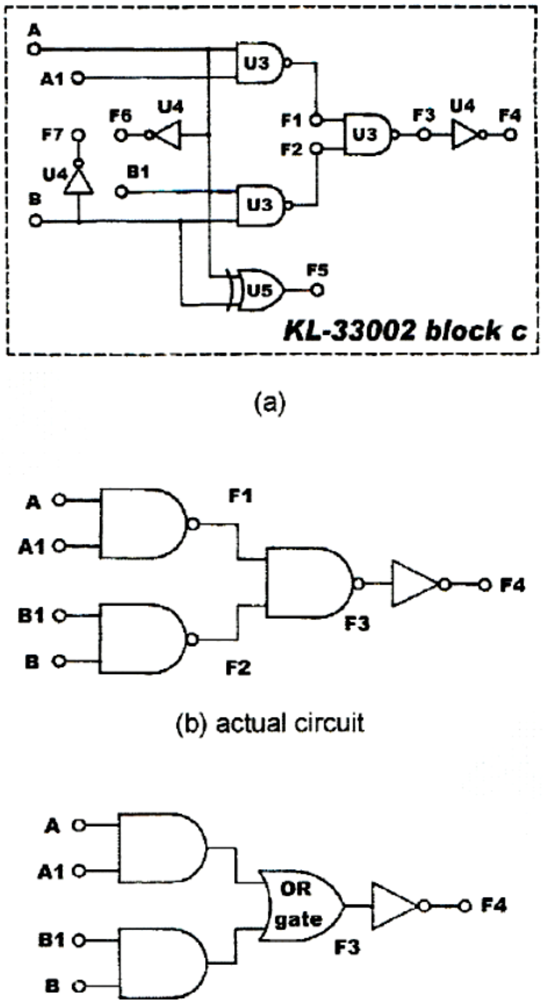
Equation (1) is also referred to as "Sum of Products".
Equation (2) is also referred to as "Product of Sum".
Basically, the A-O-I gate is a "Sum of Products" logic combination.

EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab; Module KL-33002

PROCEDURES

1. Use U3a, U3b, U3c and U4c on block c of Module KL-33002, shown in Fig. 2-13 (a), to construct the A-O-I gate of Fig. (b). Fig. 2-13 (c) is the equivalent A-O-I circuit which uses U3a, U3b, U3c used as the OR gate.



(a)

(b) actual circuit

(c) equivalent circuit

Fig. 2-13 A – O – I circuit

2. Connect inputs A, A1, B, B1 to Data Switches SW0, SW1, SW2, SW3 respectively. Connect outputs F3, F4 to Logic Indicators L1 and L2.

3. Set B×B1 to "0", follow the input sequences for A, A1 in Table 2-8 and record the outputs.

$B \times B1=0$

A1	A	F3	F4
0	0		
0	1		
1	0		
1	1		

Table 2-8

Does F3 act as an AND gate between A and A1?

4. When $B \times B1 \neq 0$, Does F3 act as an AND gate between A and A1? ($F3=A \times A1$)

5. When $A=A1=0$, follow the input sequences for B, B1 in Table 2-9 and record the outputs.

$A1 \times A=0$

B1	B	F3	F4
0	0		
0	1		
1	0		
1	1		

Table 2-9

Does F3 act as an AND gate between B and B1?

6. When $A \times A1 \neq 0$, Does F3 act as an AND gate between B and B1?

7. Does F3 equal to $A \times A1+B \times B1$?

DISCUSSION:

1- Sketch the logic circuit described by each of the following output expressions ?

a- $Y=\overline{A\overline{B}C+AB\overline{C}}$

b- $(A+B+C)(D+E)\overline{F}$

2- Show how the following expressions can be implemented using only NAND gates ?

a- $X=\overline{AB}+\overline{CD}$

b- $X=(A+B)(C+D)$

3- Write the truth table for a logic circuit that produces a 1 only when its three input variables represent a 2,5 or 7 in binary and a 0 output for all other input states?

4- Apply the distributive law and rule 7 to the equation?

$X= A(A+B)+C$

5- TTL SSI come mostly in 14-pin packages . Two pins are reserved for power supply and the other pins are used for input and output terminals. How many gates are enclosed in one such paelcage if it contains the following types of gates ?

a- 2-input exclusive – OR gates.

b- 3-input AND gate.

c- 4- input NAND gates.

d- 5-input NOR gates.

e- 8-input NAND gates.

6- Verify the truth table for 3-input exclusive OR gates?

7- Design a combinational logic circuit of binary code decimal (BCD) number to excess 3 code converter?