Multiplexer Circuit

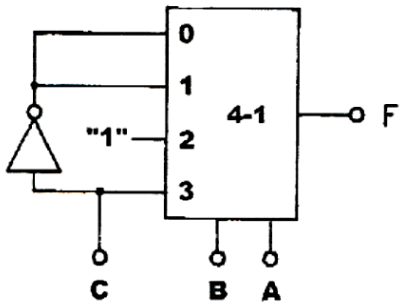
OBJECTIVE

Understanding the operating principles and construction of multiplexers.

Summary

Multiplexer, or MUX, is a logic circuit that select and route any number of inputs to a single output. One of the multiple inputs are selected by the selector gate and routed to the single output. The number of selector gates determine the capacity of a multiplexer. For example, if a certain MUX has only one selector gate, it is referred to as a "2 line-to-1 line MUX" because one selector can only select from two inputs.
A MUX with 3 selector gates is called "8 line-to-1 line MUX", since 3 selectors are capable of selecting an output from 8 inputs (2^3=8). MUX is also referred to as "Data Selector" because it selects one output from among many inputs.

Function expression, such as F(CBA)=Σ(0, 1, 2, 6, 7), can be easily executed on MUX. The function "F" generates the sum of products (CB+CB) from states 0, 1, 2, 6, 7. Refer to the 4 line-to-1 line MUX below, the output is determined by states of selectors A, Band C. When CBA=000, 001, 010, 110, 111 the output F is 1. In all other states F=0.



EQUIPMENTS REQUIRED

KL-31001 Digital Logic Lab, Module KL-33006

PROCEDURES

(a) Constructing a 2-to-1 Multiplexer

1. Block e of module KL-33006 will be used as a 2-to-1 MUX.

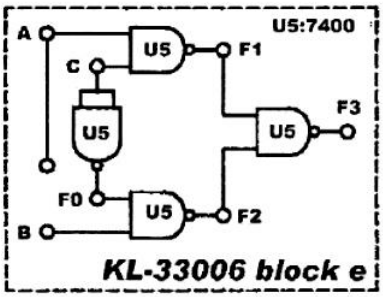


Fig. 2-71

2. Connect inputs A, B to Data Switches SW0, SW1; selector C to SW2. Connect output F3 to Logic Indicator L0.

3. Follow the input sequences in Table 2-34 and record states of F3. Which input (A or B) determines the output?

C	B	A	F3
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 2-34

(b) Using Multiplexers to Create Functions

1. Block f of module KL-33006 will be used in this section of the experiment to create functions.

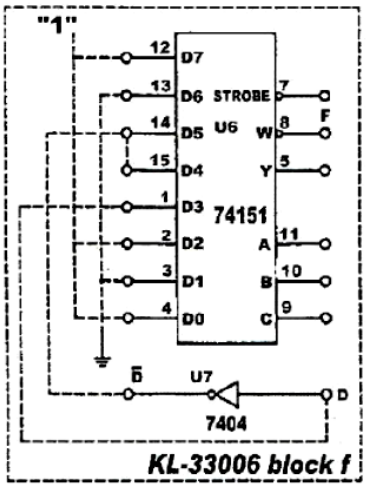


Fig. 2-72

2. Use U6 (74151) to create this function :

   F (D, C, B, A) = Σ(0, 2, 4, 5, 7, 8, 10, 11, 15)

$\overline{D}$	⓪	1	②	3	④	⑤	6	⑦
D	⑧	9	⑩	⑪	12	13	14	⑮

   Place connection leads according to Fig. 2-72 to complete the function shown above. Since D, C, B, A has 16 possible variations and the 74151 has only 8 variations, D will be used as the data input.

3. Connect inputs D, C, B, A to Data Switches SW3, SW2, SW1, SW0 respectively. Connect output Y to Logic Indicator L0. Follow the input sequences below and record output states.

D	C	B	A	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

(c) Constructing a 8 to 1 Multiplexer Circuit with TTL IC

1. U6 (74151) on block f of module KL-33006 will be used in section of the experiment.

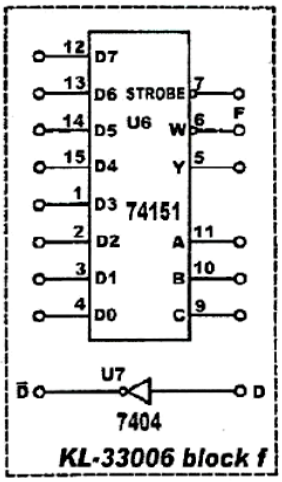


Fig. 2-73

2. Refer to the data book for specifications of the 74151.

   When CBA = "000", data at D0 is send to output F.
   When CBA = "010", data at D2 is send to output F.
   When CBA = "111", data at D7 is send to output F.
   The IC will function properly only when STROBE = "0".
   Y will remain "0" when STROBE = "1".

3. Connect inputs D0~D7 to DIP Switch 1.0~1.7; inputs C, B, A to DATA Switches SW2, SW1, SW0. Follow the input sequences in Table 2-35, adjust D0~D7 and record output states. Determine on which input among D0~D7 does F depend on.

C	B	A	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 2-35

DISCUSSION:

1- Use the 74151 to create this function shown below F(C,B,A)=∑(1,3,5,6) ?

2- Use the 74151 to create this function shown below
F(D,C,B,A)=∑(1,2 ,5,6,7,10,12,13,15)

3- Use 74150s and any other logic necessary to multiplex 32 date lines on to a single date-output line ?

4- Design 16x1 Mux using a suitable Mux ?

5- Design equation F(A,B,C,D)= ∑ (0,1,4,5,7,10,11,15) using 4x1 Mux?

6- Design 4x1 Mux using Enable pin at low active?